

E4M0025075U2

750V 25mΩ Automotive Silicon Carbide Power MOSFET
N-Channel Enhancement Mode



Features

- Industry standard Top Side Cooled (TSC) Package
- High power dissipation capability
- Optimized package with separate driver source pin
- High creepage package design
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

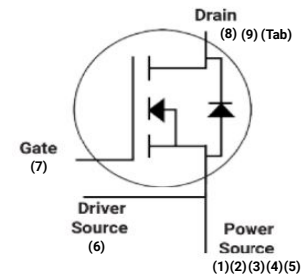
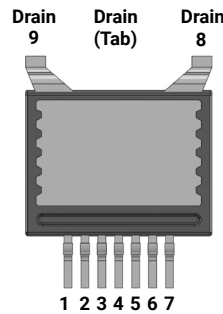
Benefits

- Increase power density
- Reduce cooling requirements
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increase system switching frequency

Typical Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

Package



Part Number	Package	Marking
E4M0025075U2	U2 (TSC)	E4M0025075U2

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			750	v	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	V_{GSop}		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			80	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19 Note 2
				58		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			251		t_{pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			288	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	750			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.8		$V_{DS} = V_{GS}, I_D = 9.22\ \text{mA}$	Fig. 11
			2.1			$V_{DS} = V_{GS}, I_D = 9.22\ \text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 750\ \text{V}, V_{GS} = 0\ \text{V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	m Ω	$V_{GS} = 15\ \text{V}, I_D = 33.5\ \text{A}$	Fig. 4, 5, 6
			41			$V_{GS} = 15\ \text{V}, I_D = 33.5\ \text{A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		24		S	$V_{DS} = 20\ \text{V}, I_{DS} = 33.5\ \text{A}$	Fig. 7
			24			$V_{DS} = 20\ \text{V}, I_{DS} = 33.5\ \text{A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		3055		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 500\ \text{V}$ $F = 100\ \text{kHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		158				
C_{rss}	Reverse Transfer Capacitance		16				
E_{oss}	C_{oss} Stored Energy		23		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		201		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0... 500\text{V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		291				
E_{on}	Turn-On Switching Energy (MOSFET FWD)		113		μJ	$V_{DS} = 500\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 33.5\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 25, 27
E_{off}	Turn-Off Switching Energy (MOSFET FWD)		42				
$t_{d(on)}$	Turn-On Delay Time		12		ns	$V_{DD} = 500\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 33.5\ \text{A}, R_{G(ext)} = 2.5\ \Omega,$ Timing relative to V_{DS} Inductive load	Fig. 26, 27
t_r	Rise Time		14				
$t_{d(off)}$	Turn-Off Delay Time		30				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		2.0		Ω	$f = 1\ \text{MHz}$	
Q_{gs}	Gate to Source Charge		33		nC	$V_{DS} = 500\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 33.5\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		40				
Q_g	Total Gate Charge		119				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 500V

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 500V


Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	$V_{GS} = -4\text{ V}, I_{SD} = 16.8\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2			$V_{GS} = -4\text{ V}, I_{SD} = 16.8\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		48	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
I_{SM}	Diode pulse Current		251		$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recovery time	17		ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.5\text{ A}, V_R = 500\text{ V}$ $dif/dt = 7125\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	650		nC		
I_{rrm}	Peak Reverse Recovery Current	63		A		
t_{rr}	Reverse Recovery time	23		ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.5\text{ A}, V_R = 500\text{ V}$ $dif/dt = 2718\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	431		nC		
I_{rrm}	Peak Reverse Recovery Current	31		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.4	0.52	$^\circ\text{C}/\text{W}$		Fig. 21



Typical Performance

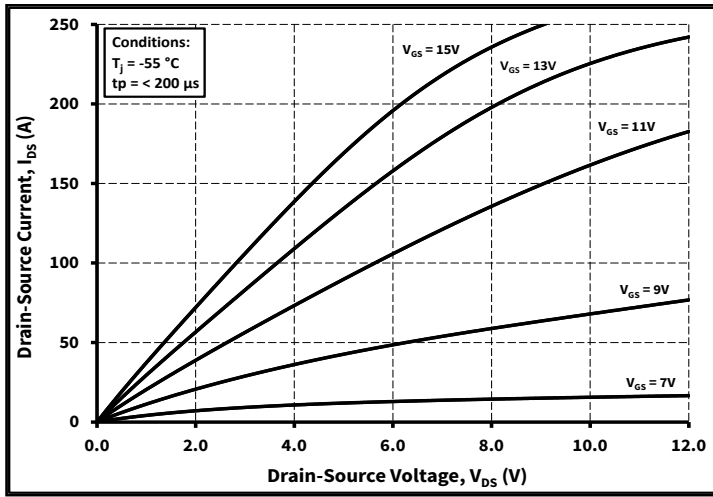


Figure 1. Output Characteristics $T_J = -55\text{ }^\circ\text{C}$

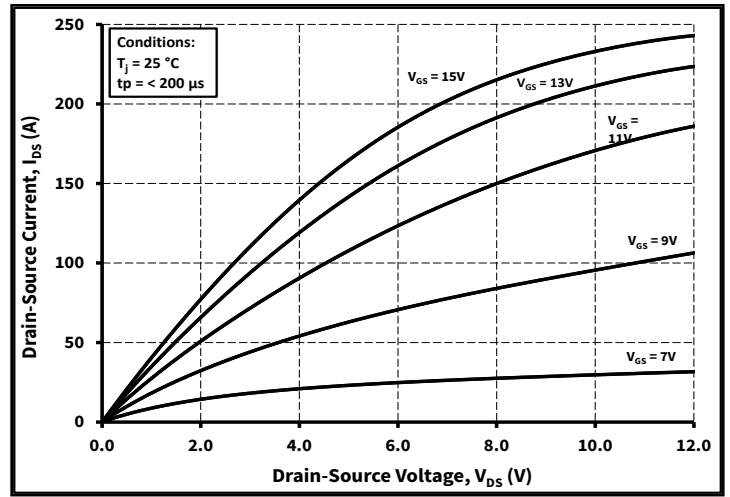


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

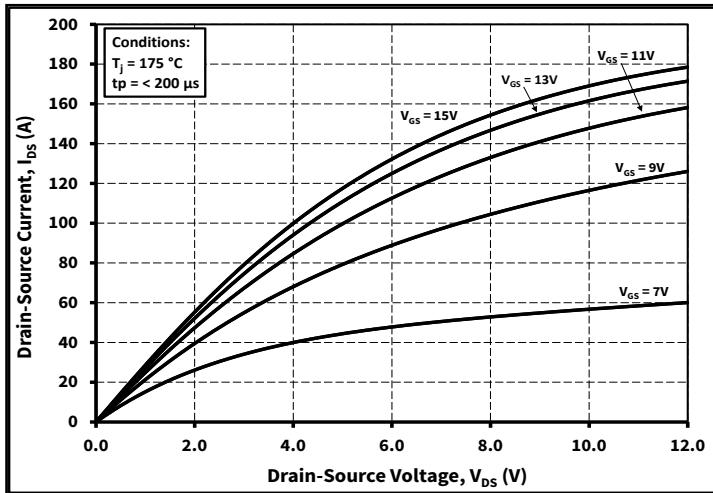


Figure 3. Output Characteristics $T_J = 175\text{ }^\circ\text{C}$

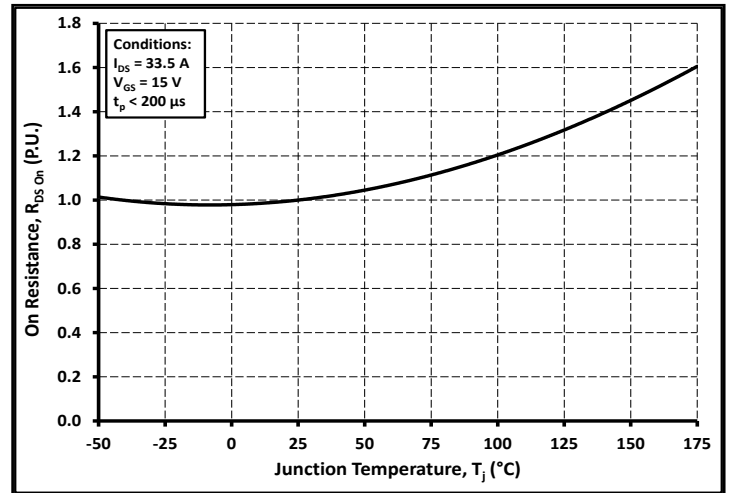


Figure 4. Normalized On-Resistance vs. Temperature

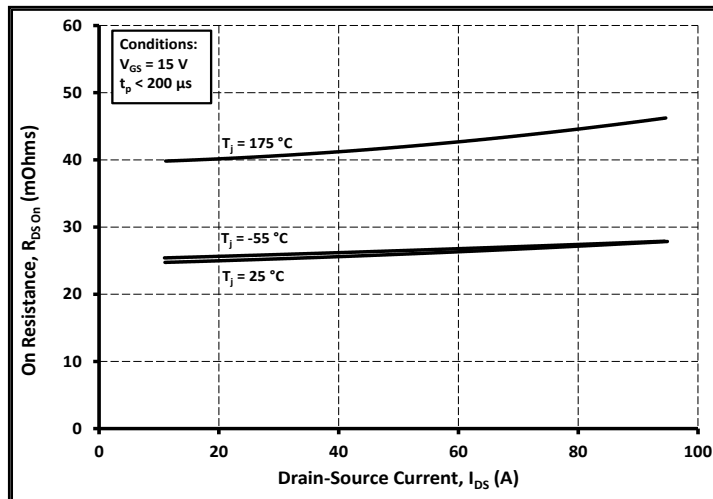


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

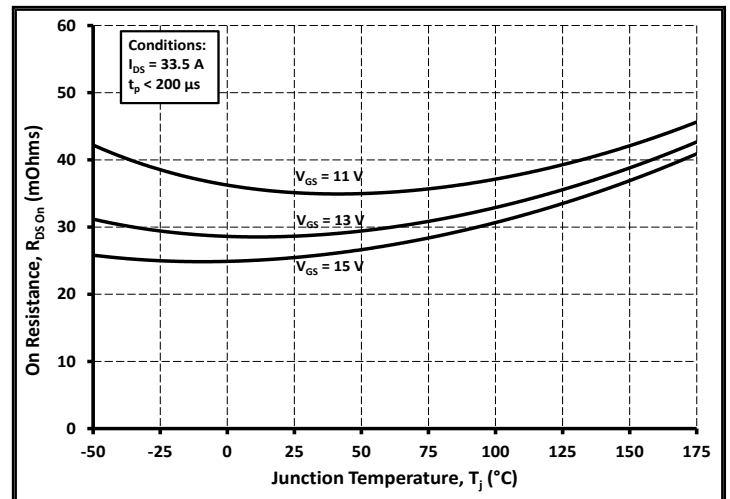


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

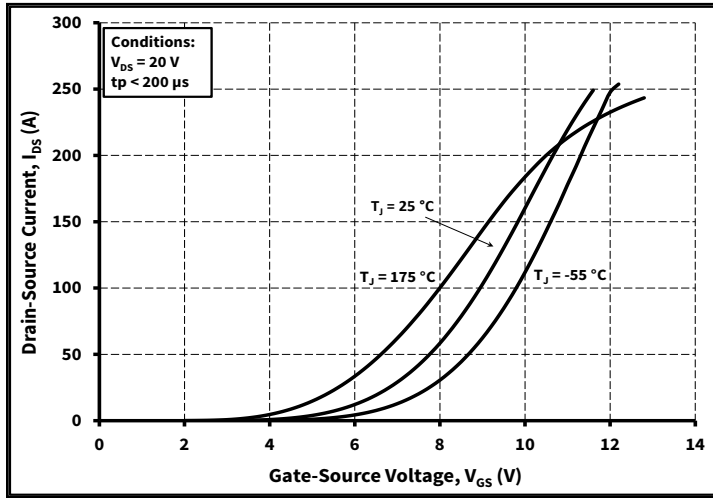


Figure 7. Transfer Characteristic for Various Junction Temperatures

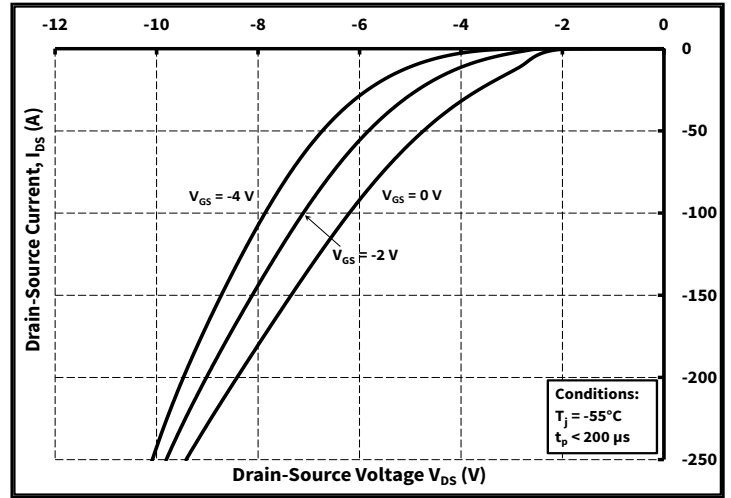


Figure 8. Body Diode Characteristic at -55 °C

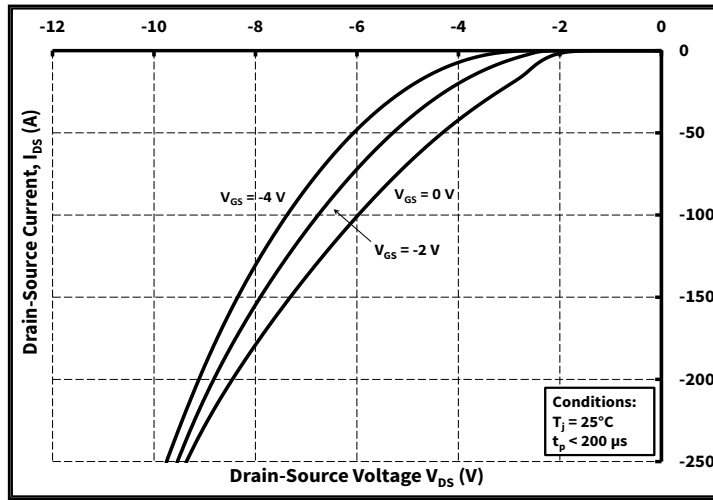


Figure 9. Body Diode Characteristic at 25 °C

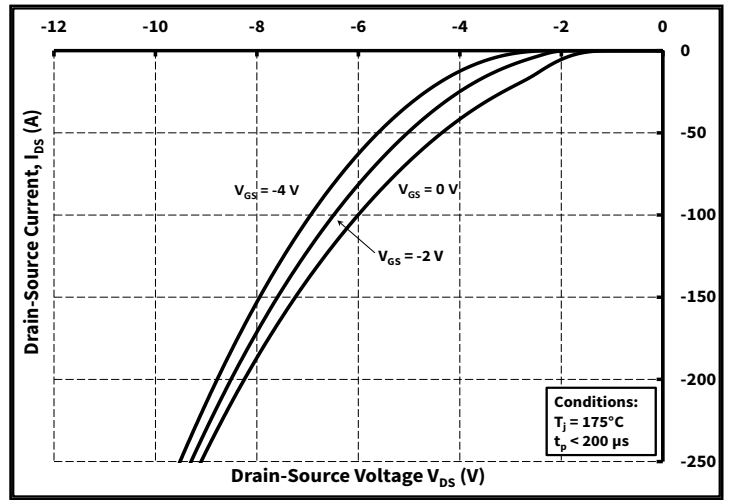


Figure 10. Body Diode Characteristic at 175 °C

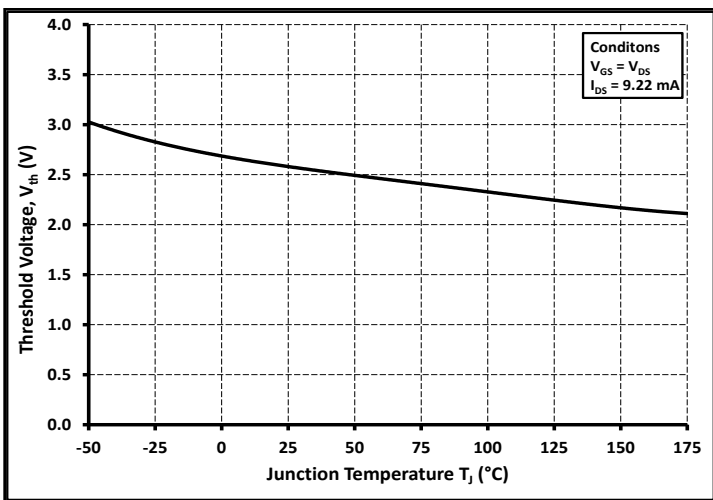


Figure 11. Threshold Voltage vs. Temperature

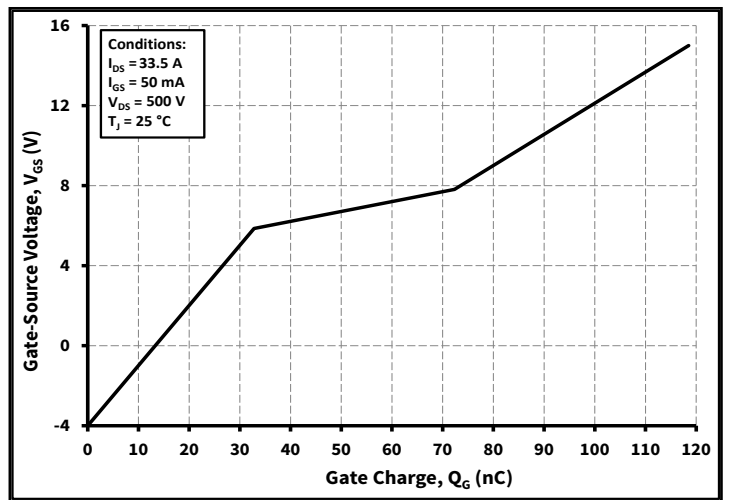


Figure 12. Gate Charge Characteristics



Typical Performance

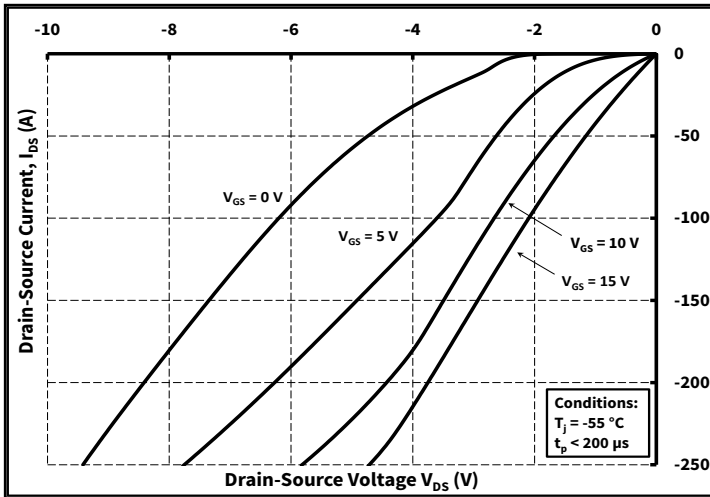


Figure 13. 3rd Quadrant Characteristic at -55 °C

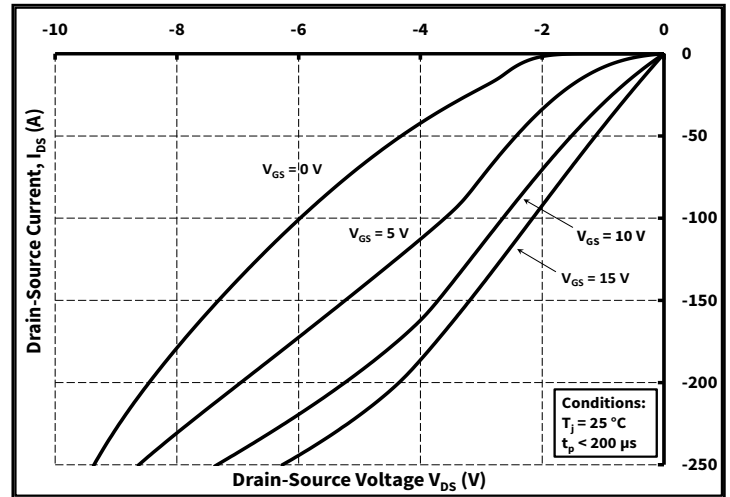


Figure 14. 3rd Quadrant Characteristic at 25 °C

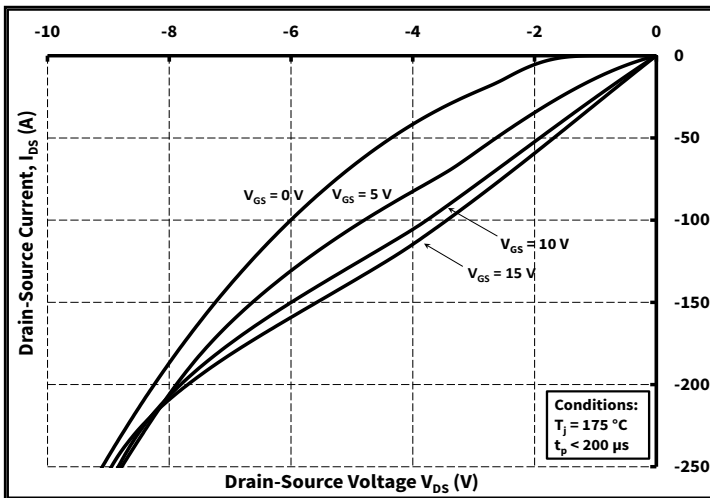


Figure 15. 3rd Quadrant Characteristic at 175 °C

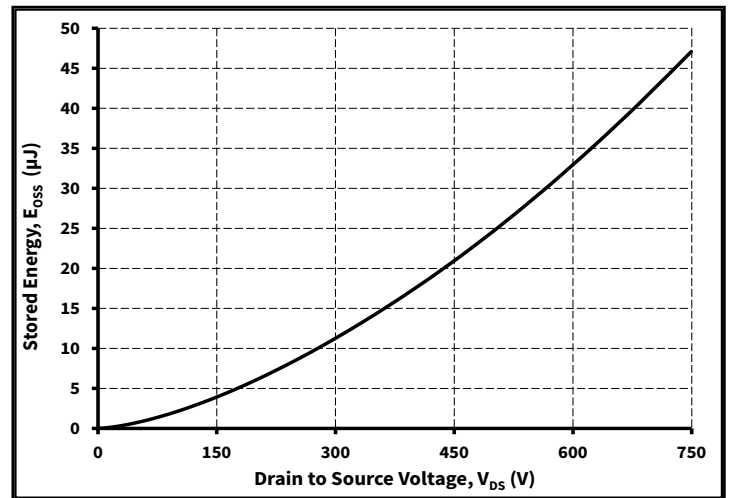


Figure 16. Output Capacitor Stored Energy

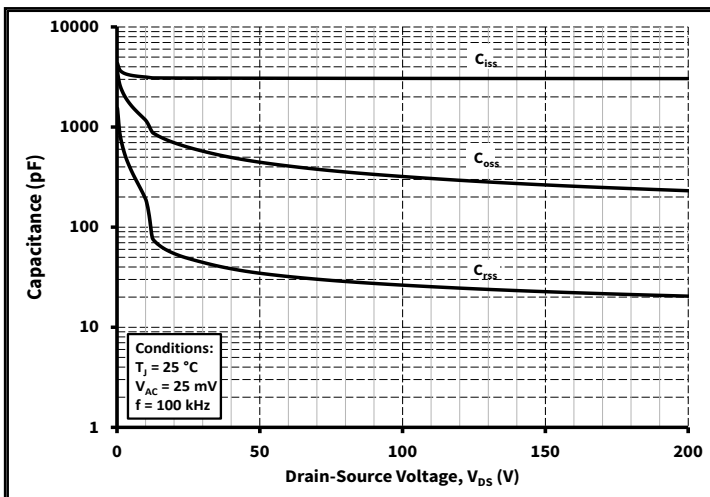


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

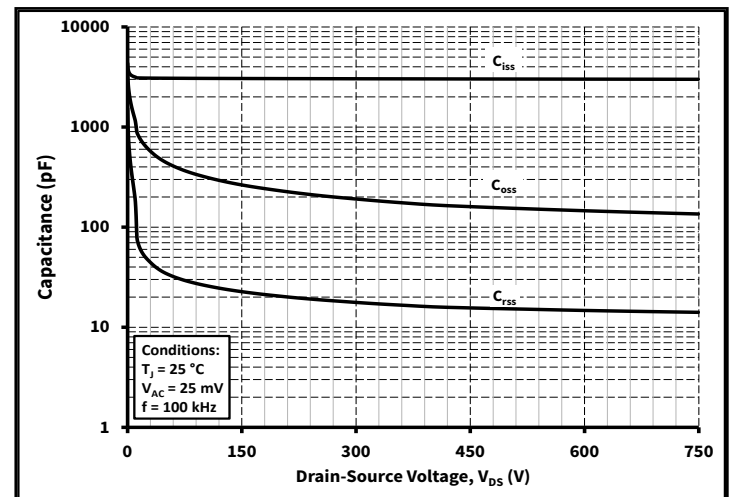


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 750V)



Typical Performance

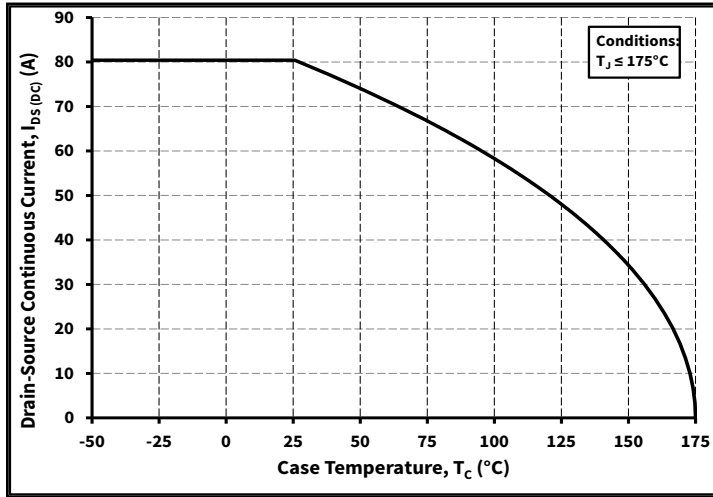


Figure 19. Continuous Drain Current Derating vs. Case Temperature

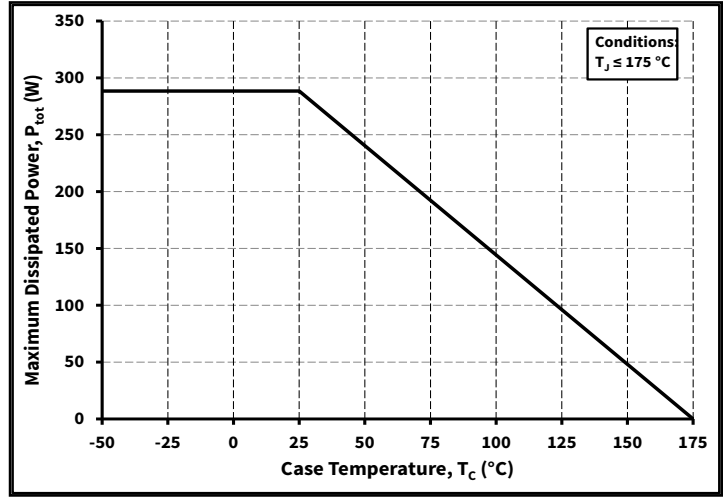


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

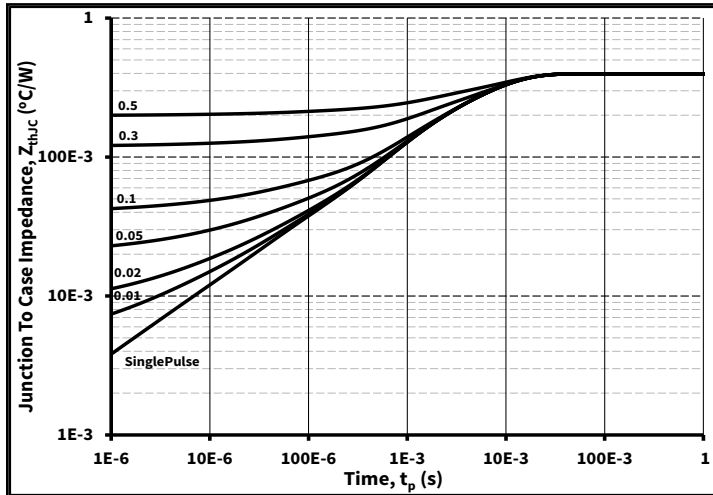


Figure 21. Transient Thermal Impedance (Junction - Case)

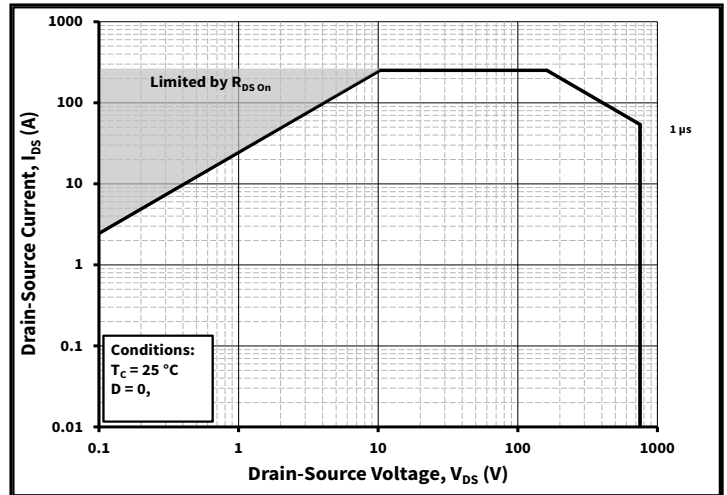


Figure 22. Safe Operating Area

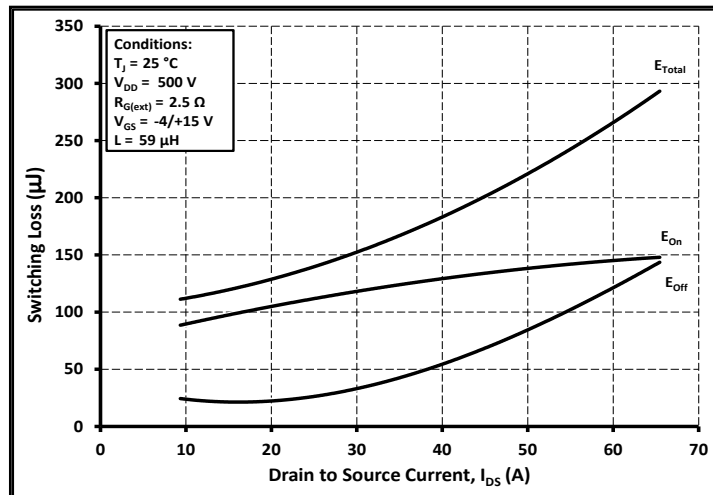


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 500V$)

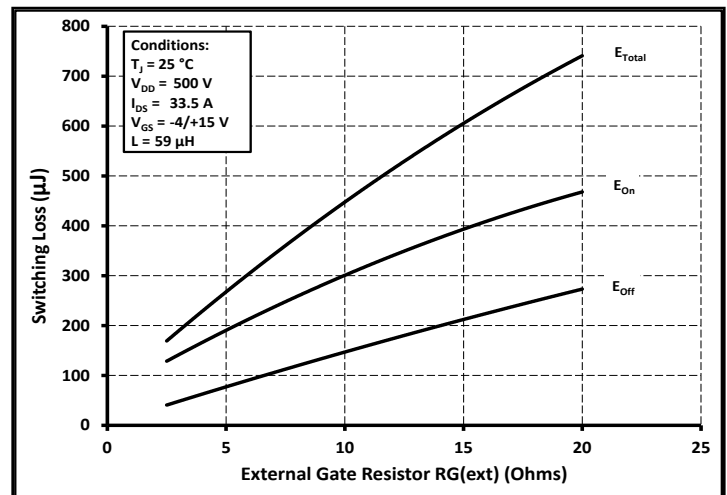


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$



Typical Performance

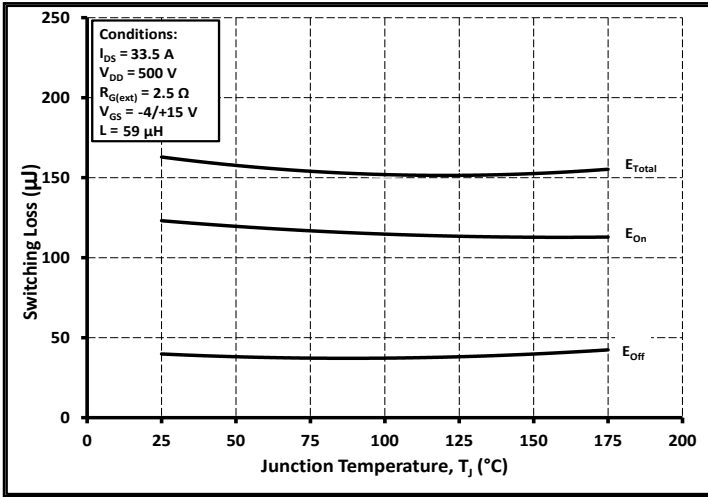


Figure 25. Clamped Inductive Switching Energy vs. Temperature

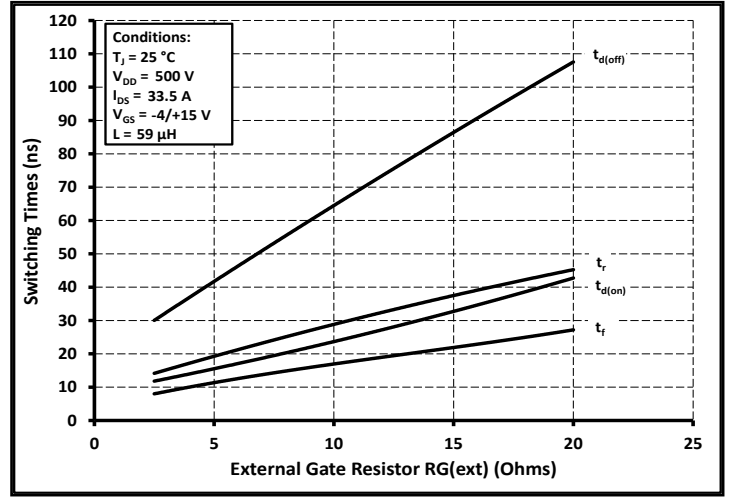


Figure 26. Switching Times vs. $R_{G(ext)}$

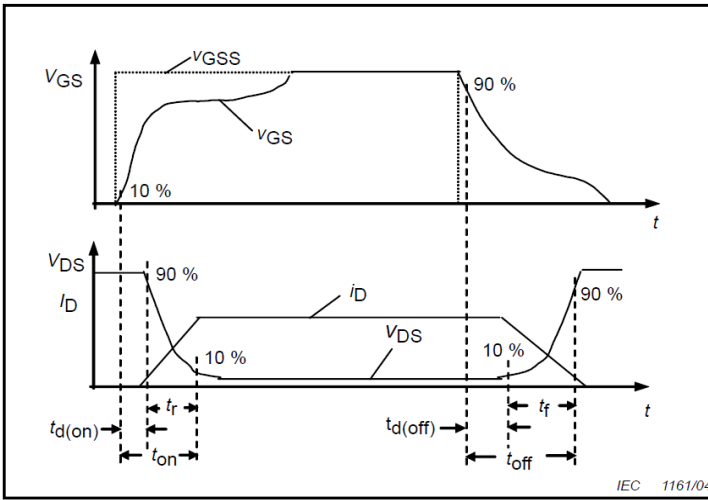


Figure 27. Switching Times Definition

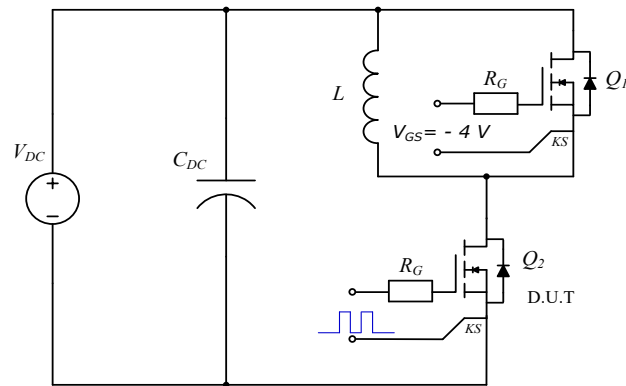
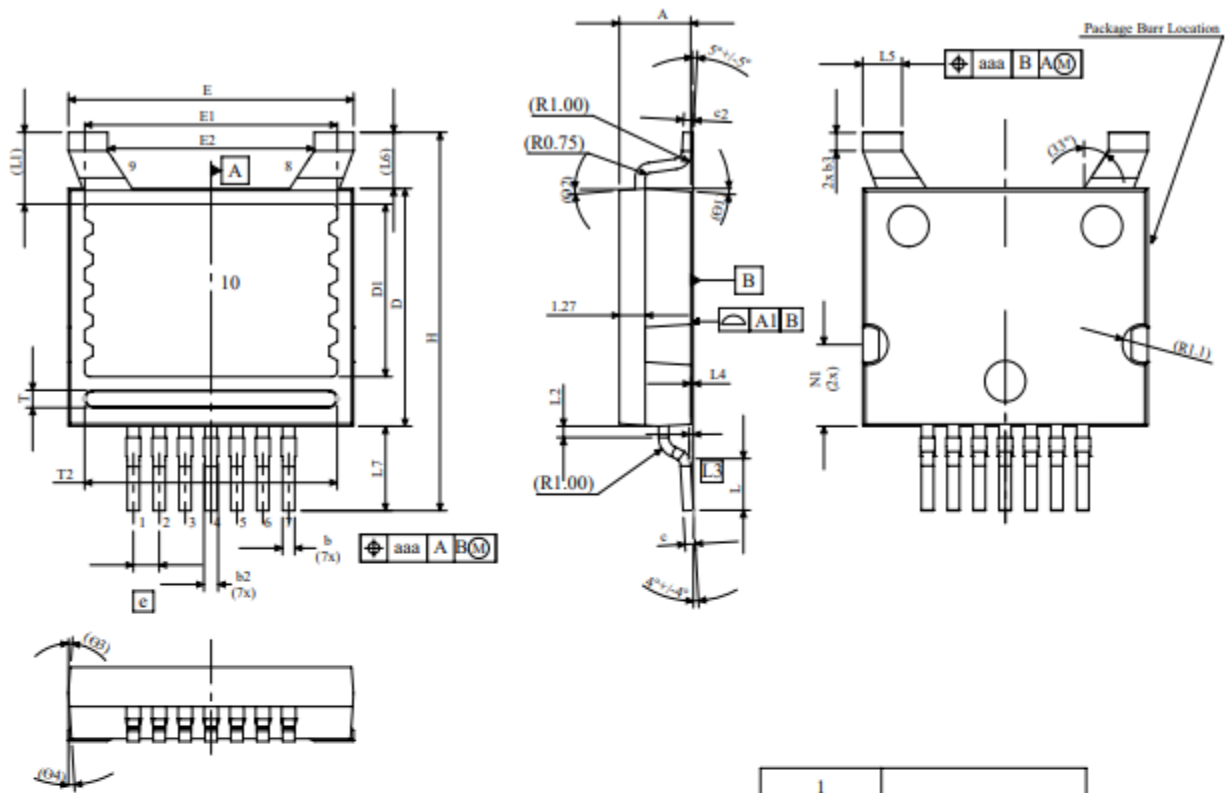
Test Circuit Schematic

Figure 28. Clamped Inductive Switching
Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	3.40	3.60
A1	---	0.05
b	0.50	0.70
b2	0.50	1.00
b3	0.85	1.05
c	0.40	0.60
c2	0.40	0.60
D	11.55	11.75
D1	8.30	8.50
E	13.92	14.12
E1	12.22	12.42
E2	9.92	10.22
e	BSC 1.27	
H	18.00	19.00
L	2.47	2.67
L1	BSC 3.51	
L2	0.3	0.73
L3	BSC 0.26	
L4	0.09	0.2
L5	1.83	2.13
L6	BSC 2.75	
L7	4.03	4.23
T	0.75	0.95
T2	12.30	12.50
N1	3.90	4.10
Θ1	0°	8°
Θ2	0°	8°
Θ3	0°	8°
Θ4	0°	8°
aaa	---	0.10

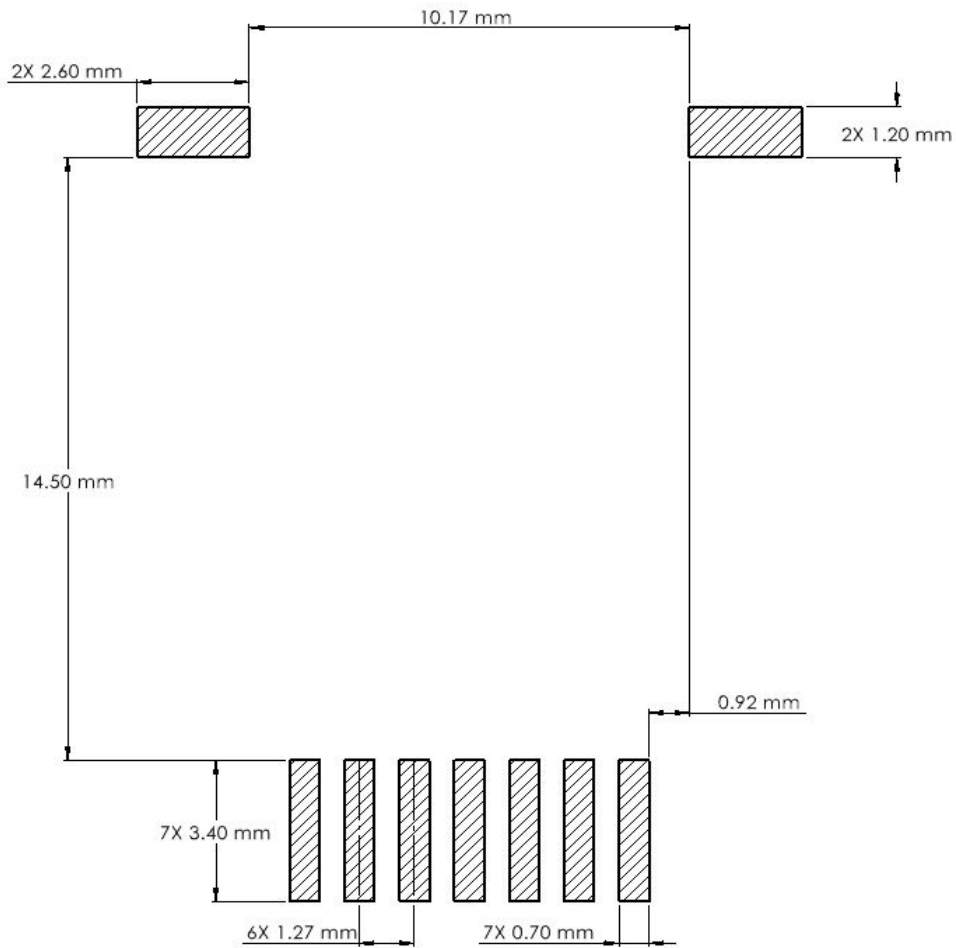
1	SOURCE
2	
3	
4	
5	
6	DRIVER SOURCE
7	GATE
8	DRAIN
9	DRAIN
10	DRAIN

- NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
 2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
 4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



Recommended Solder Pad Layout

All dimensions in mm





Revision history

Document Version	Date of release	Description of changes
1	December - 2025	Initial datasheet



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