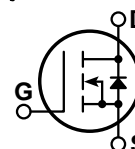
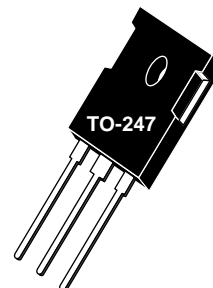


POWER MOS V®

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **100% Avalanche Tested**
- **Lower Leakage**
- **Popular TO-247 Package**

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT8075BVR	UNIT
V_{DSS}	Drain-Source Voltage	800	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	12	Amps
I_{DM}	Pulsed Drain Current ^①	48	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	260	Watts
	Linear Derating Factor	2.08	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	12	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	960	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	800			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	12			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.75	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			25	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			250	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0\text{mA}$)	2		4	Volts



CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

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DYNAMIC CHARACTERISTICS

APT8075BVR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		2600	3120	pF
C_{oss}	Output Capacitance			270	380	
C_{rss}	Reverse Transfer Capacitance			135	200	
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$		130	195	nC
Q_{gs}	Gate-Source Charge			13	20	
Q_{gd}	Gate-Drain ("Miller") Charge			66	100	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$ $R_G = 1.6\Omega$		12	24	ns
t_r	Rise Time			11	22	
$t_{d(off)}$	Turn-off Delay Time			45	70	
t_f	Fall Time			8	16	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			12	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			48	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -I_{D[Cont.]}$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$)		600		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$)		8		μC

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.48	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

③ See MIL-STD-750 Method 3471

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

④ Starting $T_j = +25^\circ C$, $L = 13.33mH$, $R_G = 25\Omega$, Peak $I_L = 12A$

APT Reserves the right to change, without notice, the specifications and information contained herein.

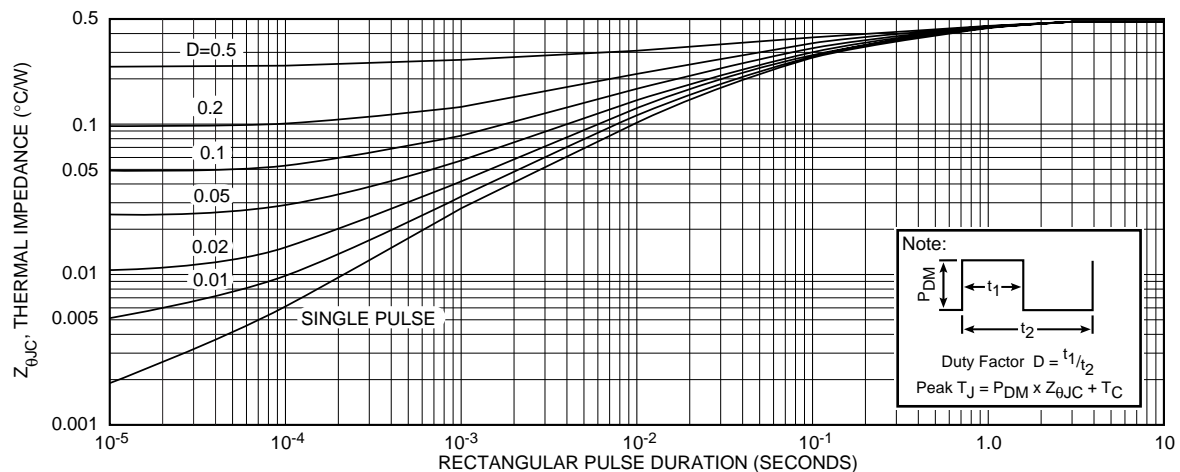


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

APT8075BVR

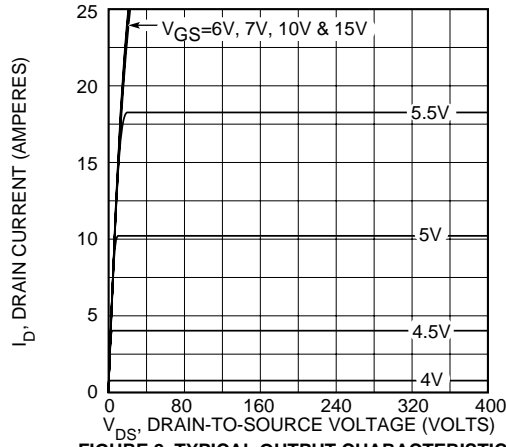


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

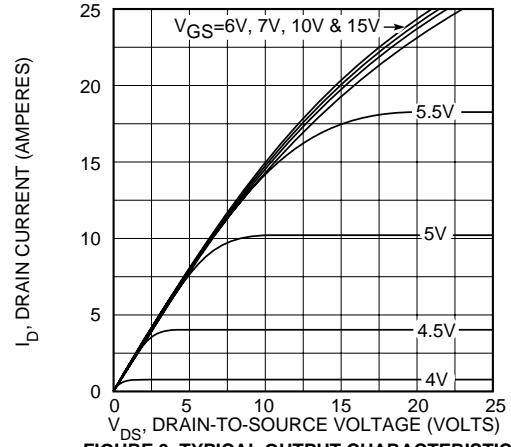


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

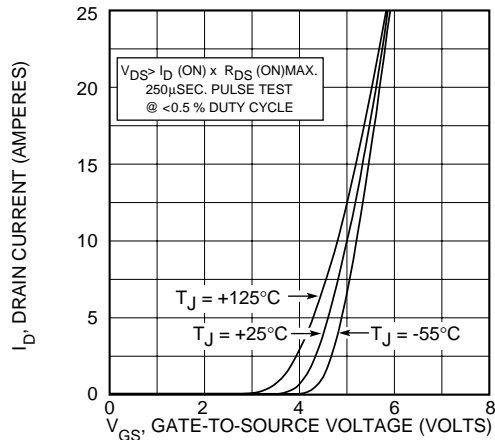


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

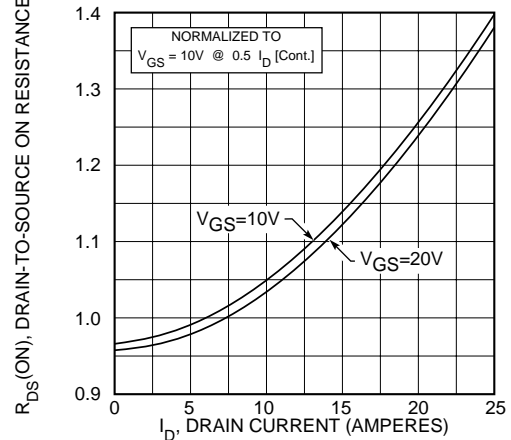


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

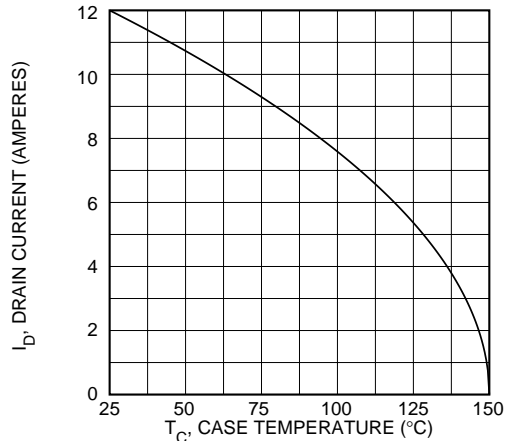


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

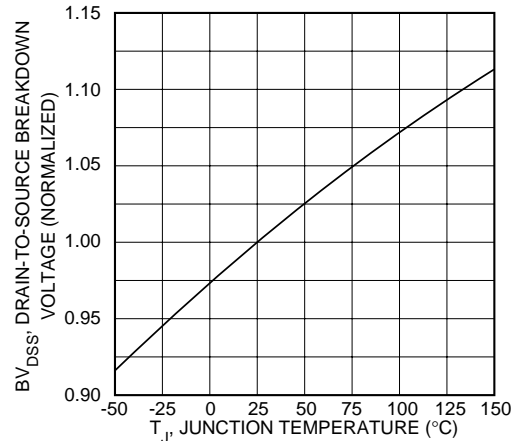


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

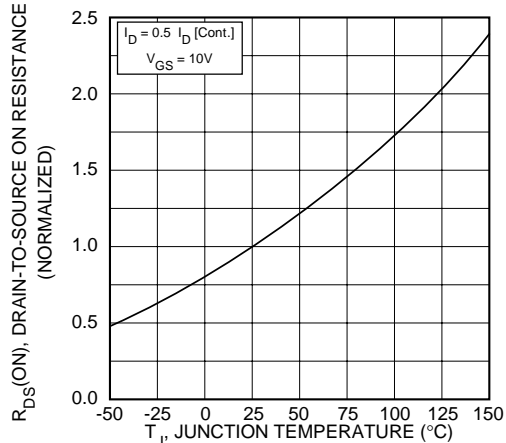


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

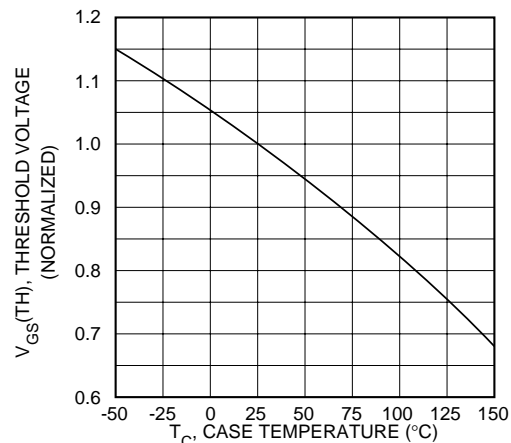


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE



Figure 1: Mechanical drawing of the 2-Plcs. package. The drawing includes a side view on the left and a top view on the right. The side view shows a package with a 'Drain' label pointing to a central feature. Dimensions include 4.69 (.185), 5.31 (.209), 1.49 (.059), 2.49 (.098), 0.40 (.016), 0.79 (.031), 2.21 (.087), and 2.59 (.102). The top view shows a square package with a central circular feature and four pins. Dimensions include 15.49 (.610), 16.26 (.640), 6.15 (.242) BSC, 20.80 (.819), 21.46 (.845), 4.50 (.177) Max., 19.81 (.780), 20.32 (.800), 1.01 (.040), 1.40 (.055), 5.45 (.215) BSC, 5.38 (.212), 6.20 (.244), 3.50 (.138), 3.81 (.150), 2.87 (.113), 3.12 (.123), 1.65 (.065), and 2.13 (.084). Labels 'Gate', 'Drain', and 'Source' are present near the pins.

APT's devices are covered by one or more of the following U.S.patents:	4,895,810	5,045,903	5,089,434	5,182,234	5,019,522	5,262,336
	5,256,583	4,748,103	5,283,202	5,231,474	5,434,095	5,528,058