DSC557-03/04/05

Multiple Output MEMS PCIe Gen1/2/3/4 Clock Generators

Features

- Complies with PCIe Gen1/2/3/4 Common Clock Spec
- Integrated MEMS Resonator Eliminates the Need for External 25 MHz Crystal
- Wide Temperature Range:
  - Ext. Industrial: –40°C to +105°C
  - Industrial: –40°C to +85°C
  - Commercial: –20°C to +70°C
- 100 MHz HCSL/LVDS/LVCMOS Options Available
- Dedicated Output Enable (OE) Pins for Clock Outputs
- Small Footprints:
  - 14-Lead VQFN (DSC557-03, Two Outputs)
  - 20-Lead VQFN (DSC557-04, Three Outputs; DSC557-05, Four Outputs)
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Low Current Consumption: 30% Lower than Competing Devices
- Supply Range of 2.25V to 3.63V
- Lead-Free and RoHS Compliant

Applications

- Communications/Networking
  - Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FcoE
  - Routers and Switches
  - Gateways, VoIP, Wireless APs
  - Passive Optical Networks
- Storage
  - SAN, NAS, SSD, JBOD
- Embedded Applications
  - Industrial, Medical, and Avionics
  - Security Systems and Office Automation
  - Digital Signage, POS, and Others
- Consumer Electronics
  - Smart TV, Blu-Ray, STB

General Description

The DSC557 series of high performance PCI Express clock generators use a proven silicon MEMS technology to provide 100 MHz differential output clocks with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

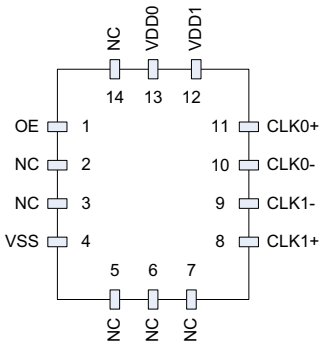
The DSC557-03/04/05 have two, three, and four 100 MHz outputs, respectively. All have output enable/disable features.

The DSC557-03 is available in a space-saving 14-lead VQFN package. The DSC557-04 and DSC557-05 are available in a 20-lead VQFN.

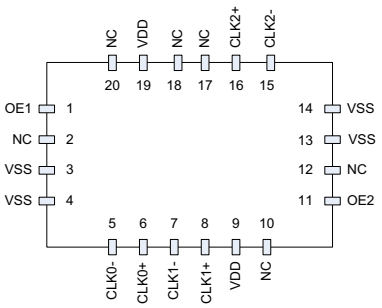
Additional LVDS and LVCMOS output formats are available in addition to the default HCSL output format.

Package Types

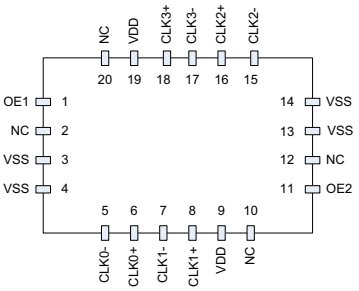
DSC557-03
14-Lead VQFN
(Top View)



DSC557-04
20-Lead VQFN
(Top View)

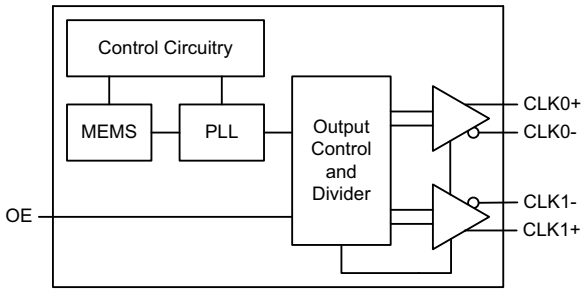


DSC557-05
20-Lead VQFN
(Top View)

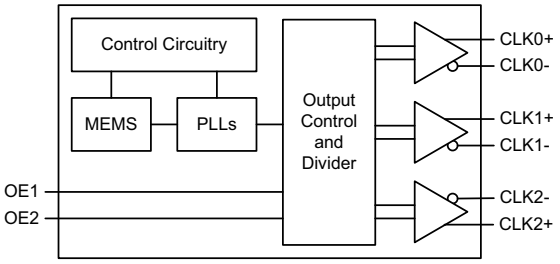


Block Diagrams

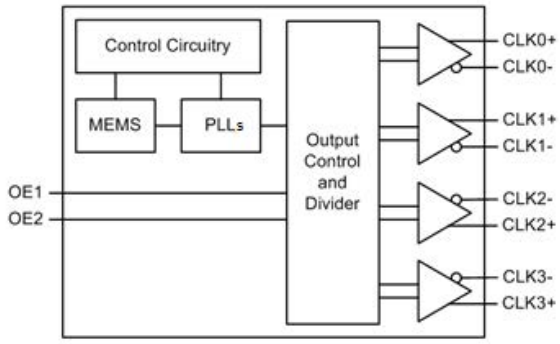
DSC557-03



DSC557-04



DSC557-05



Note: CLK0+/–, CLK1+/–, CLK2+/–, and CLK3+/– are 100 MHz, per PCIe standards.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage ..... –0.3V to V_{DD} + 0.3V
Supply Voltage ..... –0.3V to +4.0V
ESD Protection on All Pins (HBM) ..... 4 kV
ESD Protection on All Pins (CDM) ..... 1.5 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.25	—	3.63	V	Note 1
Supply Current, DSC557-03	I_{DD}	—	21	23	mA	HCSL output, EN pin low, output disabled
		—	60	—		HCSL output, EN pin high, output enabled
Supply Current, DSC557-04	I_{DD}	—	42	46	mA	HCSL output, EN pin low, output disabled
		—	100	—		HCSL output, EN pin high, output enabled
Supply Current, DSC557-05	I_{DD}	—	42	46	mA	HCSL output, EN pin low, output disabled
		—	120	—		HCSL output, EN pin high, output enabled
Frequency Stability (including frequency variations due to initial tolerance, temp., and power supply voltage)	Δf	—	—	±100	ppm	All temperature ranges
		—	—	±50		
Aging - 1st Year	Δf	—	—	±5	ppm	±1 ppm each subsequent year
Startup Time (Note 2)	t_{SU}	—	—	5	ms	T = +25°C
Input Logic Levels						
Input Logic High	V_{IH}	0.75 x V_{DD}	—	—	V	—
Input Logic Low	V_{IL}	—	—	0.25 x V_{DD}	V	—
Output Disable Time (Note 3)	t_{DS}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	20	ns	—
Enable Pull-Up Resistor (Note 4)	—	—	40	—	kΩ	Internally pulled up
HCSL Outputs (Note 5)						
Output Logic High	V_{OH}	0.725	—	—	V	R_L = 50Ω
Output Logic Low	V_{OL}	—	—	0.1	V	R_L = 50Ω
Peak-to-Peak Output Swing	—	—	750	—	mV	Single-Ended
Output Frequency	f_{OUT}	—	100	—	MHz	—

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Transition Time (Note 6)	t_r/t_f	200	—	400	ps	20% to 80%, R_L = 50Ω, C_L = 2 pF
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter (Note 7)	J_{PER}	—	2.5	—	ps_{RMS}	$f_{01} = f_{02}$ = 100 MHz
Jitter, Phase (Common Clock Architecture)	T_J	—	17	86	ps_{PP}	PCIe Gen 1.1, (Note 8) $T_J = D_J + 14.069 \times R_J$ (BER 10^{-12})
	$J_{RMS-CCHF}$	—	1.46	3.1	ps_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist, (Note 8)
	$J_{RMS-CCLF}$	—	0.08	3.0	ps_{RMS}	PCIe Gen 2.1, 10 kHz to 1.5 MHz, (Note 8)
	J_{RMS-CC}	—	0.313	1.0	ps_{RMS}	PCIe Gen 3.0, (Note 8)
	J_{RMS-CC}	—	0.313	0.5	ps_{RMS}	PCIe Gen 4.0, 16 GHz, (Note 8)
Integrated Phase Noise (Data Clock Architecture)	$J_{RMS-DCHF}$	—	2.15	4.0	ps_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist, (Note 8)
	$J_{RMS-DCLF}$	—	0.06	7.5	ps_{RMS}	PCIe Gen 2.1, 10 kHz to 1.5 MHz, (Note 8)
	J_{RMS-DC}	—	0.32	1.0	ps_{RMS}	PCIe Gen 3.0, (Note 8)
LVDS Output						
Offset Voltage	V_{OS}	1.125	1.25	1.40	V	V_{DD} = 2.5V/3.3V
V_{OS} Magnitude Change	ΔV_{OS}	—	—	50	mV	—
Output High Voltage	V_{OH}	$0.9xV_{DD}$	—	—	V	—
Output Low Voltage	V_{OL}	—	—	$0.1xV_{DD}$	V	—
Output Frequency	f_{OUT}	—	100	—	MHz	—
Differential Output Voltage	V_{OD}	275	350	475	mV_{PP}	—
V_{OD} Magnitude Change	ΔV_{OD}	—	—	40	mV	—
LVDS Output Rise/Fall Time	t_r/t_f	—	200	—	ps	20% – 80%
Output Duty Cycle	ODC	48	50	52	%	20% – 80%, R_L = 50Ω, C_L = 2 pF
Period Jitter, Peak to Peak	J_{PTP}	—	2.5	—	ps	f_{OUT} = 100 MHz, Standard Drive
Integrated Phase Noise	J_{PH}	—	0.28	—	ps_{RMS}	200 kHz to 20 MHz @ 100 MHz, T_A = +105°C
		—	0.4	—		100 kHz to 80 MHz @ 100 MHz
		—	1.7	2.0		12 kHz to 10 MHz @ 100 MHz

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
LVCMOS Output						
Output High Voltage	V_{OH}	0.8xV_{DD}	—	—	V	±10 mA drive current
Output Low Voltage	V_{OL}	—	—	0.2xV_{DD}	V	±10 mA drive current
Output Frequency	f_{OUT}	—	100	—	MHz	—
Output Rise/Fall Time	t_r/t_f	—	1.2	—	ns	20% – 80%, C_L = 15 pF
Output Duty Cycle	ODC	48	50	52	%	f_{OUT} = 100 MHz, Standard Drive
Period Jitter	J_{PTP}	—	3	—	ps_{RMS}	f_{OUT} = 100 MHz, Standard Drive
Integrated Phase Noise	J_{PH}	—	0.3	—	ps_{RMS}	200 kHz to 20 MHz @ 100 MHz
		—	0.38	—		100 kHz to 20 MHz @ 100 MHz
		—	1.7	2.0		12 kHz to 20 MHz @ 100 MHz

Note 1: Each pin V_{DD} should be filtered with a 0.1 µF capacitor.

2: t_{SU} is time to 100 ppm of output frequency after V_{DD} is applied and outputs are enabled.

3: Output Waveform and Test Circuit figures define the parameters.

4: Output is enabled if pad is floated or not connected.

5: Contact Microchip for alternate output options (LVDS, LVCMOS).

6: Output Waveform and Connection Diagram define the parameters.

7: Period Jitter includes crosstalk from adjacent output.

8: Jitter limits established by Gen 1.1, Gen 2.1, Gen 3.0, and Gen 4.0 PCIe standards.

TEMPERATURE SPECIFICATIONS

Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	–20	—	+70	°C	Ordering Option E
		–40	—	+85	°C	Ordering Option I
		–40	—	+105	°C	Ordering Option L
Junction Operating Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–55	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 40s

2.0 PIN DESCRIPTIONS AND CONNECTION DIAGRAMS

The descriptions of the pins are listed in Table 2-1, Table 2-2, and Table 2-3.

TABLE 2-1: DSC557-03 VQFN-14 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	OE	I	Output enable, active-high.
2	NC	N/A	Ground recommended or leave as a NC.
3	NC	N/A	Ground recommended or leave as a NC.
4	VSS	P	Ground.
5	NC	N/A	Ground recommended or leave as a NC.
6	NC	N/A	Ground recommended or leave as a NC.
7	NC	N/A	Ground recommended or leave as a NC.
8	CLK1+	O	True output of differential pair.
9	CLK1–	O	Complement output of differential pair.
10	CLK0–	O	Complement output of differential pair.
11	CLK0+	O	True output of differential pair.
12	VDD1	P	Power supply for core and output 1 (CLK1+/CLK1–)
13	VDD0	P	Power supply for output 0 (CLK0+/CLK0–)
14	NC	N/A	Ground recommended or leave as a NC.

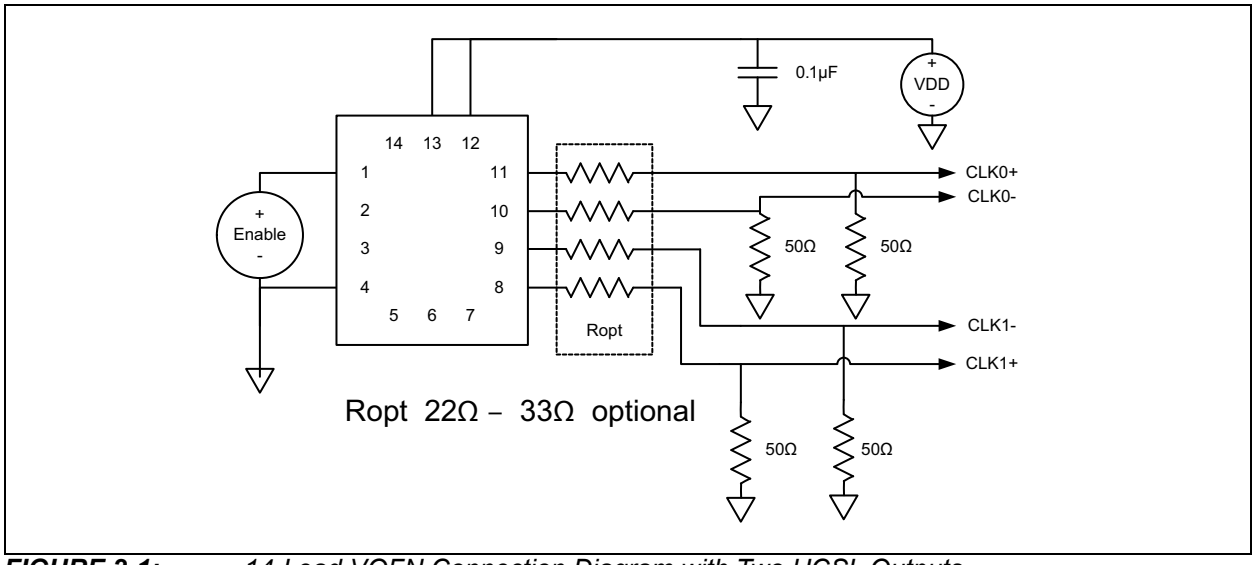


FIGURE 2-1: *14-Lead VQFN Connection Diagram with Two HCSL Outputs.*

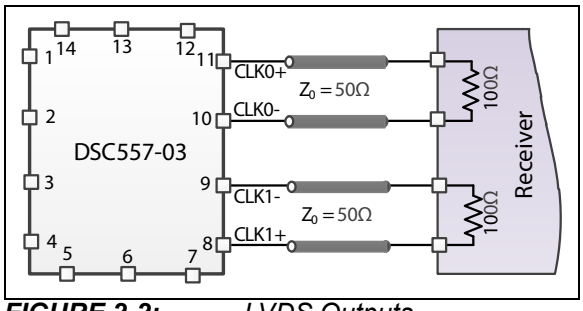


FIGURE 2-2: *LVDS Outputs.*

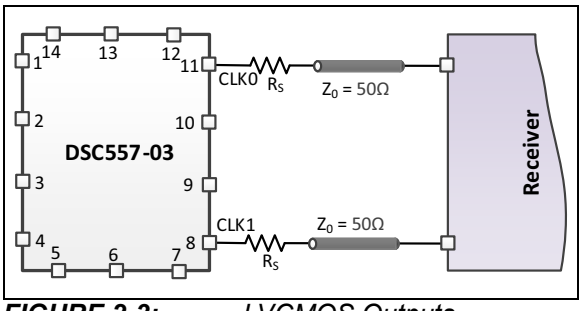


FIGURE 2-3: *LVCMOS Outputs.*

TABLE 2-2: DSC557-04 VQFN-20 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	OE1	I	Output enable, active-high. Controls CLK0.
2	NC	N/A	Leave unconnected or grounded.
3	VSS	P	Ground.
4	VSS	P	Ground.
5	CLK0–	O	Complement output of differential pair.
6	CLK0+	O	True output of differential pair.
7	CLK1–	O	Complement output of differential pair.
8	CLK1+	O	True output of differential pair.
9	VDD	P	Power supply.
10	NC	N/A	Leave unconnected or grounded.
11	OE2	I	Output enable, active-high. Controls CLK1 and CLK2.
12	NC	N/A	Leave unconnected or grounded.
13	VSS	P	Ground.
14	VSS	P	Ground.
15	CLK2–	O	Complement output of differential pair.
16	CLK2+	O	True output of differential pair.
17	NC	N/A	Leave unconnected or grounded.
18	NC	N/A	Leave unconnected or grounded.
19	VDD	P	Power supply.
20	NC	N/A	Leave unconnected or grounded.

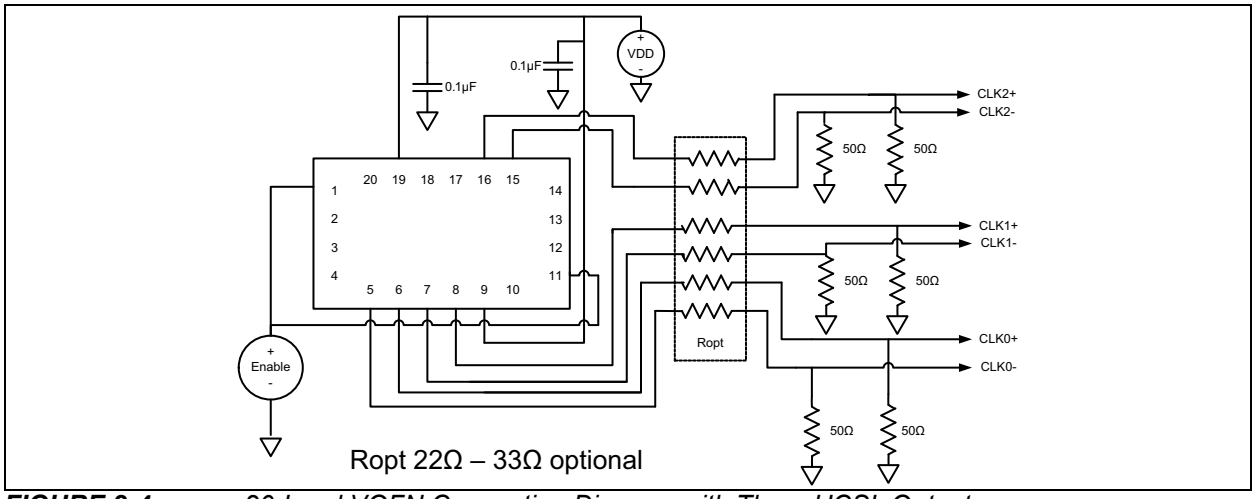


FIGURE 2-4: *20-Lead VQFN Connection Diagram with Three HCSL Outputs.*

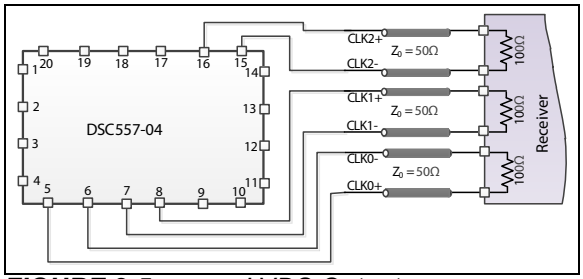


FIGURE 2-5: *LVDS Outputs.*

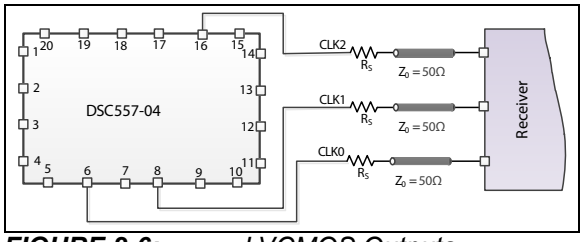


FIGURE 2-6: *LVCMOS Outputs.*

TABLE 2-3: DSC557-05 VQFN-20 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	OE1	I	Output enable, active-high. Controls CLK0 and CLK3.
2	NC	N/A	Leave unconnected or grounded.
3	VSS	P	Ground.
4	VSS	P	Ground.
5	CLK0–	O	Complement output of differential pair.
6	CLK0+	O	True output of differential pair.
7	CLK1–	O	Complement output of differential pair.
8	CLK1+	O	True output of differential pair.
9	VDD	P	Power supply.
10	NC	N/A	Leave unconnected or grounded.
11	OE2	I	Output enable, active-high. Controls CLK1 and CLK2.
12	NC	N/A	Leave unconnected or grounded.
13	VSS	P	Ground.
14	VSS	P	Ground.
15	CLK2–	O	Complement output of differential pair.
16	CLK2+	O	True output of differential pair.
17	CLK3–	O	Complement output of differential pair.
18	CLK3+	O	True output of differential pair.
19	VDD	P	Power supply.
20	NC	N/A	Leave unconnected or grounded.

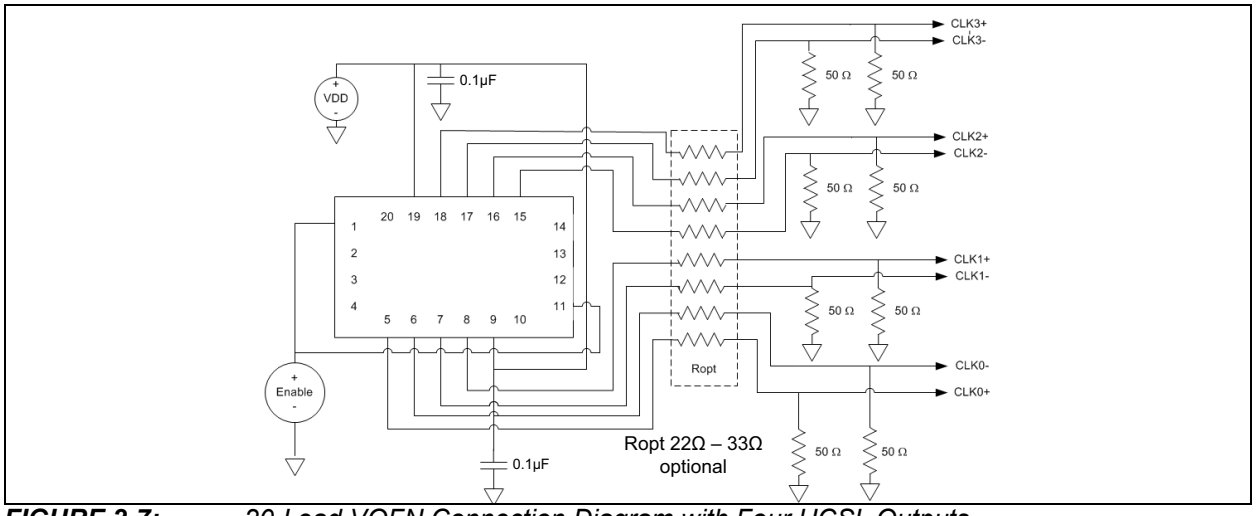


FIGURE 2-7: *20-Lead VQFN Connection Diagram with Four HCSL Outputs.*

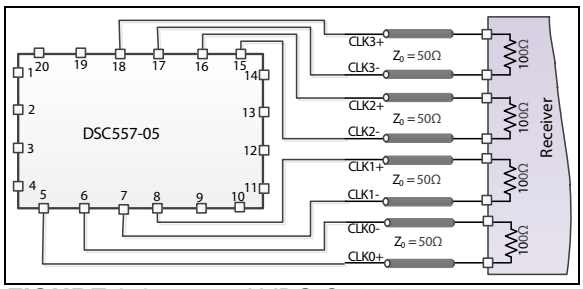


FIGURE 2-8: *LVDS Outputs.*

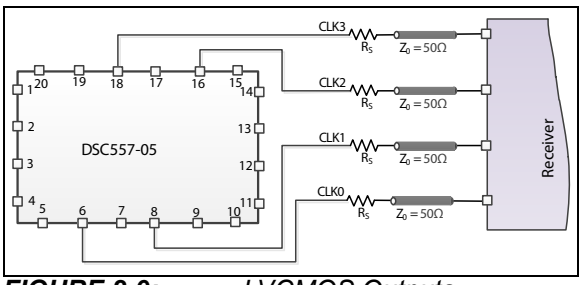


FIGURE 2-9: *LVCMOS Outputs.*

3.0 OUTPUT WAVEFORM

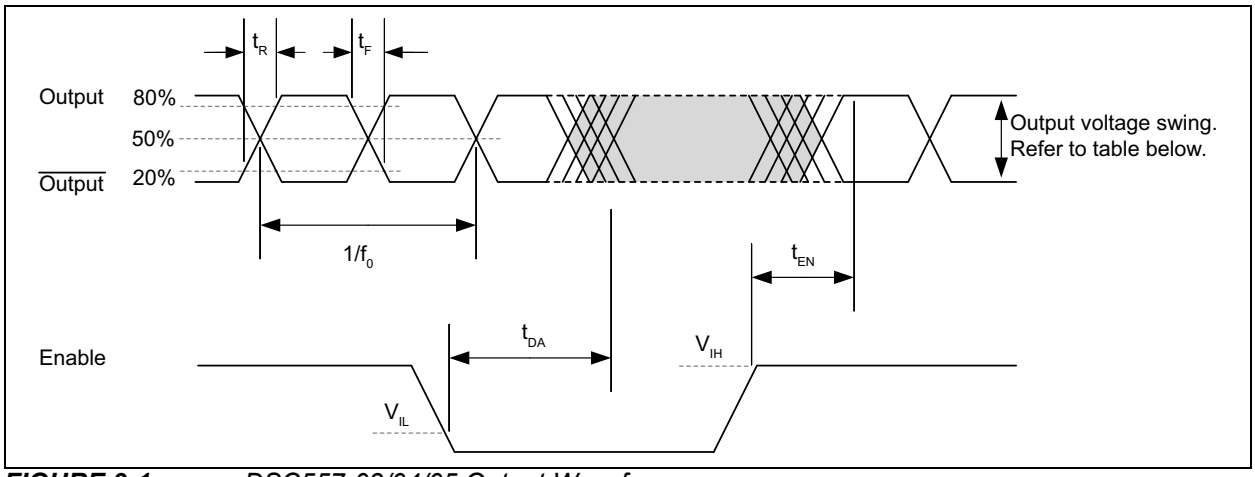


FIGURE 3-1: *DSC557-03/04/05 Output Waveform.*

TABLE 3-1: OUTPUT VOLTAGE SWING

Specification	V_{CM}	V_{SWING_SE} (typ.)
LVDS	1.2V	350 mV
HCSL	350 mV	675 mV

4.0 SOLDER REFLOW PROFILE

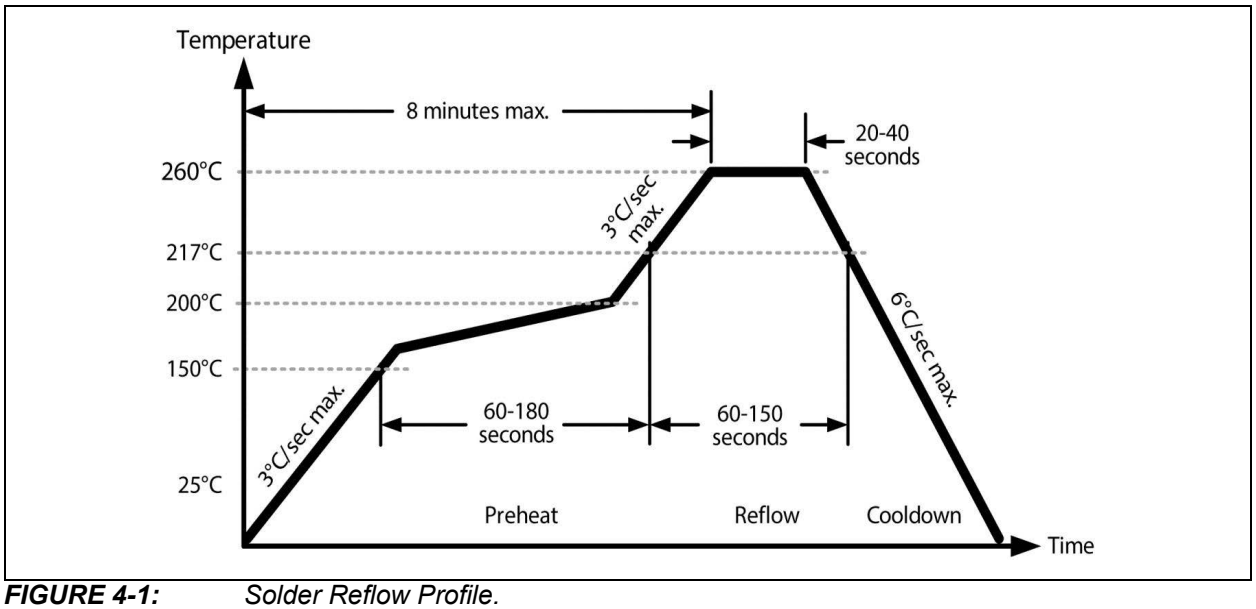


FIGURE 4-1: *Solder Reflow Profile.*

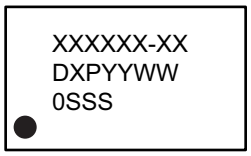
TABLE 4-1: SOLDER REFLOW

VQFN-14/VQFN-20 MSL 1 @ 260°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

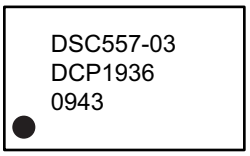
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

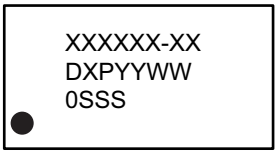
14-Lead VQFN*



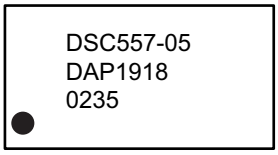
Example



20-Lead VQFN*



Example



Legend:	XX...X	Product code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

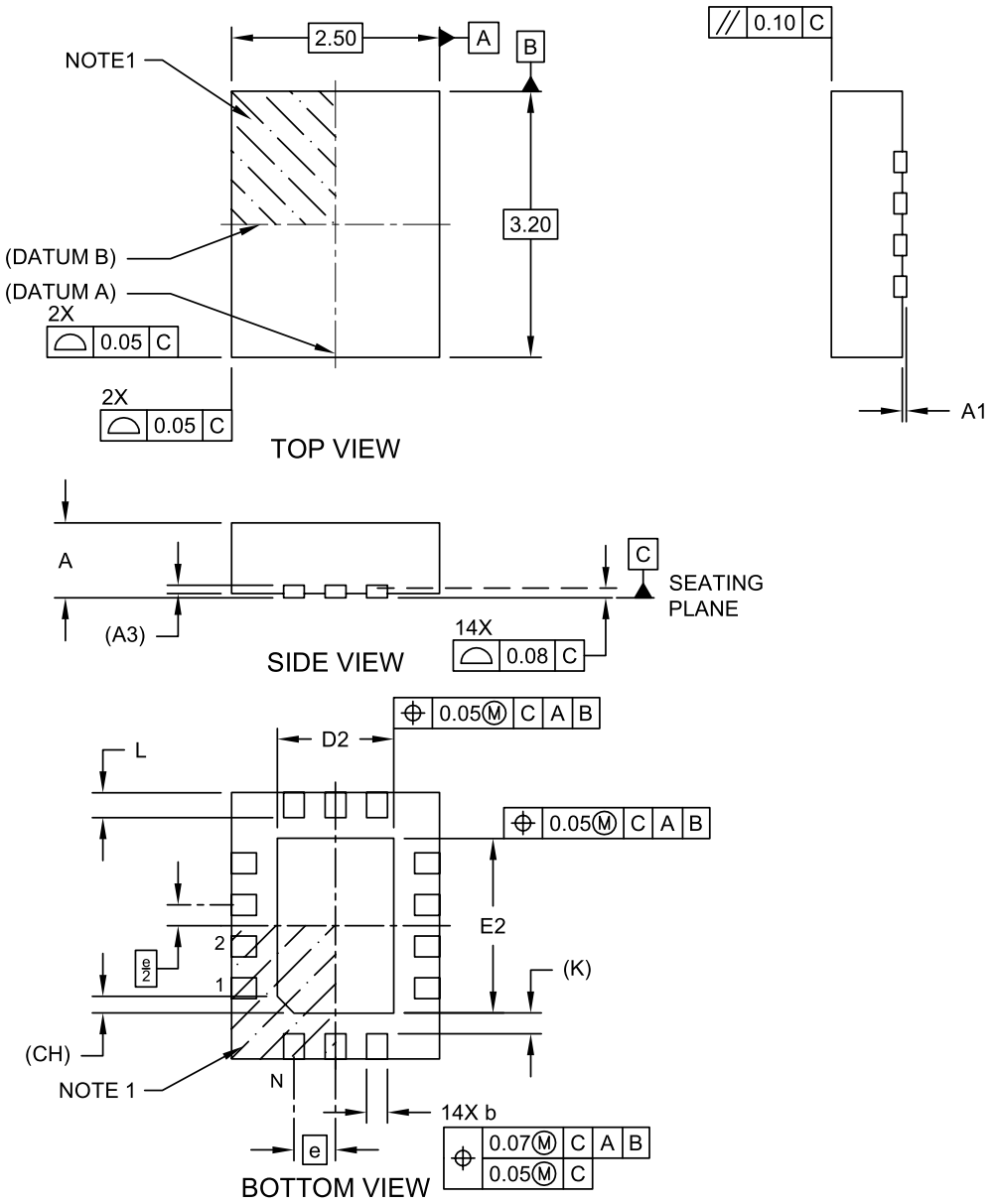
Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: DSC557 parts may ship with “DSA” on the package marking until such time as stock is depleted and the updated “DSC” marking appears. Regardless of those three characters, the part is the same.

14-Lead VQFN 2.5 mm x 3.2 mm Package Outline and Recommended Land Pattern

14-Lead Very Thin Plastic Quad Flat, No Lead Package (MUA) - 2.5x3.2x0.9 mm Body [VQFN] With 1.4x2.1 mm Exposed Pad; Micrel Legacy Package

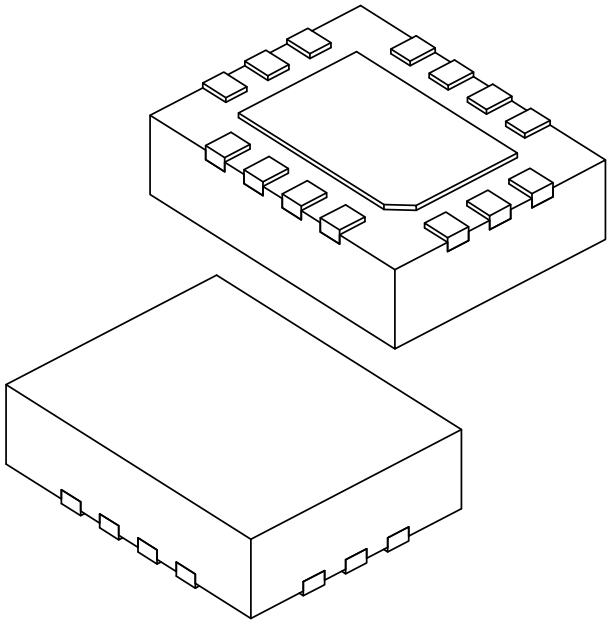
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1098 Rev A Sheet 1 of 2

14-Lead Very Thin Plastic Quad Flat, No Lead Package (MUA) - 2.5x3.2x0.9 mm Body [VQFN] With 1.4x2.1 mm Exposed Pad; Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.10 REF	
Overall Length	D		2.50 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Overall Width	E		3.20 BSC	
Exposed Pad Width	E2	2.05	2.10	2.15
Exposed Pad Index Chamfer	CH		0.20 REF	
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.30	0.35
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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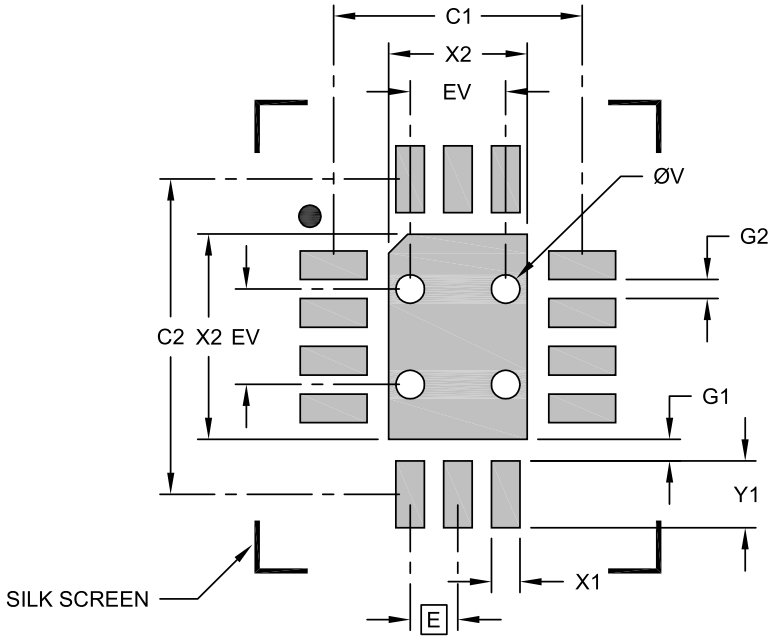
14-Lead Very Thin Plastic Quad Flat, No Lead Package (MUA) - 2.5x3.2x0.9 mm Body [VQFN] With 1.4x2.1 mm Exposed Pad; Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.45
Center Pad Length	Y2			2.15
Contact Pad Spacing	C1		2.60	
Contact Pad Spacing	C2		3.30	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.70
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

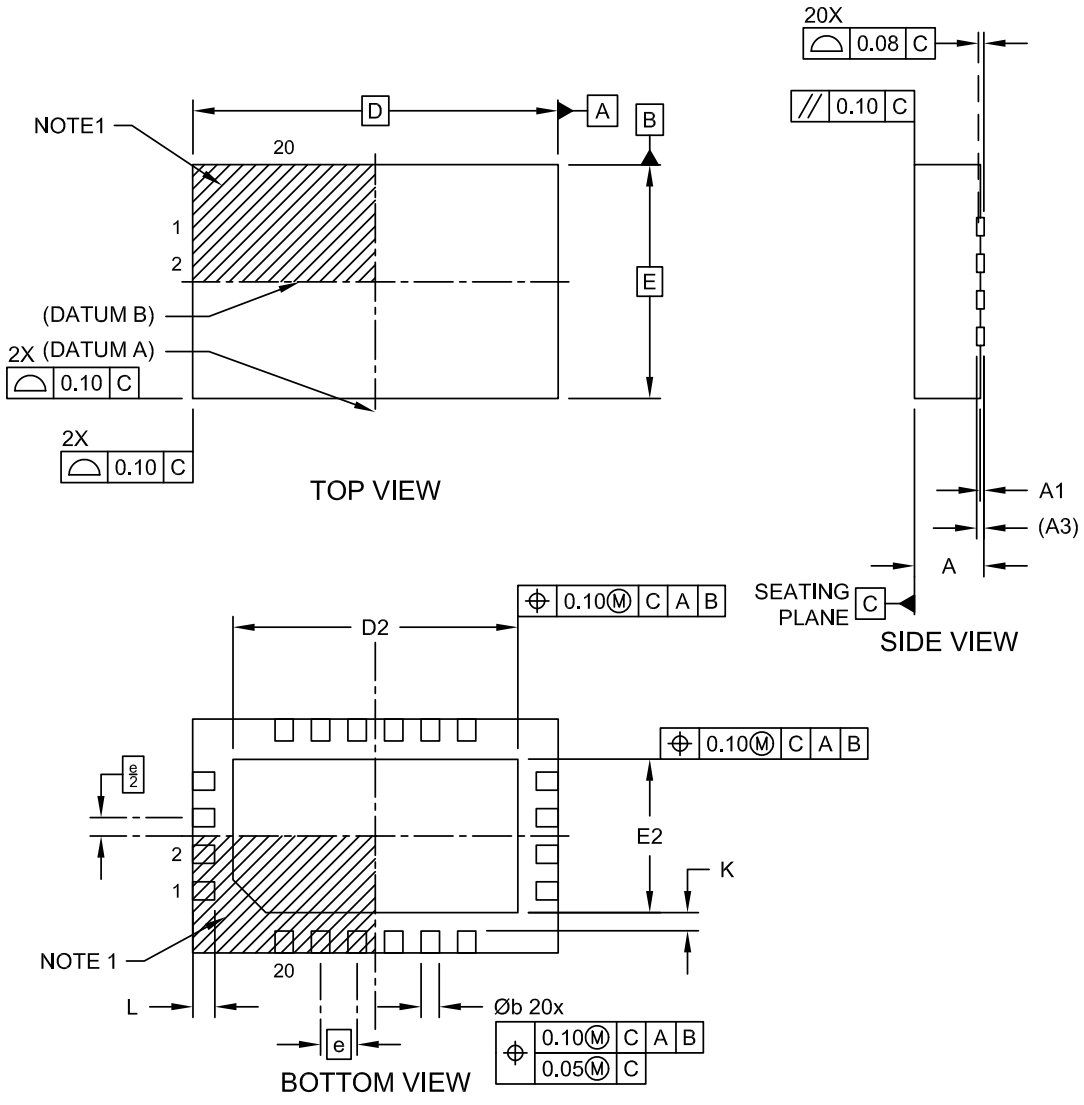
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3098 Rev A

20-Lead VQFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

20-Lead Very Thin Plastic Quad Flat, No Lead Package (P9A) - 5.0x3.2x0.9 mm Body [VQFN] With 3.9x2.1 Exposed Pad

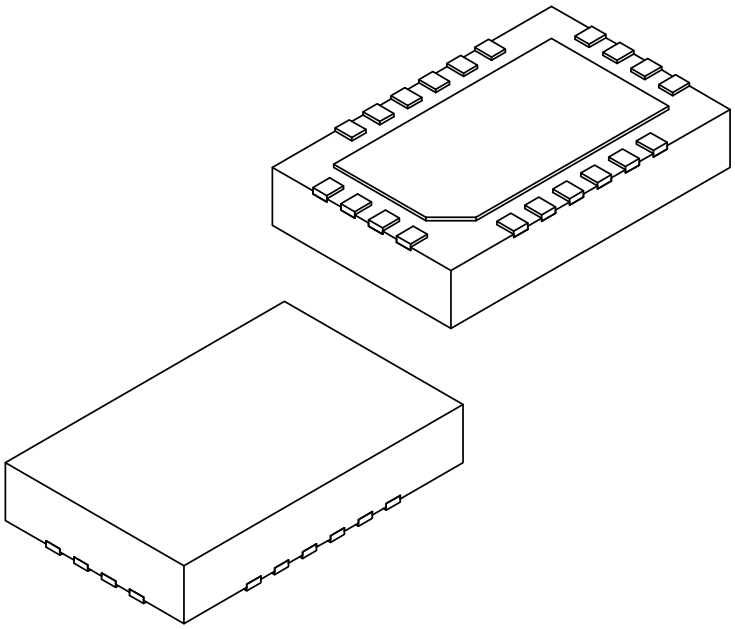
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1117 Rev A Sheet 1 of 2

20-Lead Very Thin Plastic Quad Flat, No Lead Package (P9A) - 5.0x3.2x0.9 mm Body [VQFN] With 3.9x2.1 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.80	3.90	4.00
Overall Width	E		3.20 BSC	
Exposed Pad Width	E2	2.00	2.10	2.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.20	0.30	0.40
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

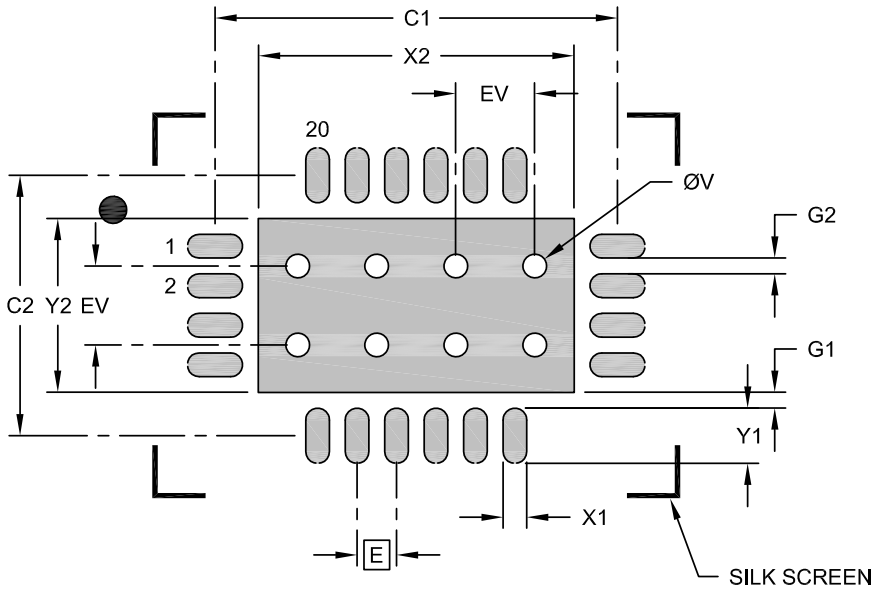
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1117 Rev A Sheet 2 of 2

20-Lead Very Thin Plastic Quad Flat, No Lead Package (P9A) - 5.0x3.2x0.9 mm Body [VQFN] With 3.9x2.1 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			4.00
Optional Center Pad Length	Y2			2.20
Contact Pad Spacing	C1		5.10	
Contact Pad Spacing	C2		3.30	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.70
Contact Pad to Center Pad (X20)	G1	0.20		
Contact Pad to Contact Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3117 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2022)

- Initial release of DSC557-03/04/05 as Microchip data sheet DS20006691A. This data sheet combines DSC557-03, DSC557-04, and DSC557-05 into a single data sheet.

Revision B (March 2023)

- Added a note to **Section 5.1 "Package Marking Information"** indicating some parts may be shipped with DSA on the package marking until that stock is depleted and the updated DSC package marking begins.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	XXXX	X	X	X	X
Device	Output Format	Package	Temp. Range	Stability	Packing Option

Device:
- DSC557-03: Two Output PCIe Clock Generator for Automotive
- DSC557-04: Three Output PCIe Clock Generator for Automotive
- DSC557-05: Four Output PCIe Clock Generator for Automotive

Output Format: (Note 1)
- 1 = LVCMOS
- 3 = LVDS
- 4 = HCSL

Package:
- F = 14-Lead VQFN (DSC557-03 Only)
- K = 20-Lead VQFN (DSC557-04/05 Only)

Temperature Range:
- L = –40°C to +105°C (Ext. Industrial)
- I = –40°C to +85°C (Industrial)
- E = –20°C to +70°C (Commercial)

Stability:
- 0 = ±100 ppm
- 1 = ±50 ppm

Packing Option:
- <blank>= 72/Tube (DSC557-04/05)
- <blank>= 110/Tube (DSC557-03)
- T = 1000/Reel (All Package Options)

Note 1: The Output Format's arrangement is CLK3 to CLK0 (left-to-right) and may only have as many digits as that particular part allows. For example, DSC557-03 has two outputs; the part number example can only have two digits in that location. DSC557-04 can only have three and DSC557-05 can only have four.

Examples:

a) DSC557-0344FL0:
Two HCSL Outputs PCIe Clock Generator, 14-Lead VQFN, –40°C to +105°C Temperature Range, ±100 ppm Stability, 110/Tube

b) DSC557-04111KI1T:
Three LVCMOS Outputs PCIe Clock Generator, 20-Lead VQFN, –40°C to +85°C Temperature Range, ±50 ppm Stability, 1000/Reel

c) DSC557-053344KE0:
Four Output PCIe Clock Generator, (CLK3/CLK2: LVDS, CLK1/CLK0: HCSL), 20-Lead VQFN, –20°C to +70°C Temperature Range, ±100 ppm Stability, 96/Tube

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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