

# E3M0021120J2

Silicon Carbide Power MOSFET  
E-Series Automotive  
N-Channel Enhancement Mode



## Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 4.7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

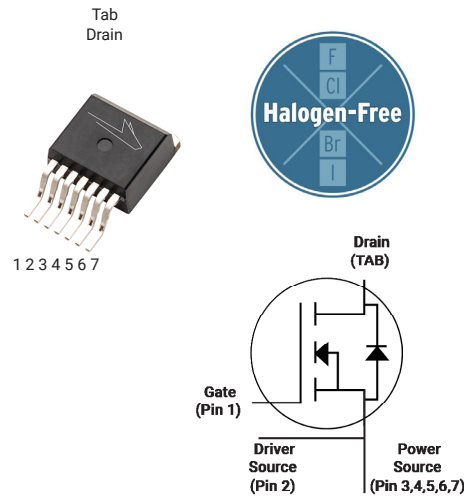
## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Typical Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

## Package



Part Number	Package	Marking
E3M0021120J2	TO-263-7XL	E3M0021120J2

## Maximum Ratings ( $T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Note
$V_{DSmax}$	Drain - Source Voltage	1200	V	
$V_{GSmax}$	Gate - Source Voltage	-8/+19	V	Note: 1
$I_D$	Continuous Drain Current, $V_{GS} = 15\text{ V}$	$T_c = 25^\circ\text{C}$	114	A Fig. 19 Note: 2
		$T_c = 100^\circ\text{C}$	83	
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width $t_p$ limited by $T_{jmax}$	248	A	Fig. 22
$P_D$	Power Dissipation, $T_c=25^\circ\text{C}$ , $T_j = 175^\circ\text{C}$	500	W	Fig. 20 Note: 2
$T_j, T_{stg}$	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$	
$T_L$	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$	

Note (1): Recommended turn off / turn on gate voltage  $V_{GS} = -4V...0V / +15V$

Note (2): Verified by design


**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.9	3.8	V	$V_{DS} = V_{GS}, I_D = 17.10\text{ mA}$	Fig. 11
			2.3		V	$V_{DS} = V_{GS}, I_D = 17.10\text{ mA}, T_J = 175^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current		1	50	$\mu\text{A}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
$I_{GSS}$	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		21	29	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 62.12\text{ A}$	Fig. 4, 5, 6
			35			$V_{GS} = 15\text{ V}, I_D = 62.12\text{ A}, T_J = 175^\circ\text{C}$	
$g_{fs}$	Transconductance		38		S	$V_{DS} = 20\text{ V}, I_{DS} = 62.12\text{ A}$	Fig. 7
			35			$V_{DS} = 20\text{ V}, I_{DS} = 62.12\text{ A}, T_J = 175^\circ\text{C}$	
$C_{iss}$	Input Capacitance		5100		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to }1000\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
$C_{oss}$	Output Capacitance		174				
$C_{rss}$	Reverse Transfer Capacitance		11				
$E_{oss}$	$C_{oss}$ Stored Energy		98		$\mu\text{J}$	$V_{DS} = 800\text{ V}, f = 100\text{ kHz}$	Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		210		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }800\text{ V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		323		pF		
$E_{ON}$	Turn-On Switching Energy (Body Diode FWD)		1.7		mJ	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 62.12\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 59\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26, 28
$E_{OFF}$	Turn-Off Switching Energy (Body Diode FWD)		0.3				
$t_{d(on)}$	Turn-On Delay Time		15		ns	$V_{DD} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 62.12\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 59\text{ }\mu\text{H}, T_J = 25^\circ\text{C}$ Timing relative to $V_{DS}$ Inductive load	Fig. 27, 28
$t_r$	Rise Time		34				
$t_{d(off)}$	Turn-Off Delay Time		54				
$t_f$	Fall Time		13				
$R_{G(int)}$	Internal Gate Resistance		2.9		$\Omega$	$f = 1\text{ MHz}$	
$Q_{gs}$	Gate to Source Charge		60		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 62.12\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
$Q_{gd}$	Gate to Drain Charge		45				
$Q_g$	Total Gate Charge		169				

Note (3):  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V

$C_{o(tr)}$ , a lumped capacitance that gives same charging time as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V


**Reverse Diode Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$V_{SD}$	Diode Forward Voltage	4.9		V	$V_{GS} = -4\text{ V}, I_{SD} = 31.1\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.4		V	$V_{GS} = -4\text{ V}, I_{SD} = 31.1\text{ A}, T_J = 175^\circ\text{C}$	
$I_S$	Continuous Diode Forward Current		85	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
$I_{S, \text{pulse}}$	Diode pulse Current		248	A	$V_{GS} = -4\text{ V}$ , pulse width $t_p$ limited by $T_{J\text{max}}$	
$t_{rr}$	Reverse Recover time	16		ns	$V_{GS} = -4\text{ V}, I_{SD} = 62.12\text{ A}, V_R = 800\text{ V}$ $di_F/dt = 5300\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	416		nC		
$I_{rrm}$	Peak Reverse Recovery Current	44		A		
$t_{rr}$	Reverse Recover time	22		ns	$V_{GS} = -4\text{ V}, I_{SD} = 62.12\text{ A}, V_R = 800\text{ V}$ $di_F/dt = 2240\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	268		nC		
$I_{rrm}$	Peak Reverse Recovery Current	21		A		

**Thermal Characteristics**

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.23	0.30	$^\circ\text{C}/\text{W}$		Fig. 21



## Typical Performance

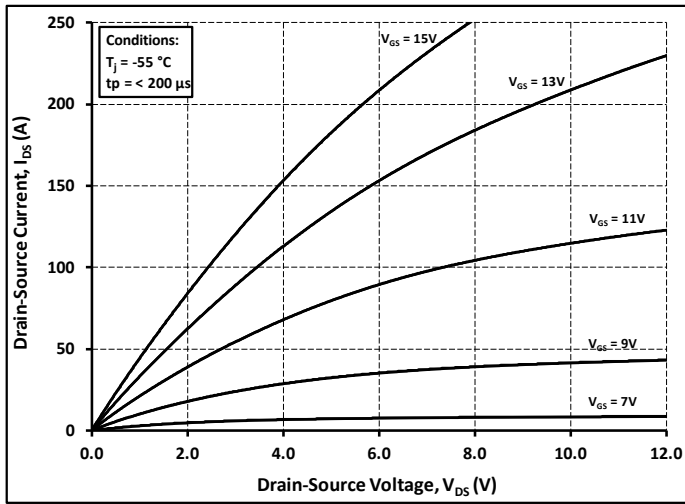


Figure 1. Output Characteristics  $T_J = -55\text{ }^{\circ}\text{C}$

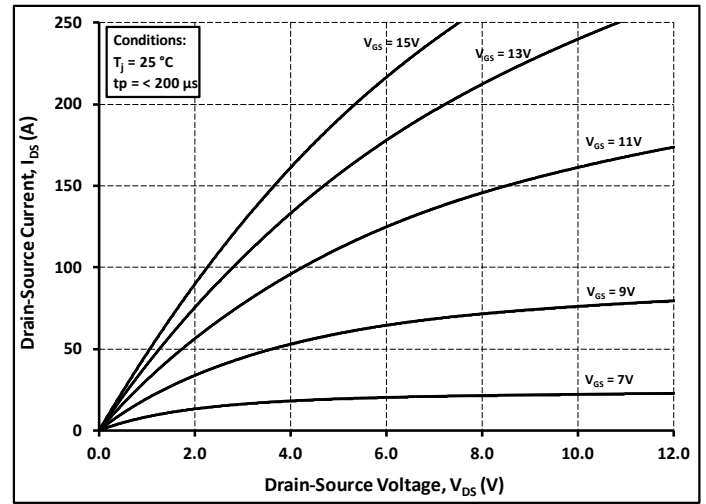


Figure 2. Output Characteristics  $T_J = 25\text{ }^{\circ}\text{C}$

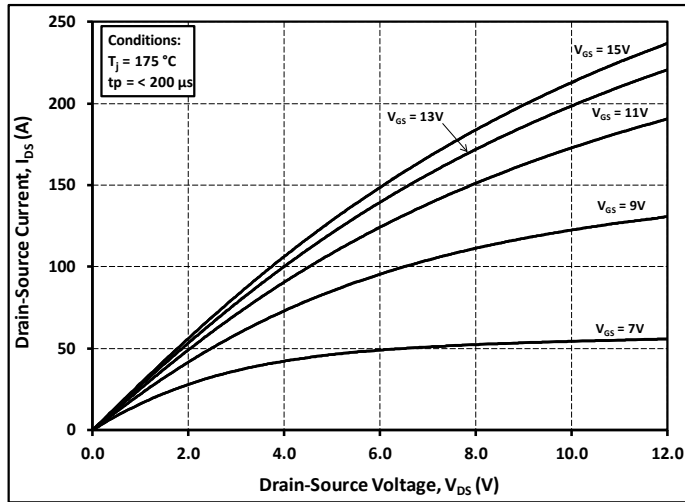


Figure 3. Output Characteristics  $T_J = 175\text{ }^{\circ}\text{C}$

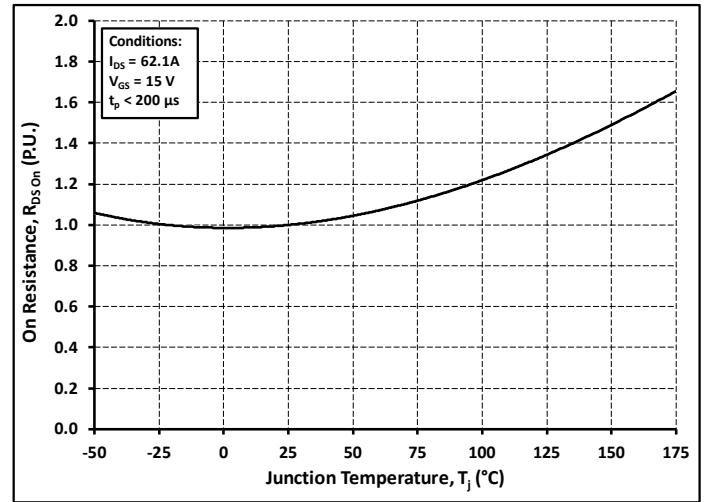


Figure 4. Normalized On-Resistance vs. Temperature

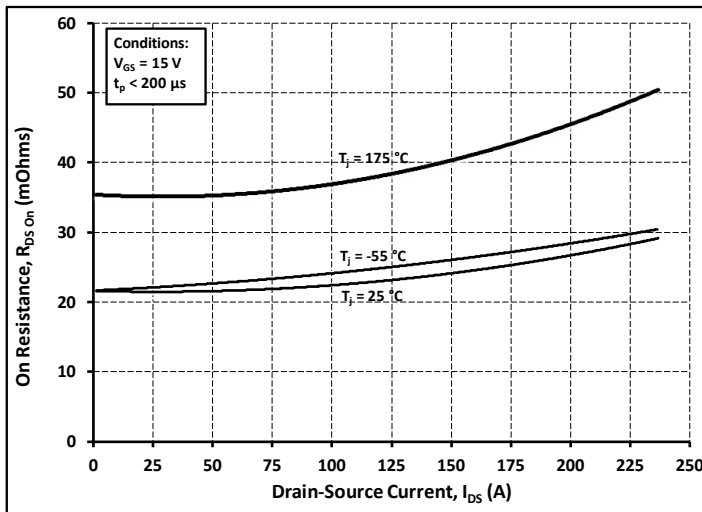


Figure 5. On-Resistance vs. Drain Current  
For Various Temperatures

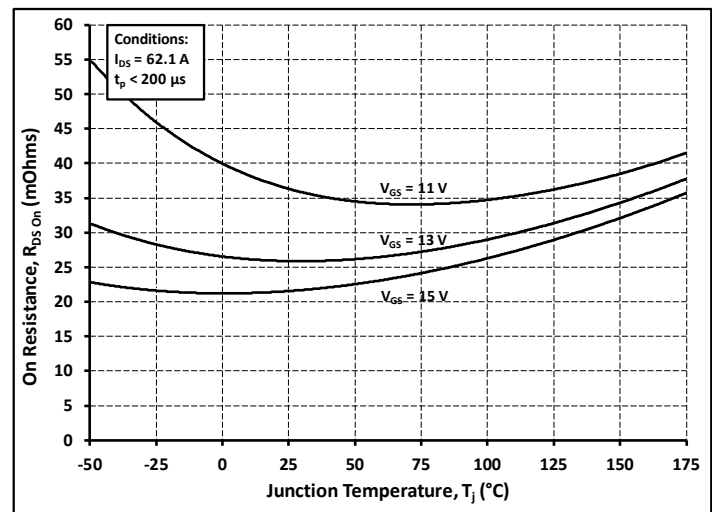


Figure 6. On-Resistance vs. Temperature  
For Various Gate Voltage

## Typical Performance

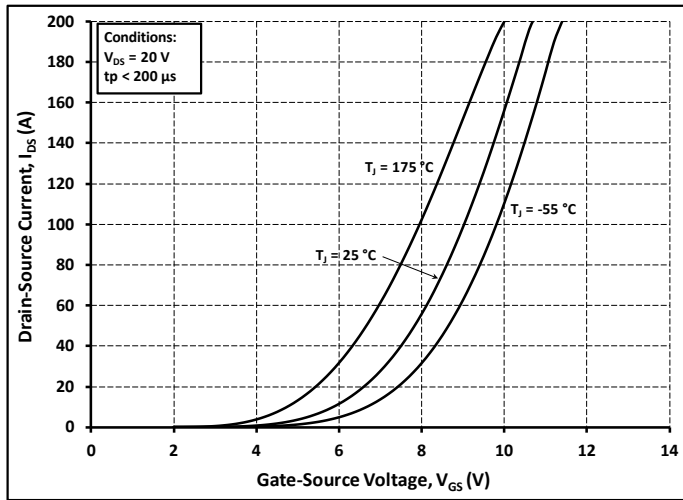


Figure 7. Transfer Characteristic for Various Junction Temperatures

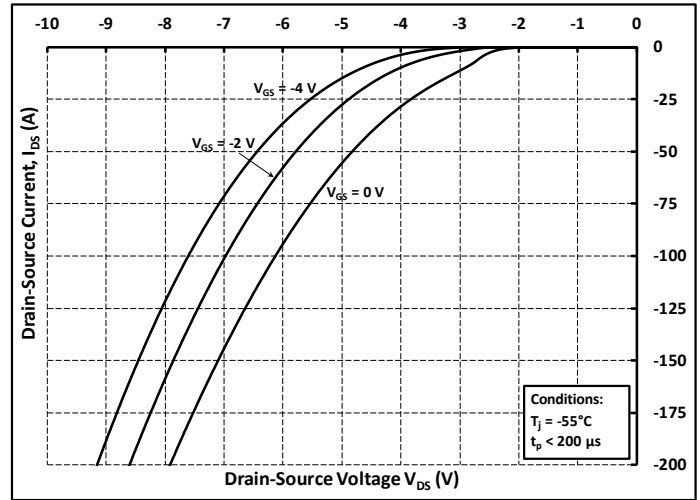


Figure 8. Body Diode Characteristic at  $-55^\circ\text{C}$

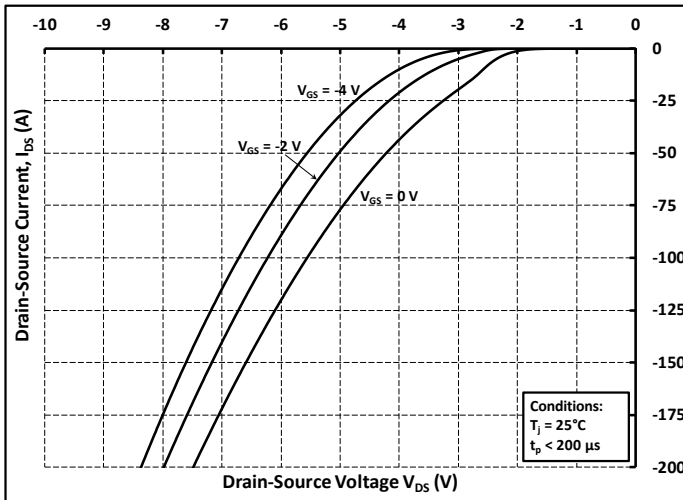


Figure 9. Body Diode Characteristic at  $25^\circ\text{C}$

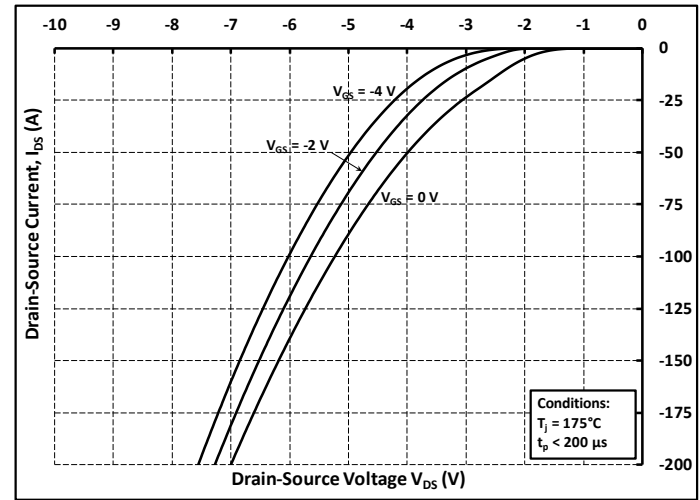


Figure 10. Body Diode Characteristic at  $175^\circ\text{C}$

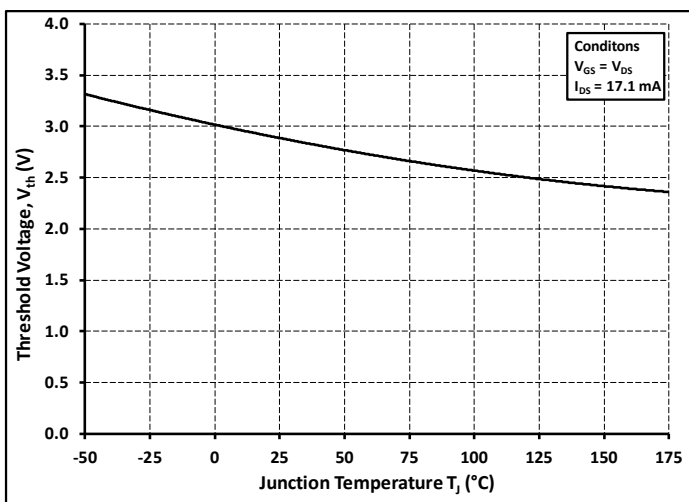


Figure 11. Threshold Voltage vs. Temperature

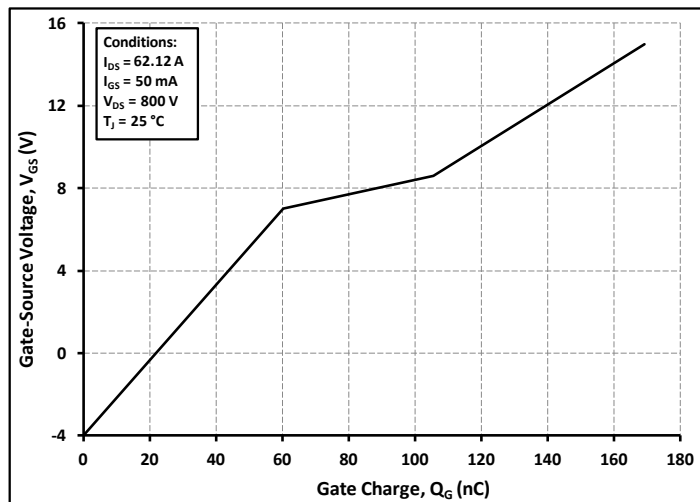


Figure 12. Gate Charge Characteristics

## Typical Performance

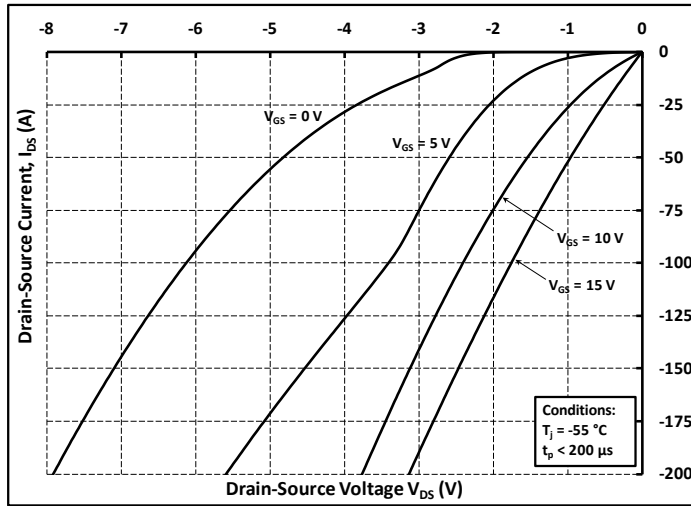


Figure 13. 3rd Quadrant Characteristic at -55 °C

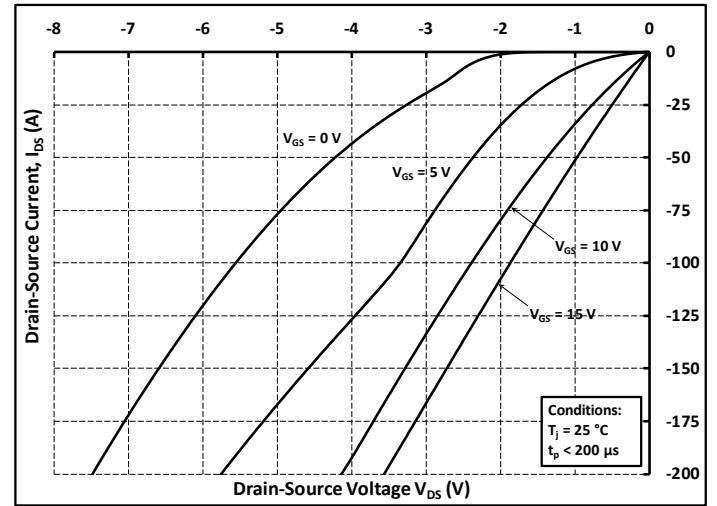


Figure 14. 3rd Quadrant Characteristic at 25 °C

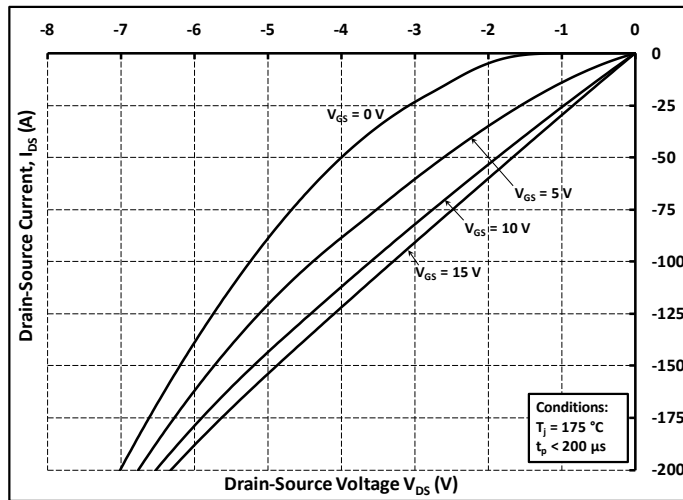


Figure 15. 3rd Quadrant Characteristic at 175 °C

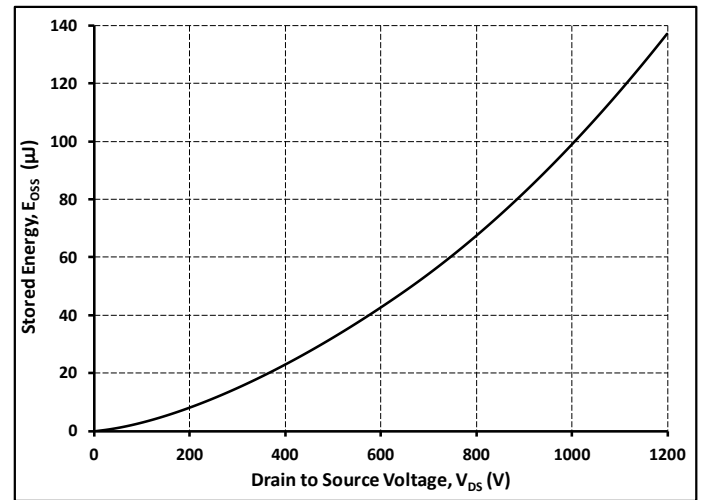


Figure 16. Output Capacitor Stored Energy

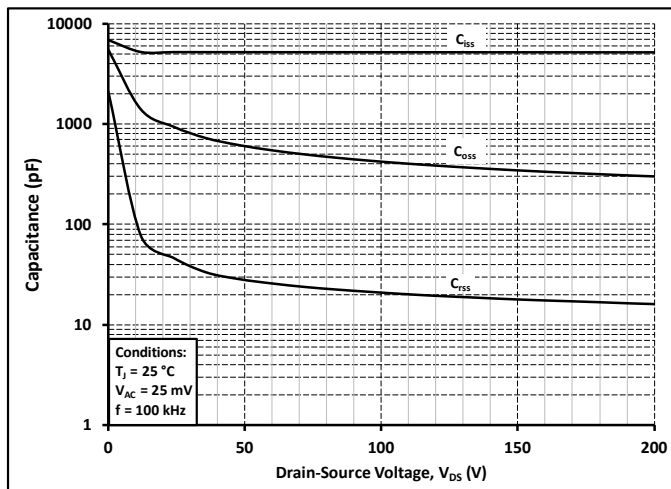


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

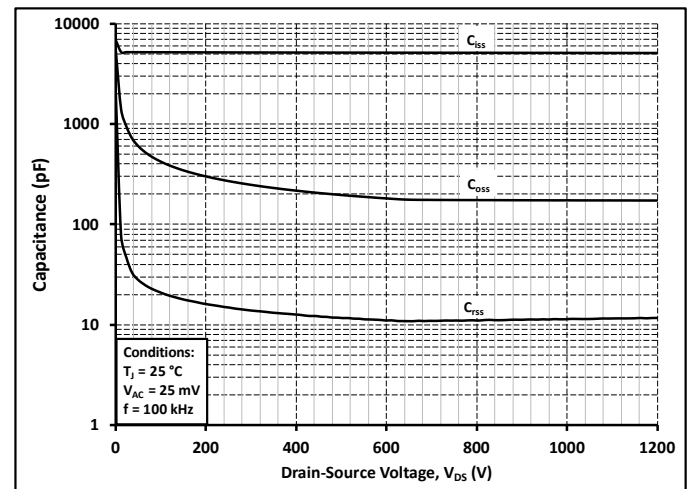


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

## Typical Performance

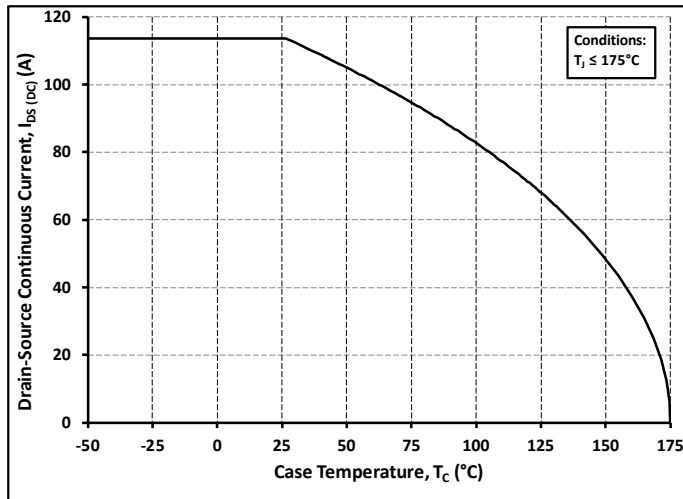


Figure 19. Continuous Drain Current Derating vs. Case Temperature

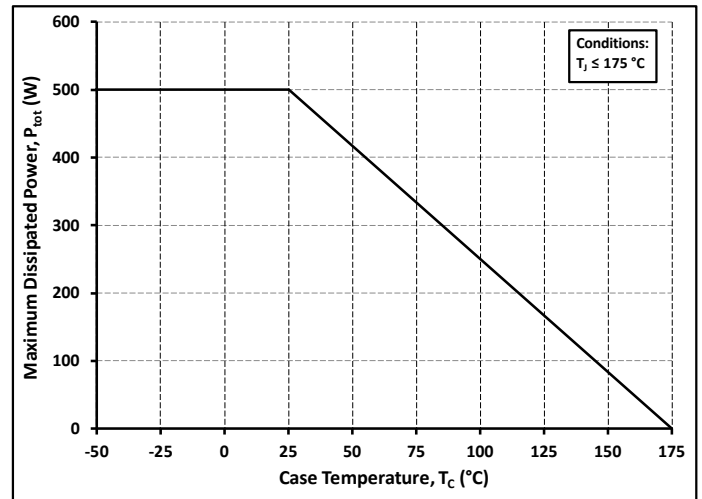


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

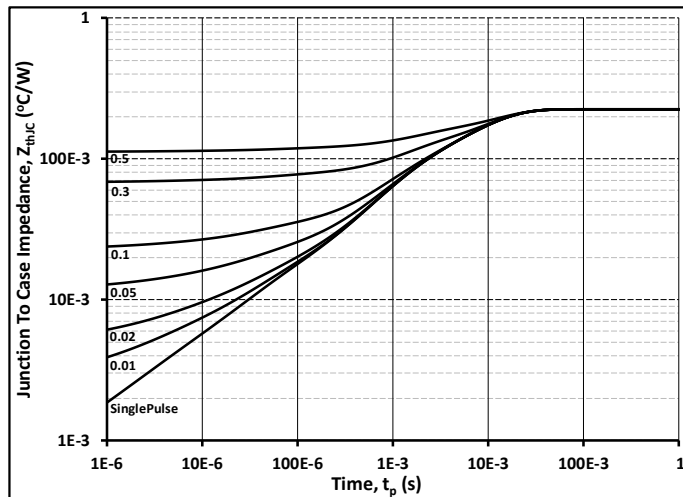


Figure 21. Transient Thermal Impedance (Junction - Case)

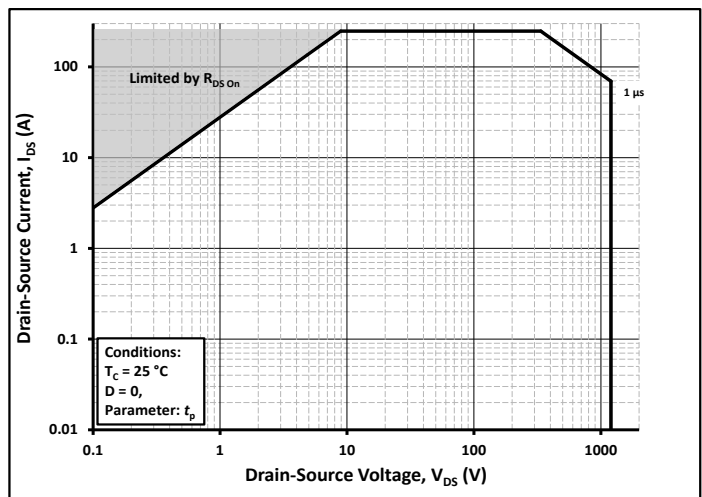
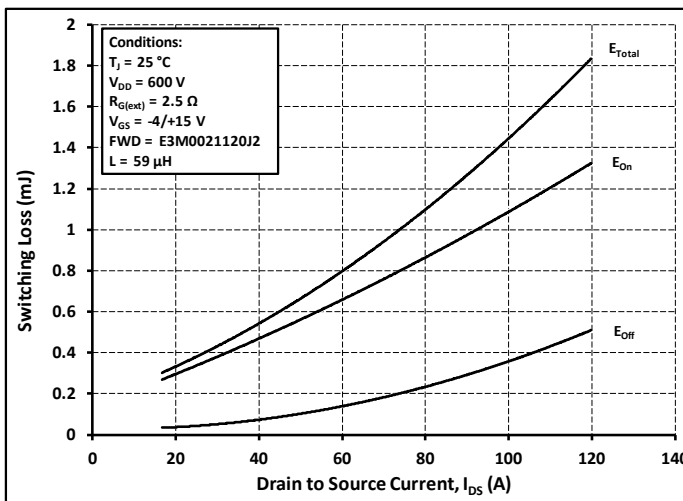
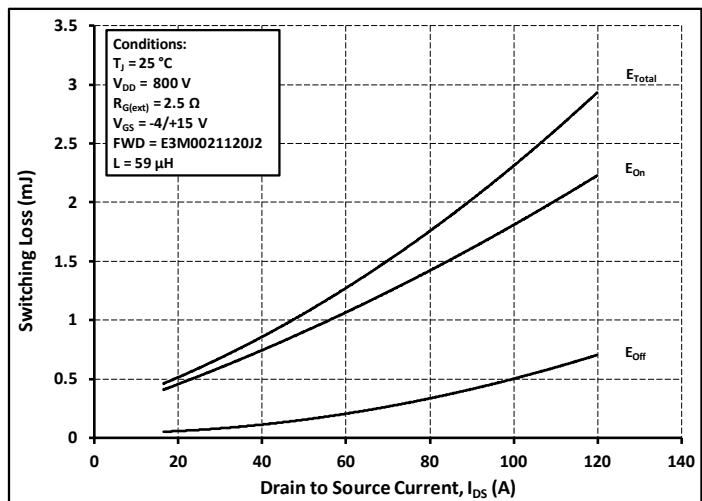


Figure 22. Safe Operating Area

Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600V$ )Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800V$ )

## Typical Performance

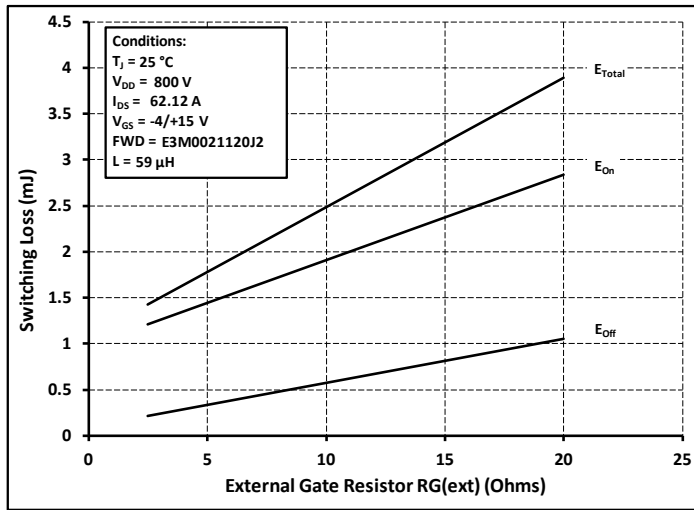


Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

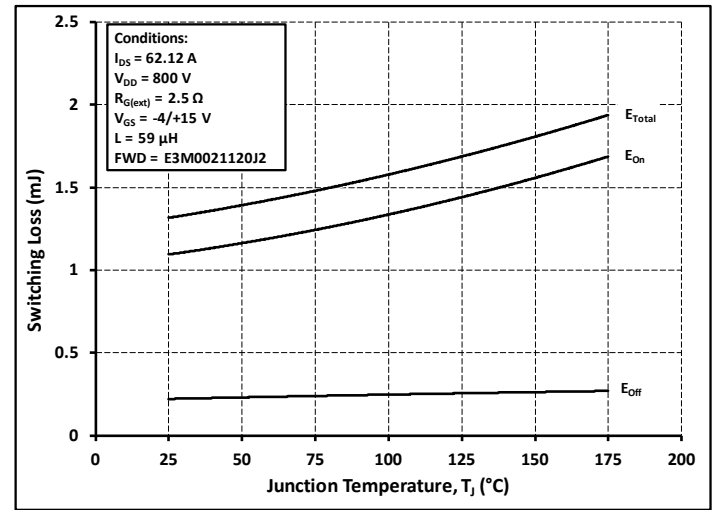


Figure 26. Clamped Inductive Switching Energy vs. Temperature

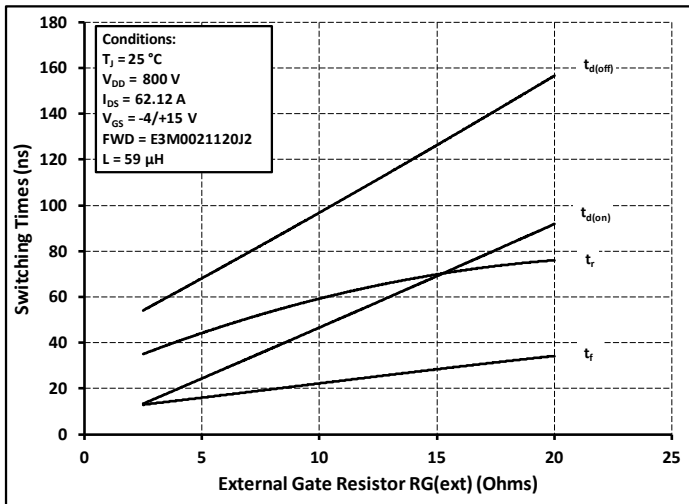


Figure 27. Switching Times vs.  $R_{G(ext)}$

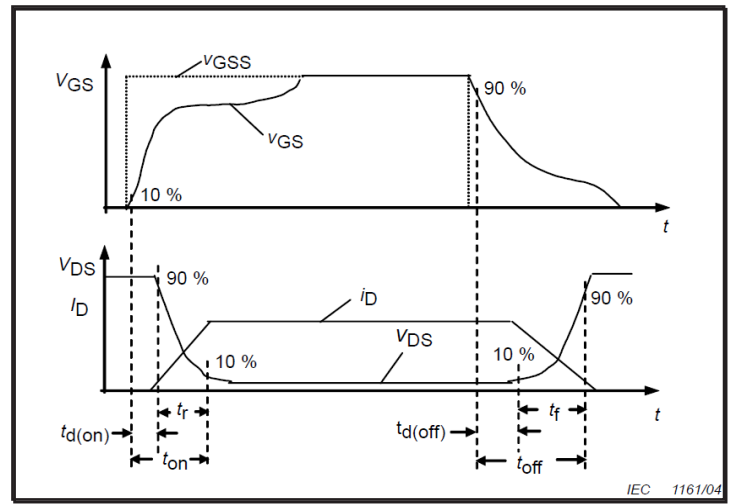


Figure 28. Switching Times Definition

## Test Circuit Schematic

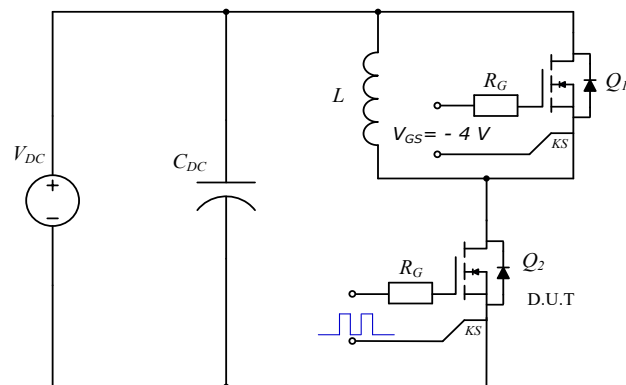
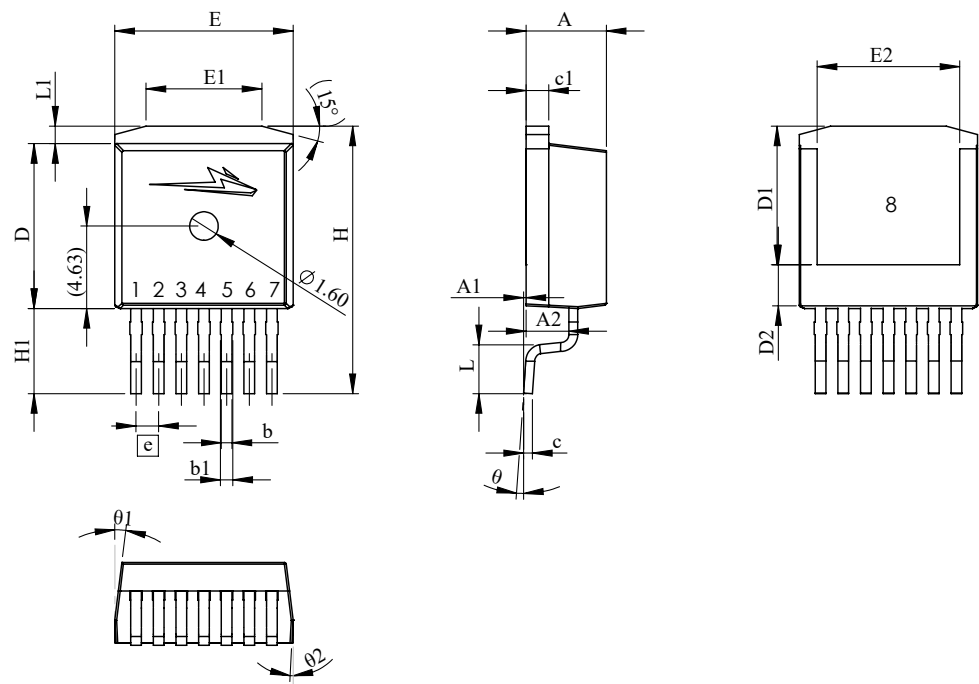


Figure 29. Clamped Inductive Switching Waveform Test Circuit



Package Dimensions



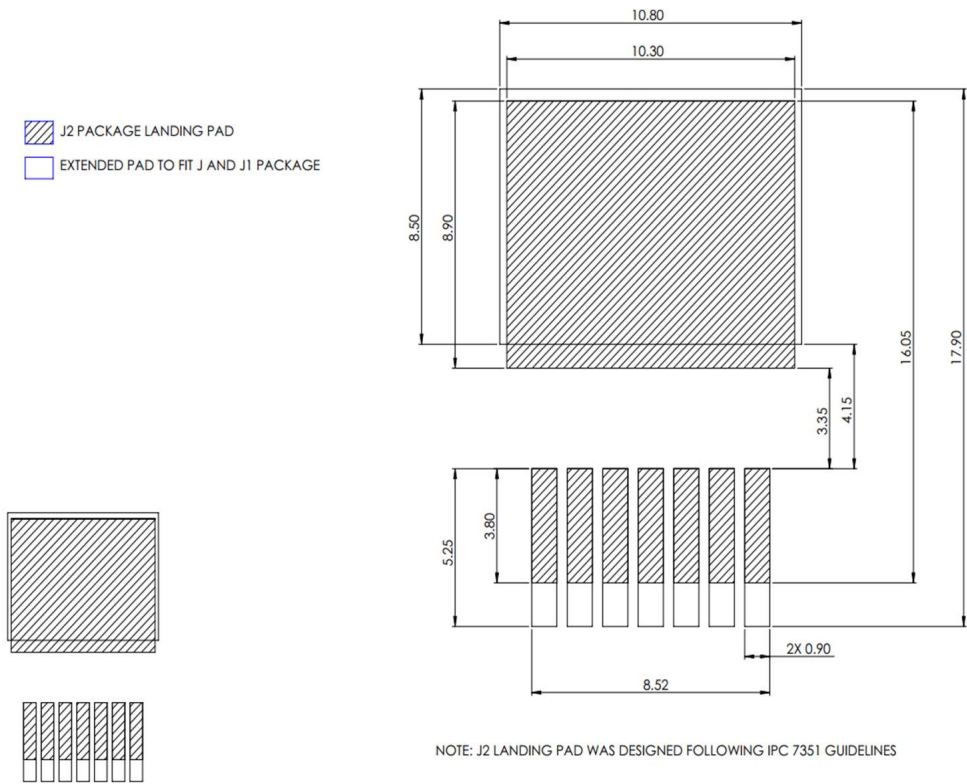
SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.70
A1	0.00	0.25
A2	2.20	2.60
b	0.52	0.72
b1	0.60	0.80
c	0.42	0.62
c1	1.07	1.47
D	9.05	9.45
D1	7.58	7.98
D2	2.05	2.45
E	9.80	10.20
E1	6.30	6.97
E2	7.80	8.20
e	1.27 BSC	
H	14.87	15.27
H1	4.55	4.95
L	2.48	2.88
L1	0.87	1.27
θ	0°	8°
θ1	4°	10°
θ2	0°	6°

1	GATE
2	KELVIN
3	SOURCE
4	
5	
6	
7	DRAIN
8	

- NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
  2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
  3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
  4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Recommended Solder Pad Layout

All dimensions in mm





Revision history

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Document Version	Date of release	Descriptiion of changes
1.0	December 2023	Initial release
2	December- 2023	Operating Temp Corrected
3	January - 2025	Legal Disclaimer Updated
4	July - 2025	$V_{AC}$ removed from $R_{G(int)}$ test condition Fig 22 updated



## Notes & Disclaimer

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