MCP1799

80 mA High-Voltage Automotive LDO

Features

- AEC-Q100 with Grade 0 and PPAP Capable
- Wide Input Voltage Range: 4.5V to 45V
  - Undervoltage Lockout (UVLO): 2.8V typical
- Extended Working Temperature Range: -40°C to +150°C
- Standard Output Regulated Voltages (V_R): 3.3V and 5.0V
  - Tolerance ±2%
- Low Quiescent Supply Current: 25 µA typical
- Output Current Capability: 80 mA typical
- Stable with 1 µF Ceramic Output Capacitor
- Short Circuit Protection
- Thermal Shutdown Protection:
  - +180°C typical
  - Hysteresis: 22°C typical
- High Power Supply Rejection Ratio (PSRR):
  - 70 dB @ 1 kHz typical
- Available in the Following Packages:
  - 3-Lead SOT-23
  - 3-Lead SOT-223

Applications

- Automotive Electronics
- Microcontroller Biasing
- Cordless Power Tools, Home Appliances E-bikes, Drones, etc.
- Smoke Detectors and other Alarm Sensors

General Description

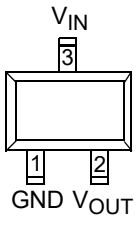
The MCP1799 is a high-voltage, Low-Dropout (LDO) regulator, capable of generating 80 mA output current. The input voltage range of 4.5V to 45V makes it ideal in 12V to 36V power rails and in high-voltage battery packs.

The MCP1799 comes in two standard fixed output-voltage versions: 3.3V and 5.0V. The regulator output is stable with 1 µF ceramic capacitors. The device is protected from short circuit events by the current limit function and from over heating by means of thermal shutdown protection.

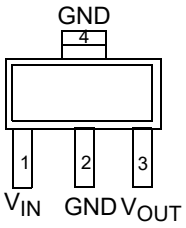
The device itself has a low ground current of 45 µA typical, while delivering maximum output current of 80 mA. Without load the device consumes 25 µA typical.

Package Types

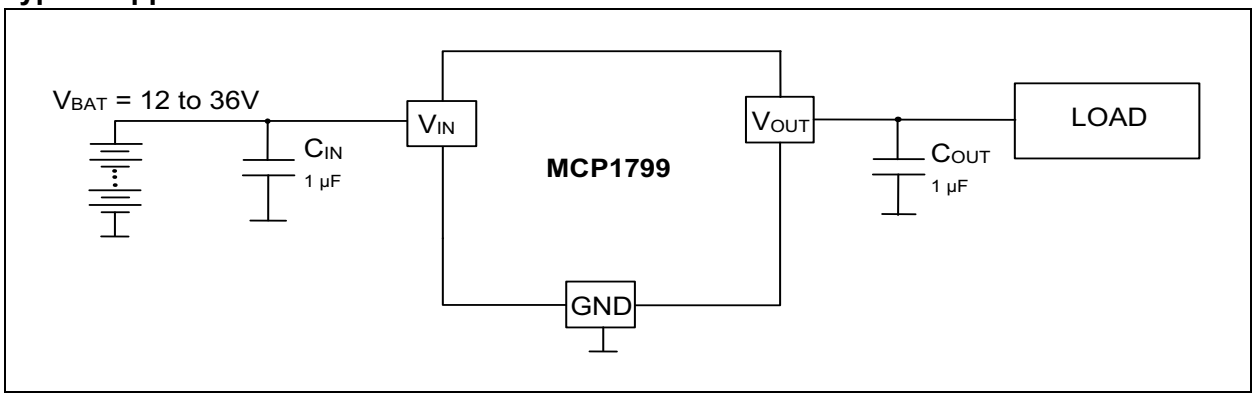
3-Pin SOT-23



3-Pin SOT-223



Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Input Voltage ..... +66.0V
Maximum Voltage on V_{IN} ..... (GND - 0.3V) to (V_{IN}+0.3V)
Maximum Voltage on V_{OUT}- ..... (GND - 0.3V) to 5.5V
Internal Power Dissipation ..... Internally-Limited **(Note 3)**
Output Short Circuit Current..... Continuous
Storage Temperature ..... -55°C to +175°C
Maximum Junction Temperature, T_J ..... +185°C
Operating Junction Temperature, T_J ..... -40°C to +150°C
ESD protection on all pins:
HBM ..... ≥ 4 kV
CDM ..... ≥ 750V
MM ..... ≥ 400V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, V_{IN} = 6.2V(for V_R =5V), V_{IN} = 4.5V(for V_R =3.3V), I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 µF ceramic (X7R), T_A = +25°C. **Boldface** type applies for ambient temperatures T_A of -40°C to +150°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Operating Voltage	V_{IN}	**4.5**	—	**45**	V	V_R = 3.3V, I_{OUT} ≤ 80 mA
		6.2	—	**45**		V_R = 5V, I_{OUT} ≤ 80 mA
Input Voltage to Turn On Output	V_{UVLO_High}	—	2.8	—	V	rising V_{IN}, V_{IN} = 0 to $V_{IN(MIN)}$
Input Voltage to Turn Off Output	V_{UVLO_Low}	—	2.6	—		falling V_{IN}, V_{IN} = $V_{IN(MIN)}$ to 0
Output Voltage Range	V_{OUT}	**V_R-2%**	V_R	**V_R+2%**		**(Note 1)**
Input Quiescent Current	I_Q	—	25	**45**	µA	I_{OUT} = 0A
Ground Current	I_{GND}	—	45	**110**	µA	I_{OUT} = 80 mA
Maximum Output Current	I_{OUT}	**80**	—	—	mA	**(Note 3)**
Line Regulation	$\Delta V_{OUT}/(V_{OUT} x \Delta V_{IN})$	**-0.05**	±0.02	**+0.05**	%/V	4.5V ≤ V_{IN} ≤ 45V for V_R = 3.3V 6.2V ≤ V_{IN} ≤ 45V for V_R = 5V

Note 1: V_R is the nominal regulator output voltage.

2: Load regulation is measured at a constant ambient temperature using a DC current source. Load regulation is tested over a load range 1 mA to the maximum specified output current.

3: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). See **Section "Temperature Specifications"** for more information. Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C might impact the device reliability.

4: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of V_{IN} = V_R + 1.2V.

5: PSRR measurement is carried out with C_{IN} = 0 µF, V_{IN} = 7V, I_{OUT} = 50 mA, V_{INAC} = 0.4V_{pkpk}

6: Not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, V_{IN} = 6.2V(for V_R =5V), V_{IN} = 4.5V(for V_R =3.3V), I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 µF ceramic (X7R), T_A = +25°C. **Boldface** type applies for ambient temperatures T_A of -40°C to +150°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-0.8**	±0.4	**+0.8**	%	I_{OUT} = 1 mA to 80 mA **(Note 2)**
Output Current Limit	I_{OUT_CL}	—	150	**215**	mA	$V_{IN} = V_{IN(MIN)}$, V_{OUT} > 0.1V, **(Note 6)**
Output Peak Current Limit	I_{OUT_PCL}		1700	**2500**	mA	
Dropout Voltage	$V_{DROPOUT}$	—	300	**1100**	mV	I_{OUT} = 80 mA **(Note 4)**
AC Performance						
Output Noise	e_N	—	500	—	µVrms	f = 100 Hz to 100 kHz V_{IN} = 12V, V_R = 5V I_{OUT} = 10 mA **(Note 6)**
Power Supply Ripple Rejection Ratio	PSRR	—	70	—	dB	f = 100 Hz **(Note 5)** **(Note 6)**
			70			f = 1 kHz **(Note 5)** **(Note 6)**
			35			f = 100 kHz **(Note 5)** **(Note 6)**

Note 1: V_R is the nominal regulator output voltage.

2: Load regulation is measured at a constant ambient temperature using a DC current source. Load regulation is tested over a load range 1 mA to the maximum specified output current.

3: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). See **Section "Temperature Specifications"** for more information. Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C might impact the device reliability.

4: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 1.2V$.

5: PSRR measurement is carried out with C_{IN} = 0 µF, V_{IN} = 7V, I_{OUT} = 50 mA, $V_{INAC} = 0.4V_{pkpk}$

6: Not production tested.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Thermal Shutdown	T_{SD}		180		°C	Rising Temperature
Thermal Shutdown Hysteresis	ΔT_{SD}	—	22		°C	Falling Temperature
Thermal Package Resistances						
Thermal Resistance, SOT23-3LD	θ_{JA}	—	212	—	°C/W	JEDEC® standard 4 layer FR4 board with 1 oz. copper
	θ_{JC}	—	139	—		
Thermal Resistance, SOT223-3LD	θ_{JA}	—	70	—		
	θ_{JC}	—	60	—		

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $C_{IN} = C_{OUT} =$ 1 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, $V_{IN} = V_R + 1.2V$.

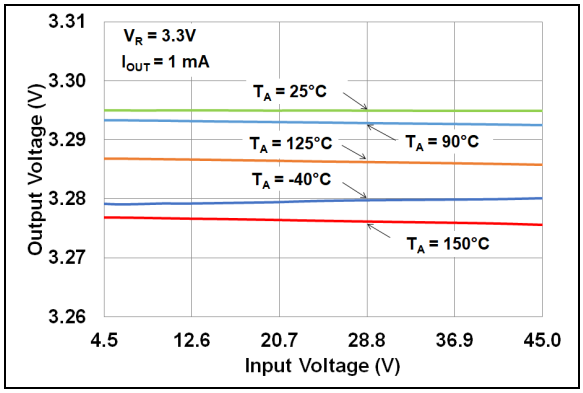


FIGURE 2-1: *Output Voltage vs. Input Voltage (V_R = 3.3V).*

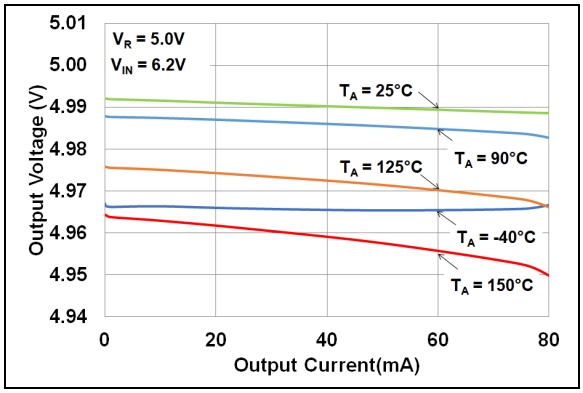


FIGURE 2-4: *Output Voltage vs. Output Current (V_R = 5.0V).*

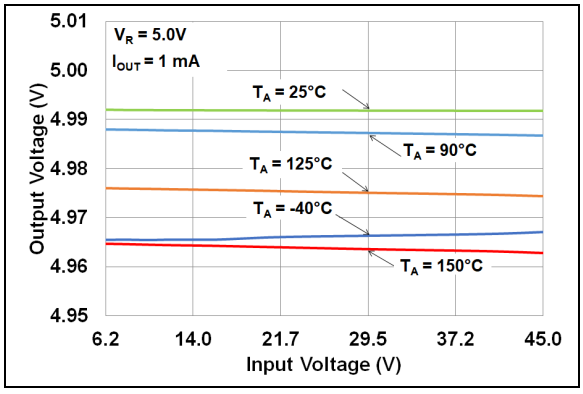


FIGURE 2-2: *Output Voltage vs. Input Voltage (V_R = 5.0V).*

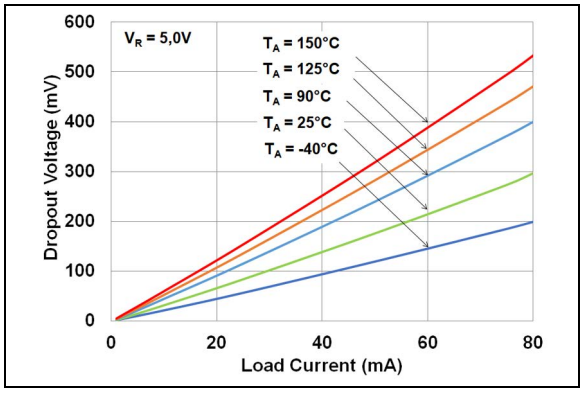


FIGURE 2-5: *Dropout Voltage vs. Output Current.*

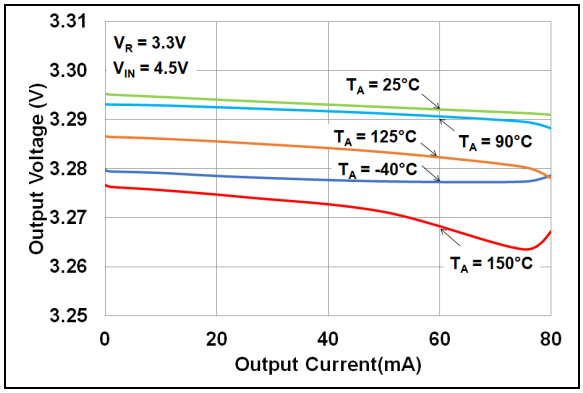


FIGURE 2-3: *Output Voltage vs. Output Current (V_R = 3.3V).*

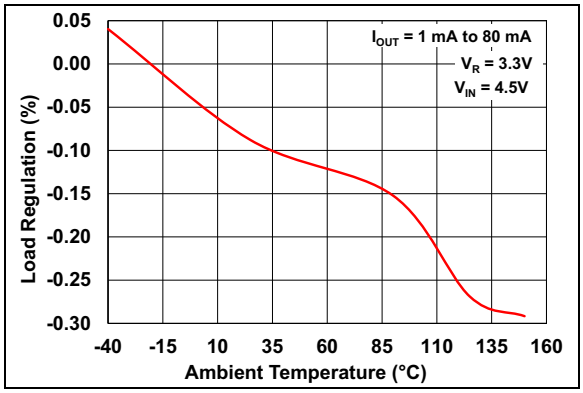


FIGURE 2-6: *Load Regulation vs. Ambient Temperature (V_R = 3.3V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT} =$ 1 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, $V_{IN} = V_R$ + 1.2V.

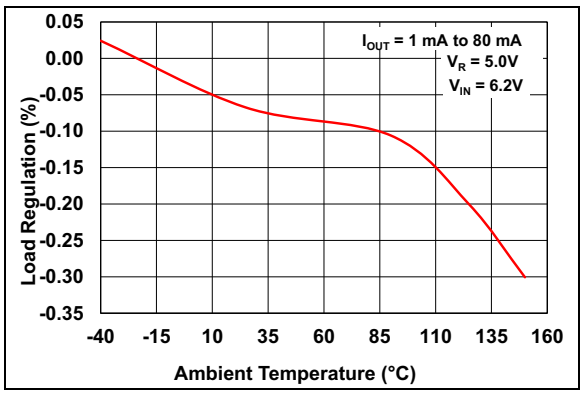


FIGURE 2-7: *Load Regulation vs. Ambient Temperature (V_R = 5.0V).*

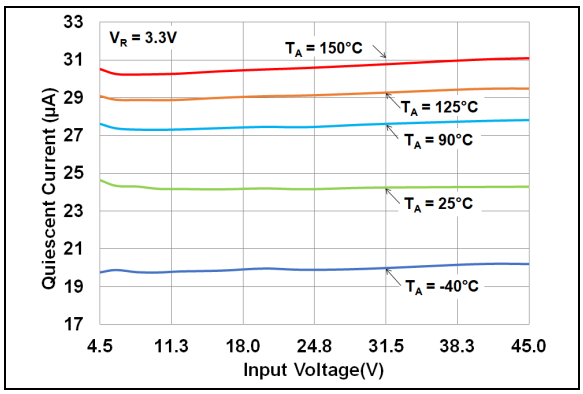


FIGURE 2-10: *Quiescent Current vs.Input Voltage (V_R = 3.3V).*

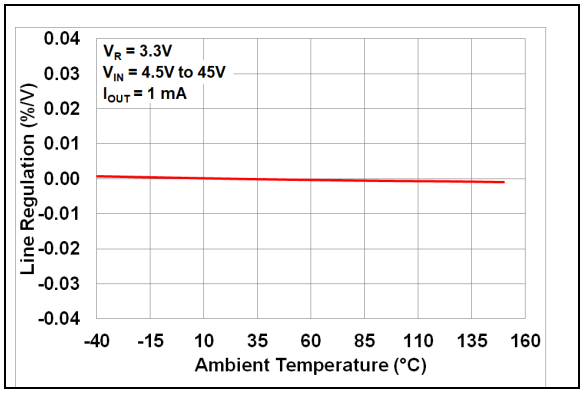


FIGURE 2-8: *Line Regulation vs. Ambient Temperature (V_R = 3.3V).*

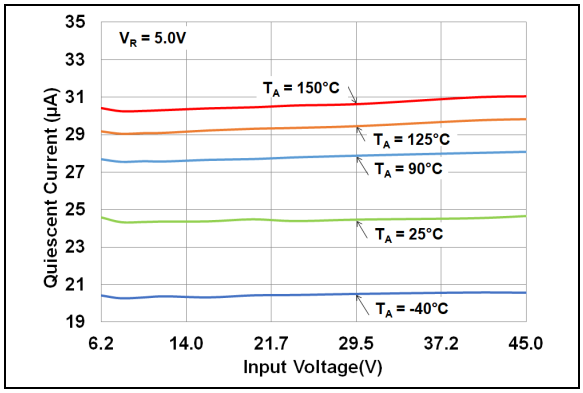


FIGURE 2-11: *Quiescent Current vs.Input Voltage (V_R = 5.0V).*

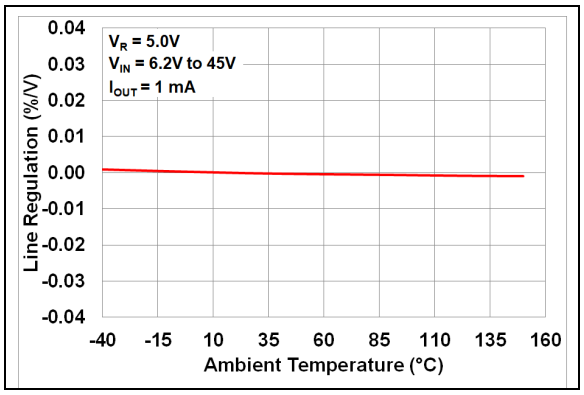


FIGURE 2-9: *Line Regulation vs. Ambient Temperature (V_R = 5.0V).*

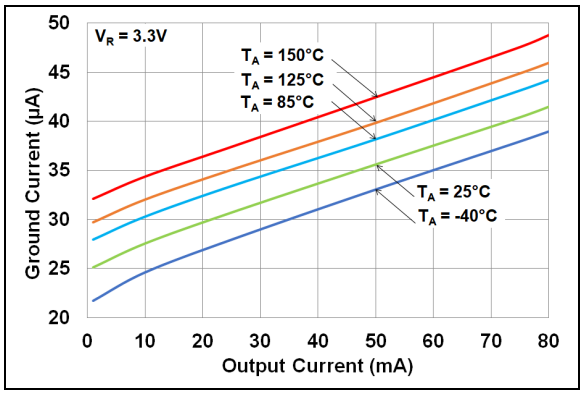


FIGURE 2-12: *Ground Current vs. Output Current (V_R = 3.3V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT} = 1\ \mu F$ ceramic (X7R), $I_{OUT} = 1$ mA, $T_A = +25°C$, $V_{IN} = V_R + 1.2V$.

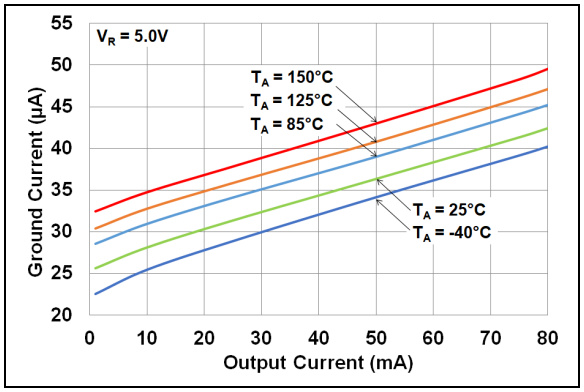


FIGURE 2-13: *Ground Current vs. Output Current (V_R = 5.0V).*

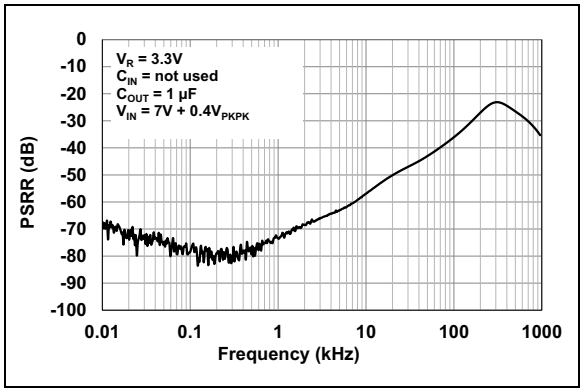


FIGURE 2-16: *Power Supply Ripple Rejection Ratio vs. Frequency (V_R = 3.3V).*

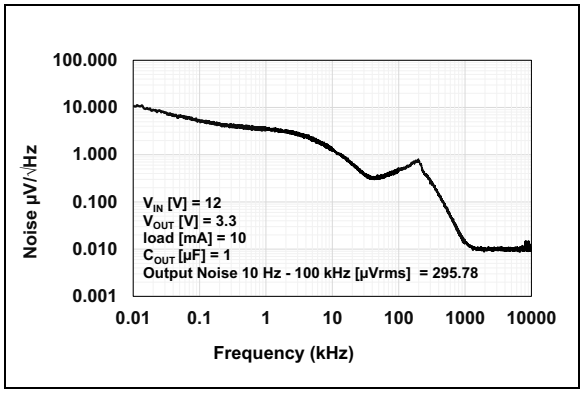


FIGURE 2-14: *Noise vs. Frequency (V_R = 3.3V).*

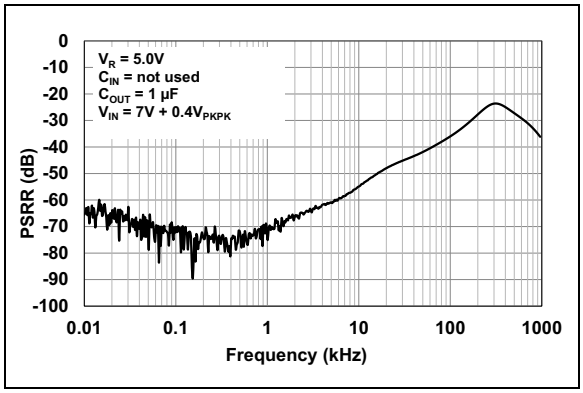


FIGURE 2-17: *Power Supply Ripple Rejection Ratio vs. Frequency (V_R = 5.0V).*

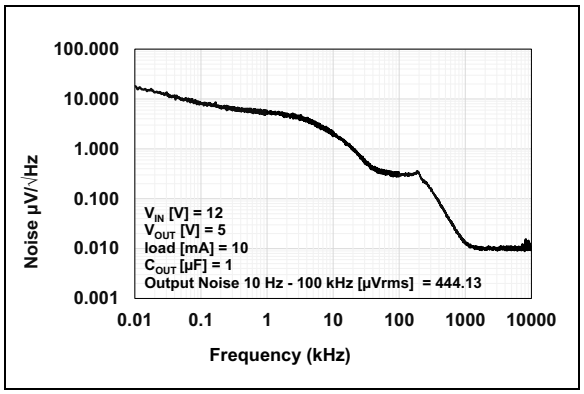


FIGURE 2-15: *Noise vs. Frequency (V_R = 5.0V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT} = 1\ \mu F$ ceramic (X7R), $I_{OUT} = 1$ mA, $T_A = +25°C$, $V_{IN} = V_R + 1.2V$.

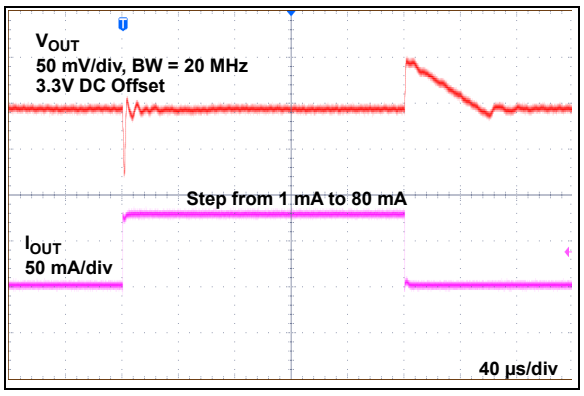


FIGURE 2-18: *Load Step Response ($V_R = 3.3V$).*

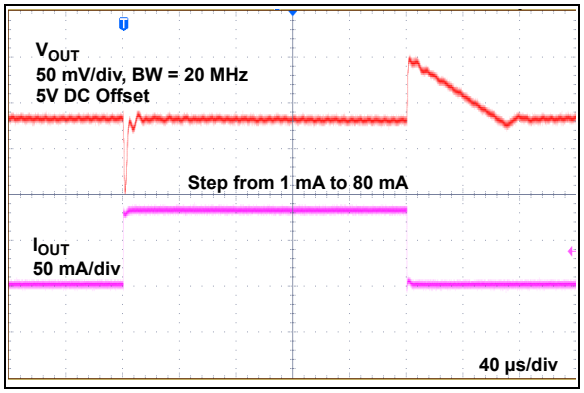


FIGURE 2-19: *Load Step Response ($V_R = 5.0V$).*

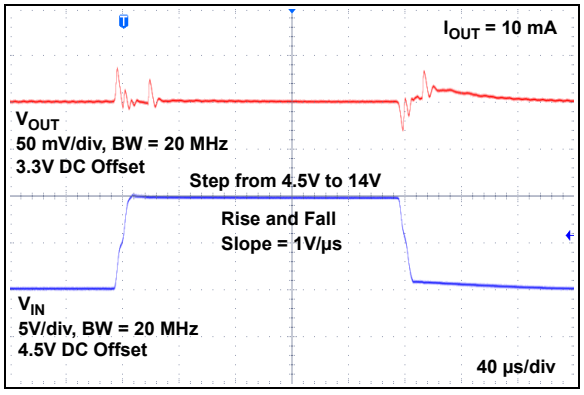


FIGURE 2-20: *Line Step Response ($V_R = 3.3V$).*

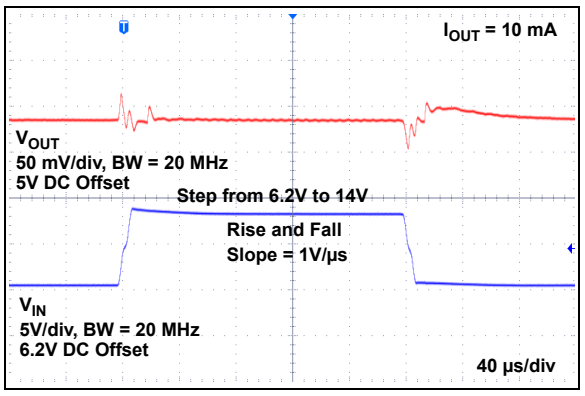


FIGURE 2-21: *Line Step Response ($V_R = 5.0V$).*

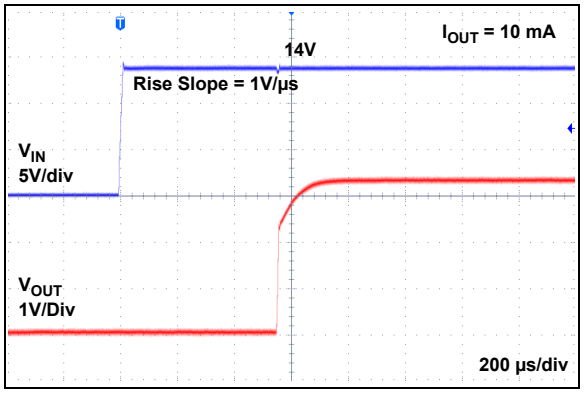


FIGURE 2-22: *Start-up ($V_R = 3.3V$).*

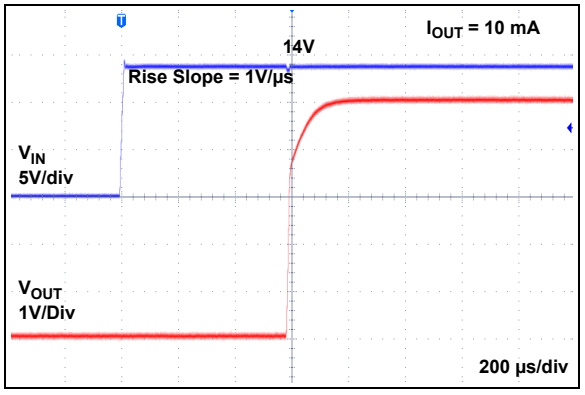


FIGURE 2-23: *Start-up ($V_R = 5.0V$).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT} = 1\ \mu F$ ceramic (X7R), $I_{OUT} = 1$ mA, $T_A = +25°C$, $V_{IN} = V_R + 1.2V$.

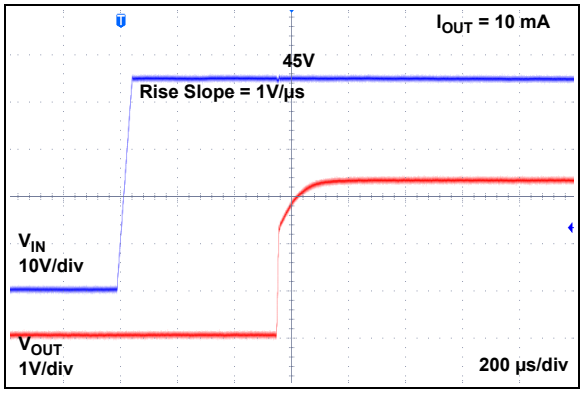


FIGURE 2-24: *Start-up (V_R = 3.3V).*

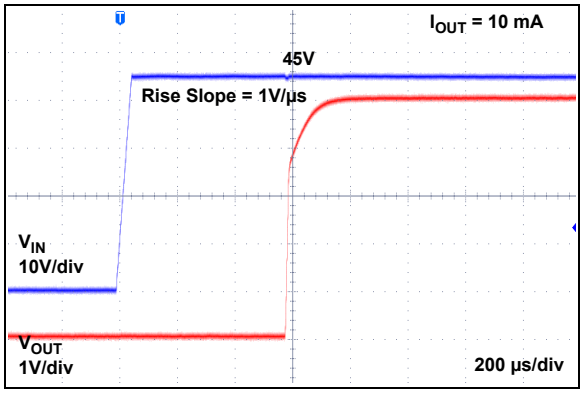


FIGURE 2-25: *Start-up (V_R = 5V).*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

SOT 23-3	SOT 223-3	Symbol	Description
1	2	GND	Ground
2	3	V_{OUT}	Regulated Output Voltage V_R
3	1	V_{IN}	Input Voltage Supply
—	4	TAB	Exposed Thermal Pad, connected internally to GND

3.1 Ground Pin (GND)

For optimal noise and Power Supply Rejection Ratio (PSRR) performance, the GND pin of the LDO should be tied to an electrically quiet circuit ground. This will ensure the LDO power supply rejection ratio and noise device performance. The GND pin of the LDO conducts only ground current, therefore a wide trace is not required. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower the inductance and as a result, reduce the effect of fast current transients.

3.2 Regulated Output Voltage Pin (V_{OUT})

The V_{OUT} pin is the regulated output voltage V_R of the LDO. A minimum output capacitance of 1 µF is required for the LDO to ensure the stability in all the typical applications. The MCP1799 is stable with ceramic capacitors. See **Section 4.2, Output Capacitance Requirements** for output capacitor selection guidance.

3.3 Input Voltage Supply Pin (V_{IN})

Connects the voltage source to V_{IN}. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 µF to 10 µF should be sufficient for most applications. The type of capacitor used is ceramic. However, the low ESR characteristics of the ceramic capacitor will yield better noise and PSRR performance at high frequency.

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP1799 is an AEC-Q100 qualified LDO, capable of delivering 80 mA of current, over the entire operating temperature range. The part is stable with a minimum 1 µF output ceramic capacitor, has current limit protection and extended working temperature range: -40° to +150°. The device also features a PSRR of 70 dB typical for 100 Hz frequency.

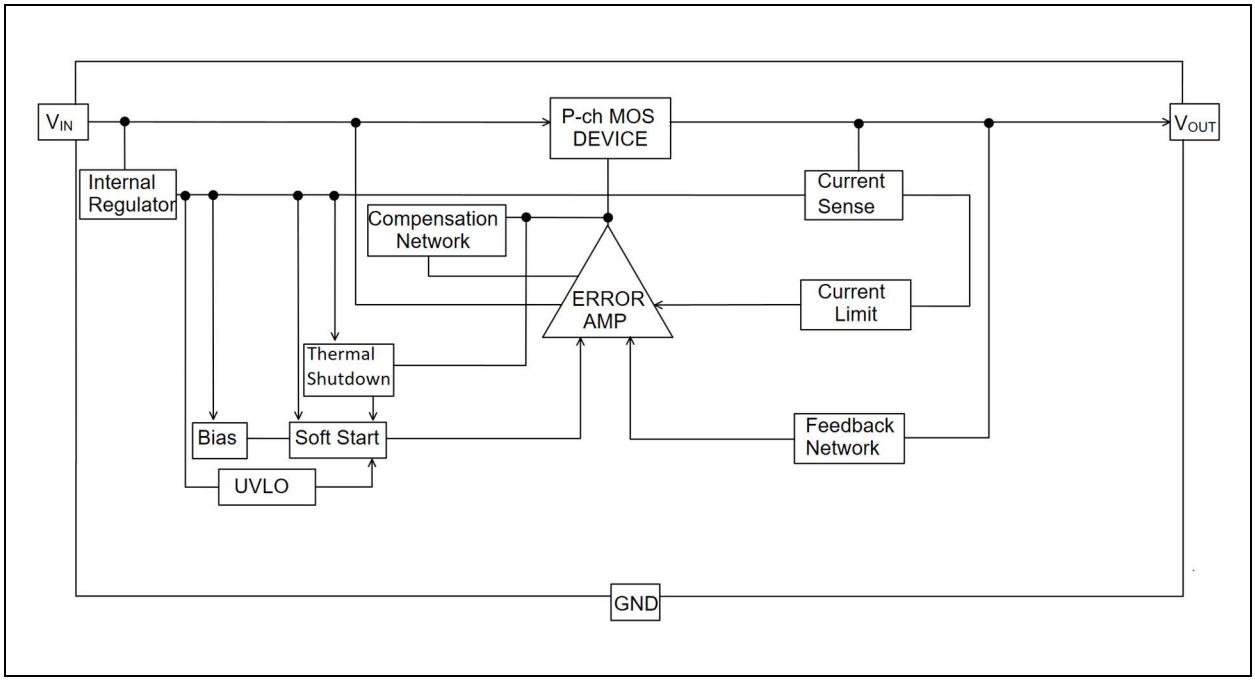


FIGURE 4-1: *Simplified Functional Block Diagram.*

4.2 Output Capacitance Requirements

The MCP1799 requires a minimum output capacitance of 1 µF for output voltage stability. The output capacitor should be located as close to the LDO output as it is practical. The device is designed to work with low ESR ceramic capacitors. Ceramic materials X8R/L or X7R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 mΩ. It is recommended to use an appropriate voltage rating capacitor, and the derating of the capacitance as a function of voltage and temperature needs to be taken into account. For improved transitory behavior over the entire temperature range, a 2.2 µF output capacitor is recommended. The ceramic capacitor type should be X7R or X8R/L because their dielectrics are rated for use with temperatures between -40°C to +125° or -55°C to +150°C, respectively.

4.3 Input Capacitance Requirements

Low input-source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (>10 inches) between the input source and the LDO, adding input capacitance is recommended. A minimum of 1 µF to 10 µF of capacitance is sufficient for most applications. Given the high input voltage capability of the MCP1799, of up to 45V DC, it is recommended to use an appropriate voltage rating capacitor, and the de-rating of the capacitance as a function of voltage and temperature needs to be taken into account. The ceramic capacitor type should be X7R or X8R/L because their dielectrics are rated for use with temperatures between -40°C to +125°C or -55°C to +150°C, respectively.

4.4 Circuit Protection

The MCP1799 features current limit protection during an output short circuit event that occurs in normal operation.

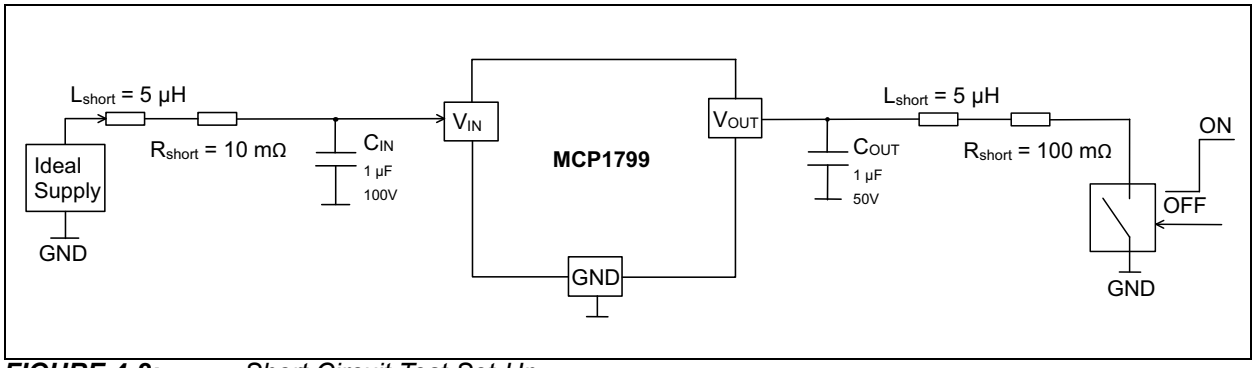


FIGURE 4-2: *Short Circuit Test Set-Up.*

The MCP1799 was tested using the AEC-Q100 test set-up as shown in Figure 4-2. The testing conditions require the use of very high parasitic inductances on the input and output. For cases like this, it is required to prevent the output voltage going below ground with more than 1V.

Note that the V_{OUT} pin can withstand a maximum of -0.3V_{DC} (see **Absolute Maximum Ratings (†)**). This can be achieved by placing a Schottky diode with the cathode to V_{OUT} and anode to ground.

Thermal shutdown functionality is present on the device and adds to the protection features of the part. Thermal shutdown gets triggered at typical value of +180°C and has a typical hysteresis of 22°.

4.5 Dropout Operation

For V_R = 5V, MCP1799 can be found operating in a dropout condition (the minimum input voltage is 4.5V), which can happen during a cold crank event, when the supply voltage can drop down to 3V. It is preferred to make sure that the part does not operate in dropout during DC operation so that the AC performance is maintained. See Figure 4-3.

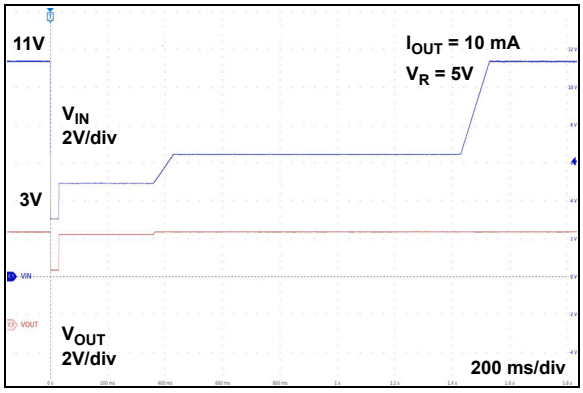


FIGURE 4-3: *Line Step from Dropout.*

The device has a dropout voltage of approximately 300 mV at full load and room temperature, but because of the extended temperature range at +150°C, due to increased leakage at hot, it reaches up to 1100 mV. For a 5V output, the minimum supply voltage required in order to have a regulated output, within specification, is 6.2V.

4.6 Input UVLO

On the rising edge of the V_{IN} input, the internal architecture adds 550 µs delay before allowing the regulator output to turn on. After this 550 µs delay, the regulator starts charging the load capacitor as the output rises from 0V to its regulated value. The charging current amplitude will be limited by the short circuit current value of the device.

The UVLO block helps prevent false start-ups, during the power-up sequence, until the input voltage reaches a value of 2.8V. The minimum input voltage required for normal operation is 4.5V.

4.7 Package and Device Qualifications

The MCP1799 are AEC-Q100, grade 0 and PPAP capable. The Grade 0 qualification allows the MCP1799 to be used within an extended temperature range, from -40°C to +150°C.

5.0 APPLICATION INFORMATION

5.1 Typical Application

The MCP1799 is used for applications that require high input voltage and are prone to high transient voltages on the input.

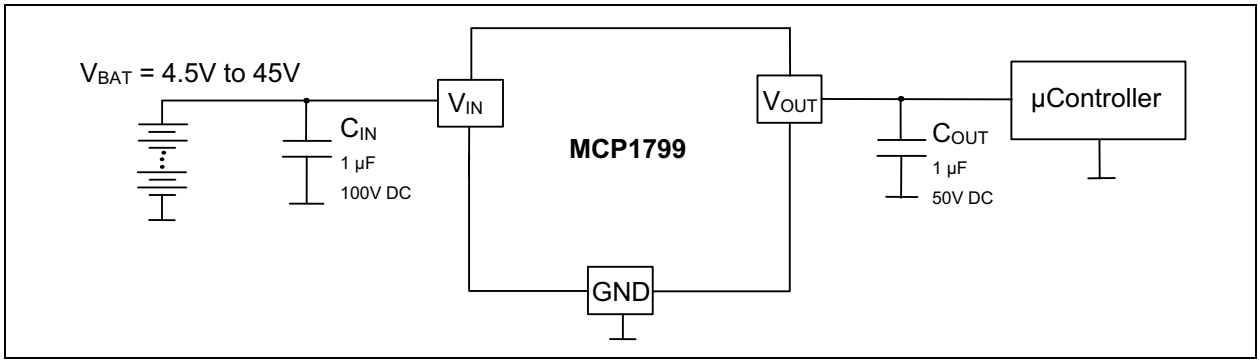


FIGURE 5-1: *Typical Application Circuit using a High Voltage Battery Pack.*

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1799 is a function of input voltage, output voltage, output current and quiescent current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

P_{LDO} = Internal power dissipation of the LDO pass device

$V_{IN(MAX)}$ = Maximum input voltage

$V_{OUT(MIN)}$ = LDO minimum output voltage

$I_{OUT(MAX)}$ = Maximum output current

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1799 as a result of quiescent or ground current. The power dissipation, as a result of the ground current, can be calculated by applying Equation 5-2:

EQUATION 5-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{GND}$$

Where:

$P_{I(GND)}$ = Power dissipation due to the ground current of the LDO

$V_{IN(MAX)}$ = Maximum input voltage

I_{GND} = Current flowing into the GND pin

The total power dissipated within the MCP1799 is the sum of the power dissipated in the LDO pass device and the $P(I_{GND})$ term. Because of the CMOS construction, the typical I_{GND} for the MCP1799 is typical 50 µA at full load. Operating at a maximum V_{IN} of 45V results in a power dissipation of 2.25 mW.
For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1799 is +150°C. To estimate the internal junction temperature of the MCP1799, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient ($R\theta_{JA}$) of the device. See Equation 5-3. For example, the thermal resistance from junction-to-ambient for the 3-Lead SOT-223 package is estimated at 70°C/W.

EQUATION 5-3:

$$T_{J(MAX)} = P_{LDO} \times \theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$ = Maximum continuous junction temperature

P_{LDO} = Total power dissipation of the device

θ_{JA} = Thermal resistance from junction-to-ambient

$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. Equation 5-4 can be used to determine the package maximum internal power dissipation.

EQUATION 5-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation of the device

$T_{J(MAX)}$ = Maximum continuous junction temperature

$T_{A(MAX)}$ = Maximum ambient temperature

θ_{JA} = Thermal resistance from junction-to-ambient

EQUATION 5-5:

$$T_{J(RISE)} = P_{D(MAX)} \times \theta_{JA}$$

Where:

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

$P_{D(MAX)}$ = Maximum power dissipation of the device

θ_{JA} = Thermal resistance from junction-to-ambient

EQUATION 5-6:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J = Junction temperature

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

T_A = Ambient temperature

5.3 Typical Application Examples

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

Note that the formulas to calculate Example 5-1 are shown in Equation 5-5 and Equation 5-6.

5.3.1 POWER DISSIPATION EXAMPLE

EXAMPLE 5-1:

Package

Package Type = 3 Lead SOT223

Input Voltage

V_{IN} = 14V ± 5%

LDO Output Voltage and Current

V_{OUT} = 5V

I_{OUT} = 50 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +60°C

Internal Power Dissipation

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

P_{LDO} = (14.7 – 4.9) x 50 mA

P_{LDO} = 0.49 Watts

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and of the thermal resistance from junction-to-ambient for the application. The thermal resistance from junction-to-ambient (θ_{JA}) is derived from EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction-to-ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to Application Note AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"* (DS00792), for more information regarding this subject.

EXAMPLE 5-2:

$T_{J(RISE)} = P_{LDO(Max)} \times \theta_{JA}$

$T_{J(RISE)}$ = 0.49W x 70°C/W

$T_{J(RISE)}$ = 34.3°C

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

EXAMPLE 5-3:

$T_J = T_{J(RISE)} + T_{A(MAX)}$

$T_J = 34.3°C + 60.0°C$

$T_J = 94.3°C$

5.3.1.3 Maximum Package Power Dissipation at +60°C Ambient Temperature

EXAMPLE 5-4:

3Lead SOT223 (θ_{JA} = 70°C/W):

$P_{D(MAX)} = (150°C - 60°C)/70°C/W$

$P_{D(MAX)} = 1.28W$

6.0 BATTERY PACK APPLICATION

The features of the MCP1799 make it a candidate for use in smart battery packs. The high input voltage range of up to 45V and the transient voltage capability makes it ideal for powering low-power microcontrollers used for monitoring battery health.

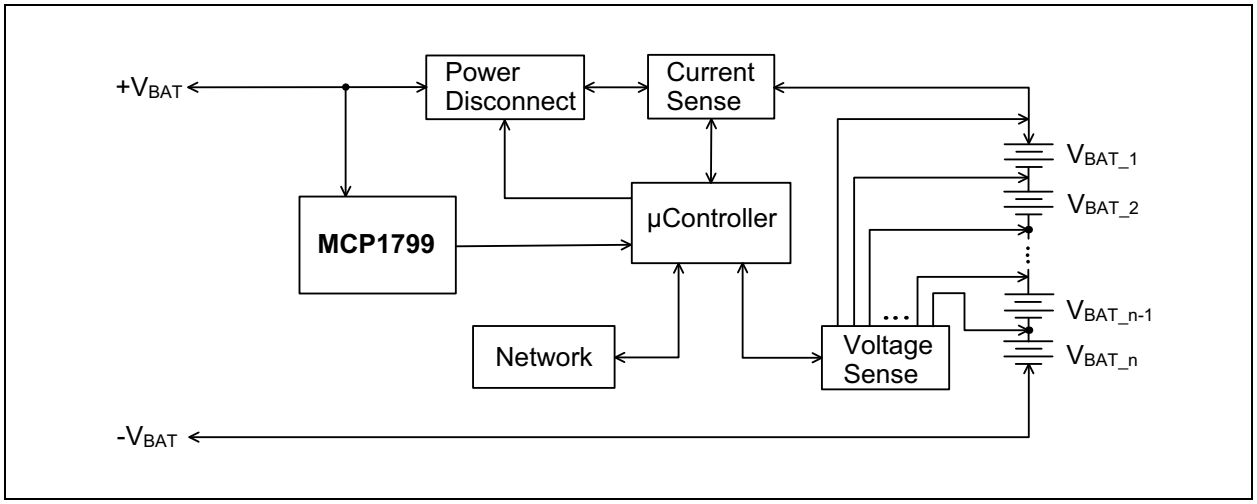
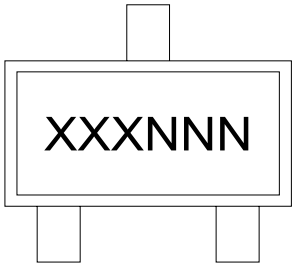


FIGURE 6-1: *Smart Battery Pack Application Example.*

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

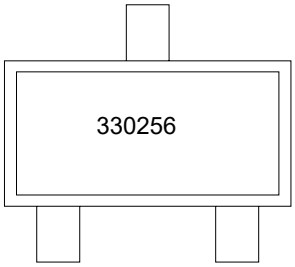
3-Lead SOT-23



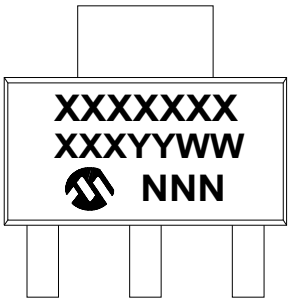
Part Number	Code
MCP1799T-3302H/TT(VAO)	330
MCP1799T-5002H/TT(VAO)	500

Note: The content of this table applies to 3-Lead SOT-23.

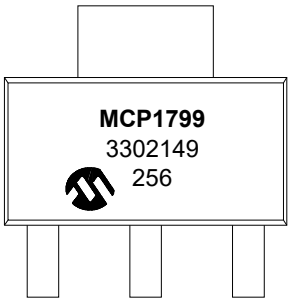
Example



3-Lead SOT-223



Example

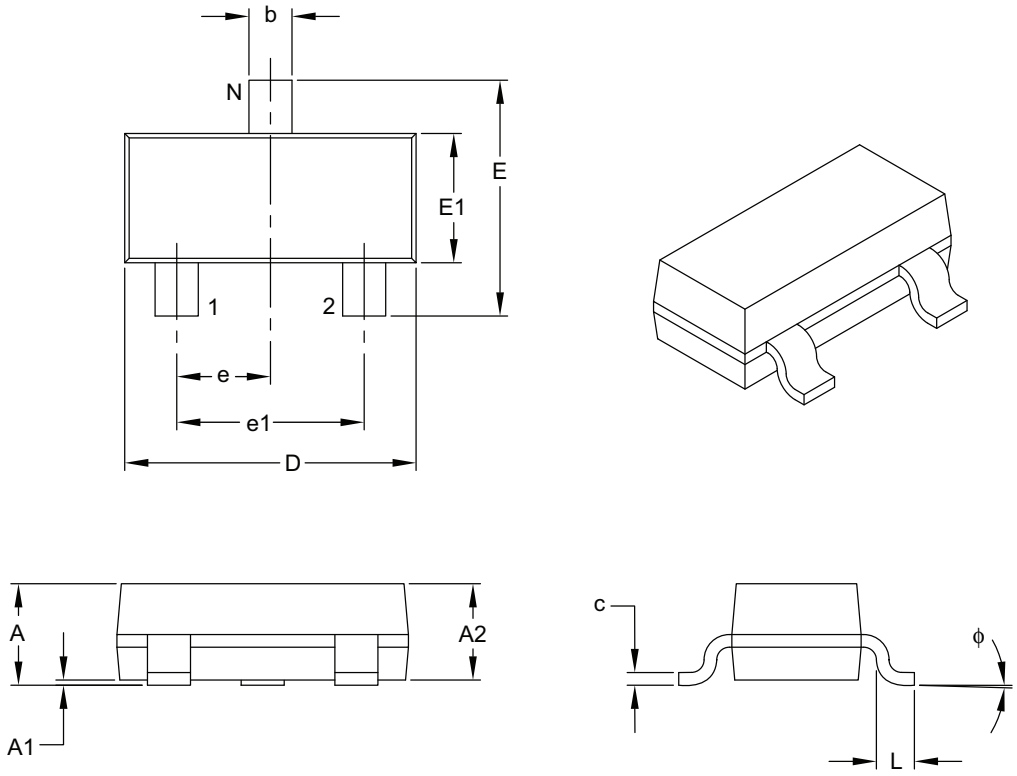


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.89	–	1.12
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	–	0.10
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.16	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Foot Angle	ϕ	0°	–	10°
Lead Thickness	c	0.08	–	0.20
Lead Width	b	0.30	–	0.54

Notes:

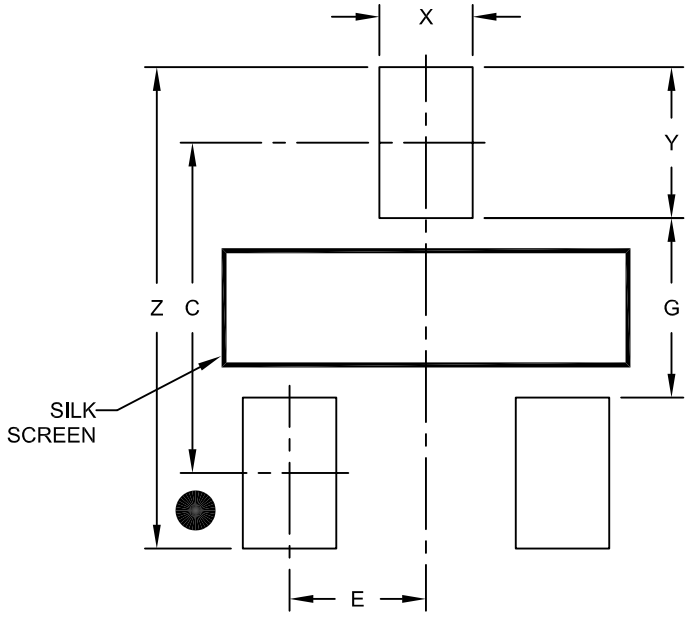
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-104B

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.30	
Contact Pad Width (X3)	X			0.65
Contact Pad Length (X3)	Y			1.05
Distance Between Pads	G	1.25		
Overall Width	Z			3.35

Notes:

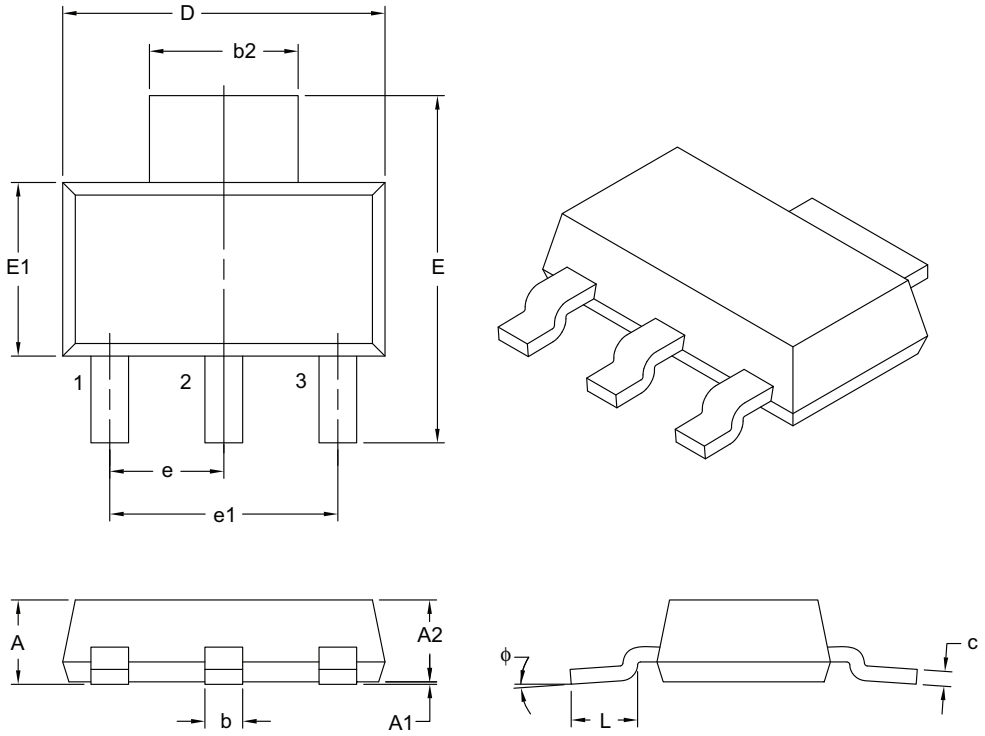
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2104A

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		3	
Lead Pitch	e		2.30 BSC	
Outside Lead Pitch	e1		4.60 BSC	
Overall Height	A	–	–	1.80
Standoff	A1	0.02	–	0.10
Molded Package Height	A2	1.50	1.60	1.70
Overall Width	E	6.70	7.00	7.30
Molded Package Width	E1	3.30	3.50	3.70
Overall Length	D	6.30	6.50	6.70
Lead Thickness	c	0.23	0.30	0.35
Lead Width	b	0.60	0.76	0.84
Tab Lead Width	b2	2.90	3.00	3.10
Foot Length	L	0.75	–	–
Lead Angle	ϕ	0°	–	10°

Notes:

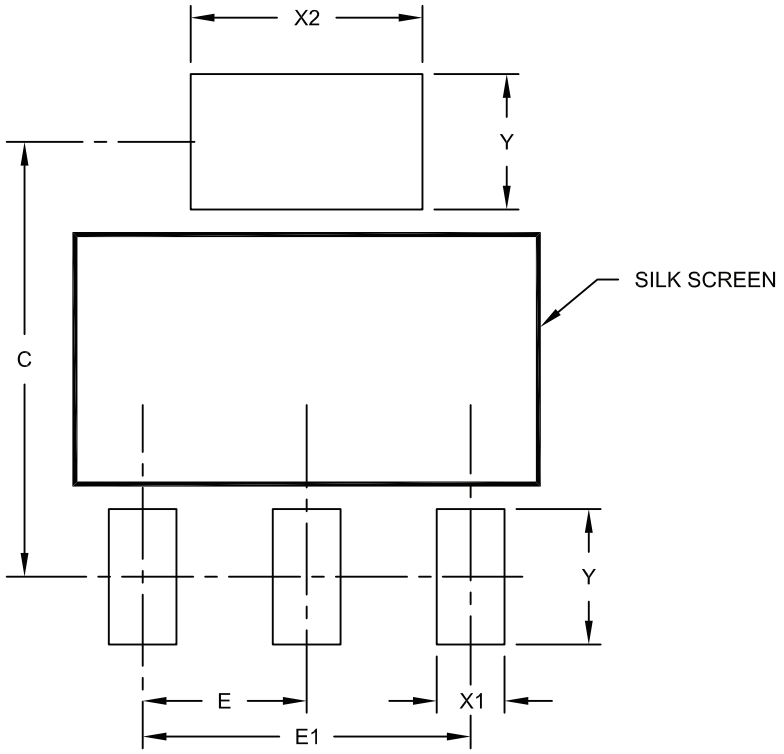
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-032B

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		2.30 BSC	
Overall Pitch	E1		4.60 BSC	
Contact Pad Spacing	C		6.10	
Contact Pad Width	X1			0.95
Contact Pad Width	X2			3.25
Contact Pad Length	Y			1.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2032A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-XX	X	X	X/	XX	XXX
Device	Tape and Reel	Output Voltage	Featured Code	Tolerance	Temp.	Package	Qualification

Device:	MCP1799:	High-voltage, Low-Dropout (LDO) Regulator
Tape and Reel Option:	<Blank>	= Standard packaging (tube or tray)
	T	= Tape and Reel
Standard Output Voltages:	33	= 3.3V
	50	= 5.0V
Temperature:	H	= -40°C to +150°C
Feature Code:	0	= Fixed
Tolerance:	2	= Standard Accuracy
Package Type:	TT	= 3-Lead Plastic Small Outline Transistor, SOT-23
	DB	= 3-Lead Plastic Small Outline Transistor, SOT-223
Qualification:	<Blank>	= Standard Part
	VAO	= Automotive AEC-Q100 Qualified

Examples:

a) MCP1799T-3302H/TT: Tape and Reel, 3.3V output voltage, Automotive temperature, 3-LD SOT-23 package

b) MCP1799T-5002H/TT: Tape and Reel, 5.0V output voltage, Automotive temperature, 3-LD SOT-23 package

c) MCP1799-3302H/DB: Tube, 3.3V output voltage, Automotive temperature, 3-LD SOT-223 package

d) MCP1799-5002H/DB: Tube, 5.0V output voltage, Automotive temperature, 3-LD SOT-223 package

e) MCP1799T-3302H/DB: Tape and Reel, 3.3V output voltage, Automotive temperature, 3-LD SOT-223 package

f) MCP1799T-5002H/DB: Tape and Reel, 5.0V output voltage, Automotive temperature, 3-LD SOT-223 package

g) MCP1799T-3302H/DBVAO: Tape and Reel, 3.3V output voltage, 3-LD SOT-223 package, Automotive Qualified

h) MCP1799T-5002H/DBVAO: Tape and Reel, 5.0V output voltage, 3-LD SOT-223 package, Automotive Qualified

i) MCP1799T-3302H/TTVAO: Tape and Reel, 3.3V output voltage, 3-LD SOT-23 package, Automotive Qualified

j) MCP1799T-5002H/TTVAO: Tape and Reel, 5.0V output voltage, 3-LD SOT-23 package, Automotive Qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2019)

- Initial release of this document.

Revision B (December 2021)

- Updated Product Identification System to include automotive qualification information and examples.
- Updated Section 7.0, Packaging Information layout and content.

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