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1. **Abstract**
 2. **Introduction**
 3. **Methods**
 4. **Results**
 5. **Discussion**
 6. **Conclusion**
 7. **References**

Figure 6

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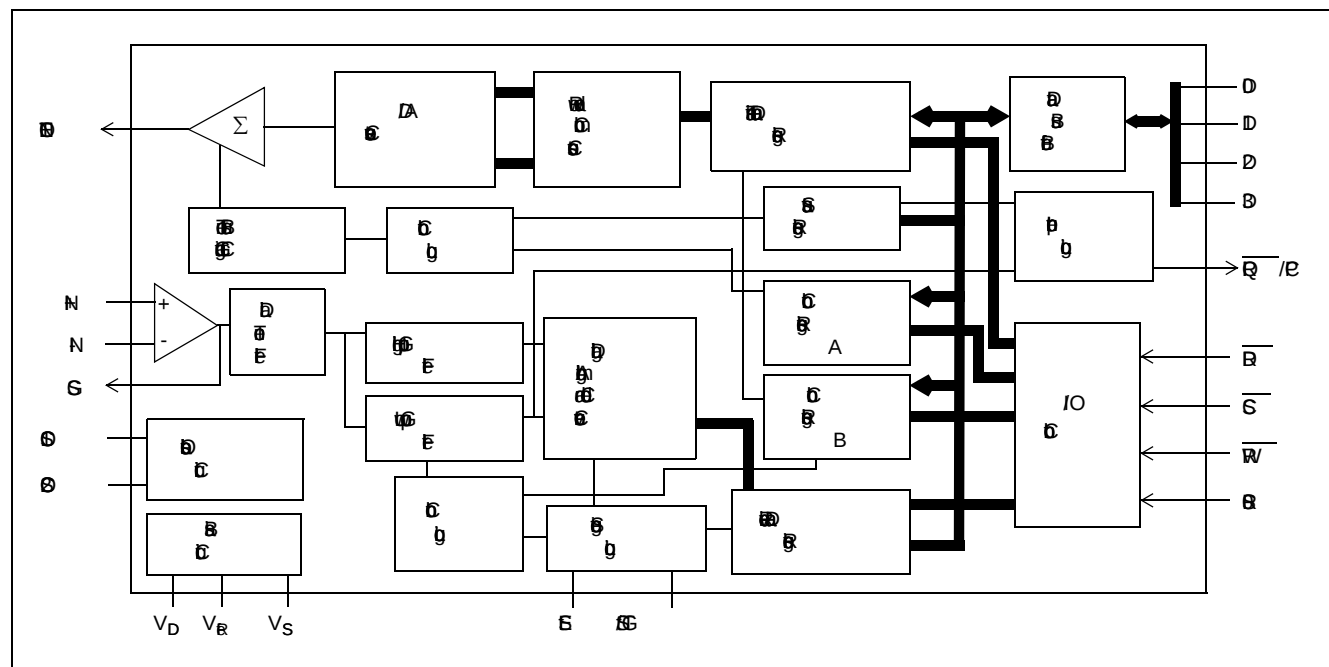


Figure 1 - Functional Block Diagram

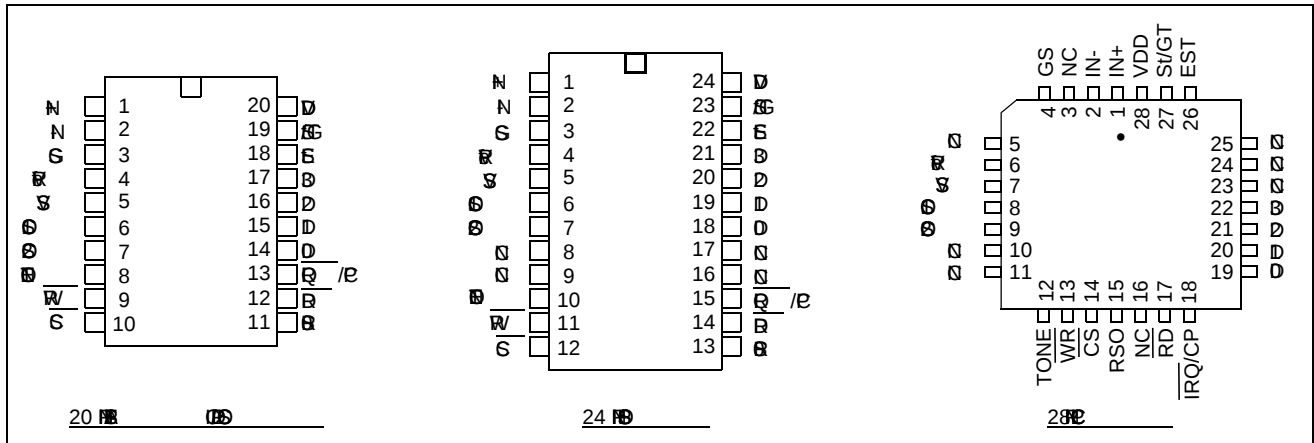


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
20	24	28		
1	1	1	N	Non-inverting μp
2	2	2	N	Inverting μp
3	3	4	S	Gain Select. μp
4	4	6	V_R	Reference Voltage ($V_D / 2$).
5	5	7	V_S	COV.
6	6	8	μp	μp
7	7	9	μp	Oscillator μp
8	10	12	μp	μp
9	11	13	$\overline{W}$	Write μp
10	12	14	$\overline{S}$	Chip Select μp
11	13	15	$\overline{R}$	Register Select μp
12	14	17	$\overline{B}$	Read μp
13	15	18	$\overline{R} / \overline{E}$	Interrupt Request/Call Progress (μp)
14-17	18-21	22-25	$\overline{D}$	Microprocessor Data Bus. μp

Pin Description (continued)

Pin #			Name	Description
20	24	28		
18	22	26	ES	Early Steering pulse
19	23	27	SG	Steering Input/Guard Time
20	24	28	V _D	5 V
	89	3,5,10, 16,17 11,16, 23,25	Q	

1.0 Functional Description

The system is designed to provide a reliable and accurate measurement of the steering input signal. The system consists of a steering input signal, a guard time, and a steering input signal. The system is designed to provide a reliable and accurate measurement of the steering input signal. The system consists of a steering input signal, a guard time, and a steering input signal.

2.0 Input Configuration

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3.0 Receiver Section

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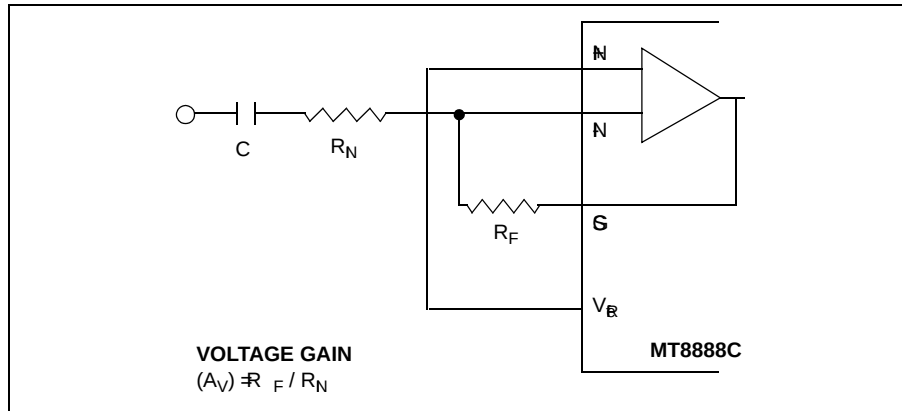


Figure 3 - Single-Ended Input Configuration

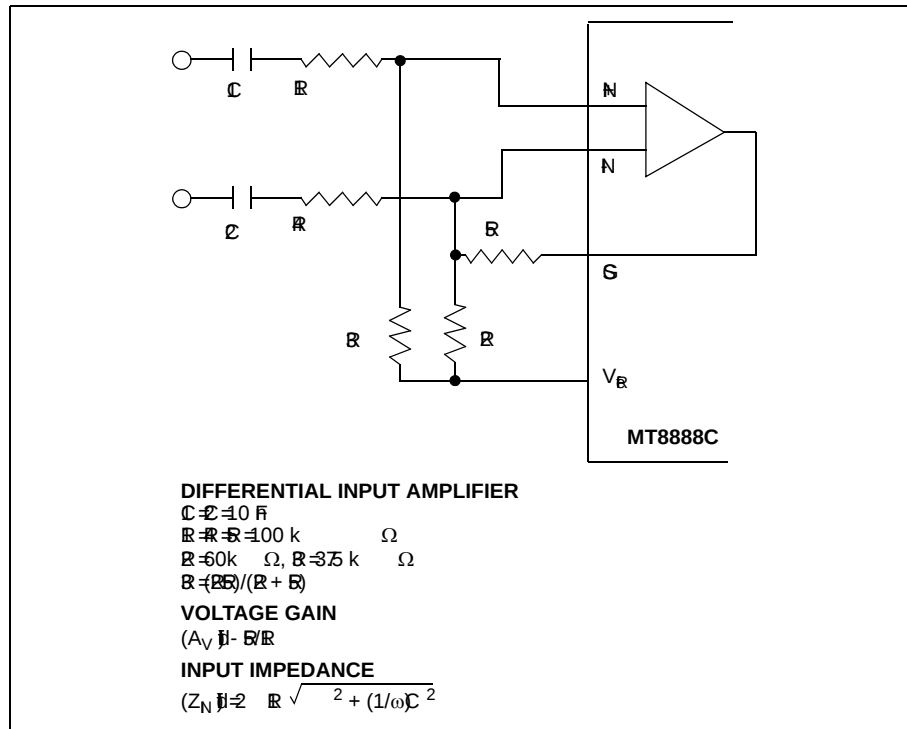


Figure 4 - Differential Input Configuration

Table 1 - Functional Encode/Decode Table

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Figure 5 is a circuit diagram of a basic steering circuit. The circuit includes an MT8888C component, a resistor R1, and a capacitor C1. The input signal is applied to the input of the MT8888C. The output of the MT8888C is connected to the input of the steering circuit. The steering circuit consists of a resistor R1 and a capacitor C1. The output of the steering circuit is connected to the input of the MT8888C. The circuit is designed to provide a guard time adjustment.

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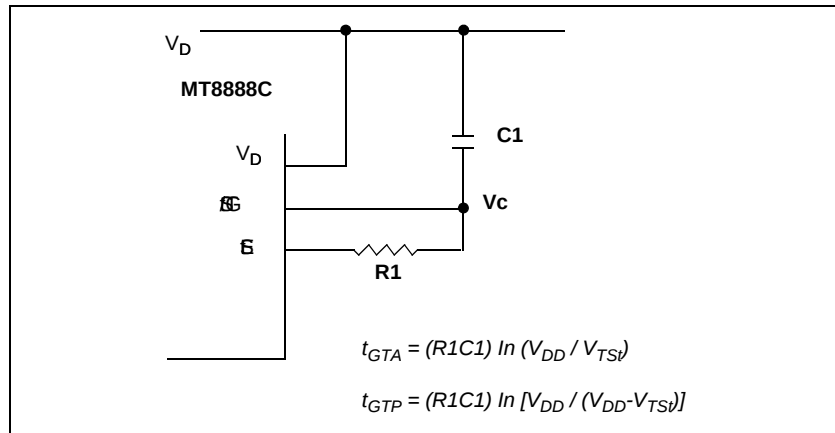


Figure 5 - Basic Steering Circuit

5.0 Guard Time Adjustment

Figure 5 is a circuit diagram of a basic steering circuit. The circuit includes an MT8888C component, a resistor R1, and a capacitor C1. The input signal is applied to the input of the MT8888C. The output of the MT8888C is connected to the input of the steering circuit. The steering circuit consists of a resistor R1 and a capacitor C1. The output of the steering circuit is connected to the input of the MT8888C. The circuit is designed to provide a guard time adjustment.

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$$t_{REC} \geq t_{DPmax} + t_{GTPmax} - t_{DAmin}$$

$$t_{REC} \leq t_{DPmin} + t_{GTPmin} - t_{DAmax}$$

$$t_{ID} \geq t_{DAmax} + t_{GTmax} - t_{DPmin}$$

$$t_{DO} \leq t_{DAmin} + t_{GTmin} - t_{DPmax}$$

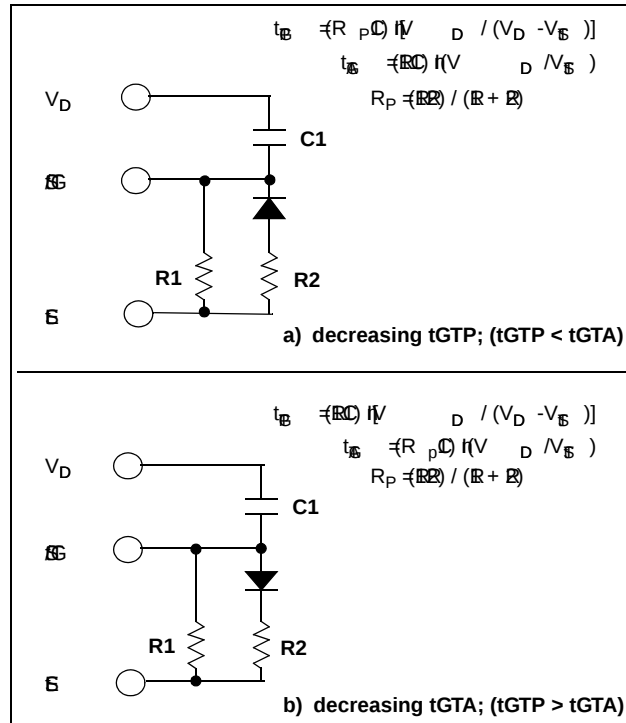


Figure 6 - Guard Time Adjustment

The circuit in Figure 6 is used to adjust the guard time (tG) of the detector. The guard time is the time interval between the detection of a signal and the start of the next measurement. The guard time is adjusted by changing the values of the resistors R1 and R2. The capacitor C1 is used to filter the signal. The equations for tG, tB, and Rp are given above.

6.0 Call Progress Filter

The Call Progress Filter is used to filter the call progress signal. The filter is a low-pass filter that allows the call progress signal to pass while blocking the noise. The filter is composed of a resistor R1 and a capacitor C1. The equations for the filter's time constant and cutoff frequency are given below.

Time constant: $\tau = R_1 C_1$
 Cutoff frequency: $f_c = \frac{1}{2\pi R_1 C_1}$

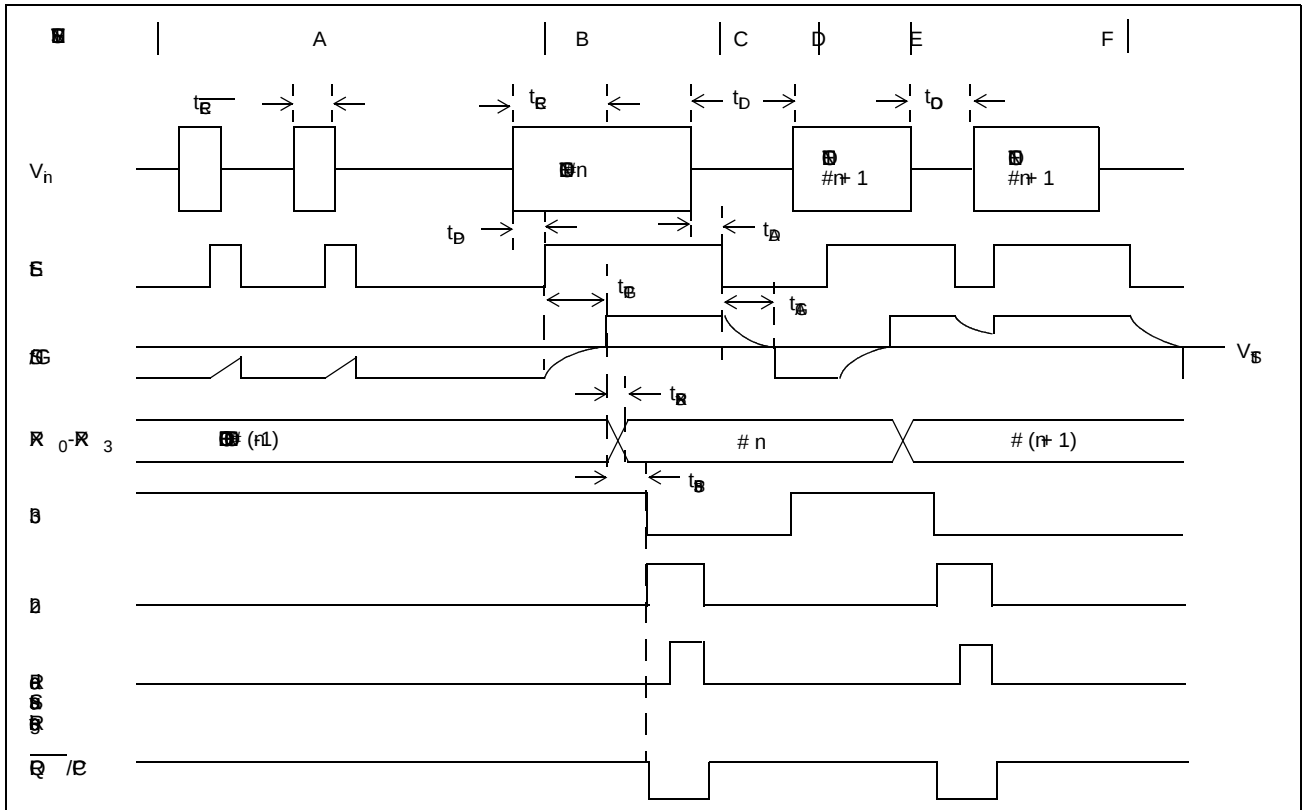


Figure 7 - Receiver Timing Diagram

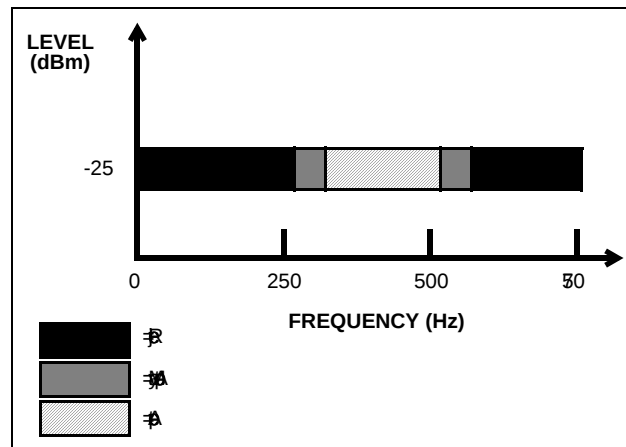
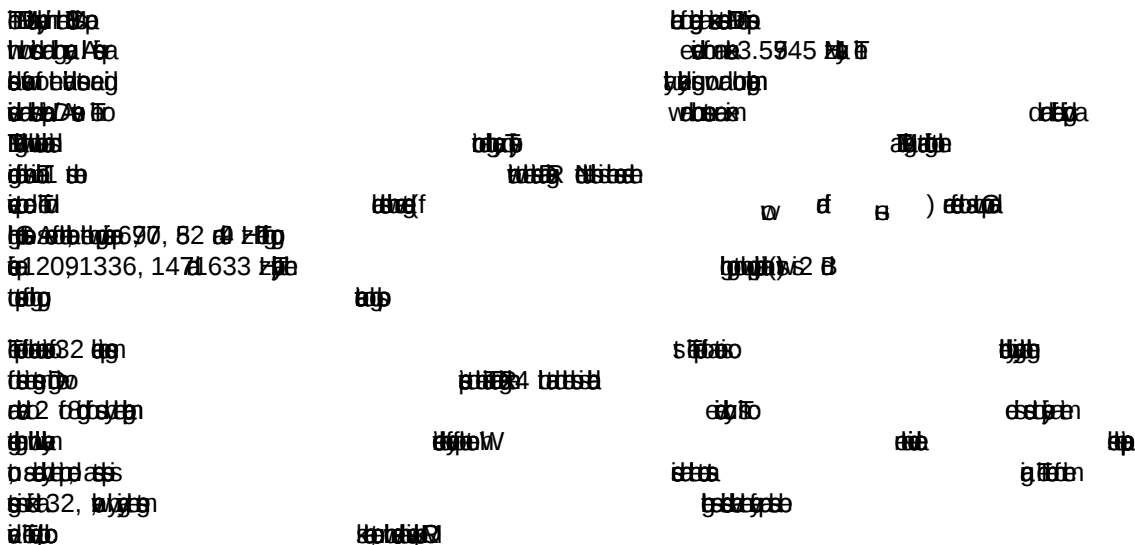


Figure 8 - Call Progress Response

EXPLANATION OF EVENTS	
A	NOISE
B	NOISE
C	NOISE
D	NOISE
E	NOISE
F	NOISE
EXPLANATION OF SYMBOLS	
V _n	NOISE
S	NOISE
AC	NOISE
R _{0-R₃}	NOISE
B	NOISE
Q	NOISE
R / E	NOISE
t _E	NOISE
t _E	NOISE
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Figure 9 - Description of Timing Events

7.0 DTMF Generator





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9.0 Single Tone Generation

Table 2 - Actual Frequencies Versus Standard Requirements

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	69	69.1	+0.30
L2	70	66.2	-0.49
L3	82	87.4	-0.54
L4	91	98	+0.7
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	147	147.9	-0.35
H4	1633	1645.0	+0.7

Table 2 - Actual Frequencies Versus Standard Requirements

10.0 Distortion Calculations

Equation 1. THD (%) For a Single Tone

$$\text{THD}(\%) = \frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \dots + V_{fn}^2}}{V_{fn}} \times 100$$

Figure 11 - Equation 1. THD (%) For a Single Tone

Equation 2. THD (%) For a Dual Tone

Equation 2. THD (%) For a Dual Tone

$$\text{THD}(\%) = \frac{\sqrt{V_{2L}^2 + V_{3L}^2 + \dots + V_{fn}^2 + V_{2H}^2 + V_{3H}^2 + \dots + V_{fn}^2}}{\sqrt{V_L^2 + V_H^2}} \times 100$$

Figure 12 - Equation 2. THD (%) For a Dual Tone

RS0	WR	RD	FUNCTION
0	0	1	Write
0	1	0	Read
1	0	1	Write
1	1	0	Read

Table 3 - Internal Register Functions

b3	b2	b1	b0
0	0	0	0

Table 4 - CRA Bit Positions

b3	b2	b1	b0
0	0	0	0

Table 5 - CRB Bit Positions

BIT	NAME	DESCRIPTION
0	0	0
1	1	1
2	2	2
3	3	3

Table 6 - Control Register A Description

Table 7 - Control Register B Description

Table 8 - Status Register Description

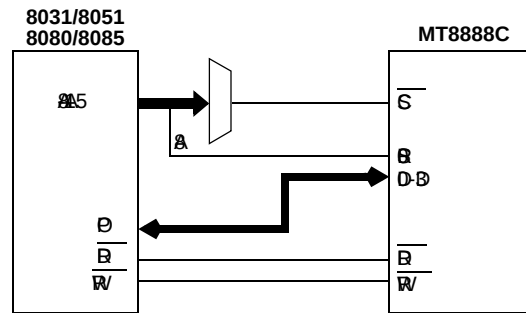


Figure 14 - MT8888C Interface Connections for Various Intel Micros

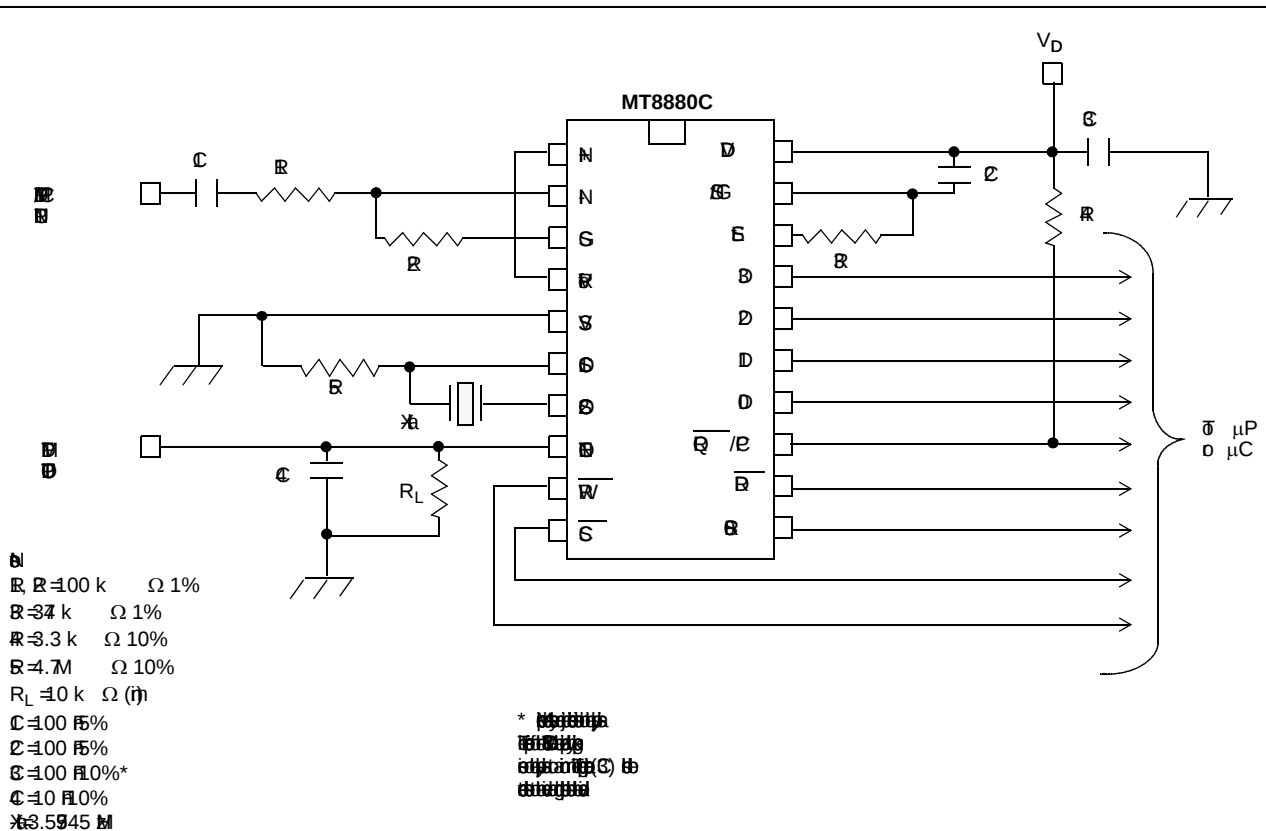


Figure 15 - Application Circuit (Single-Ended Input)

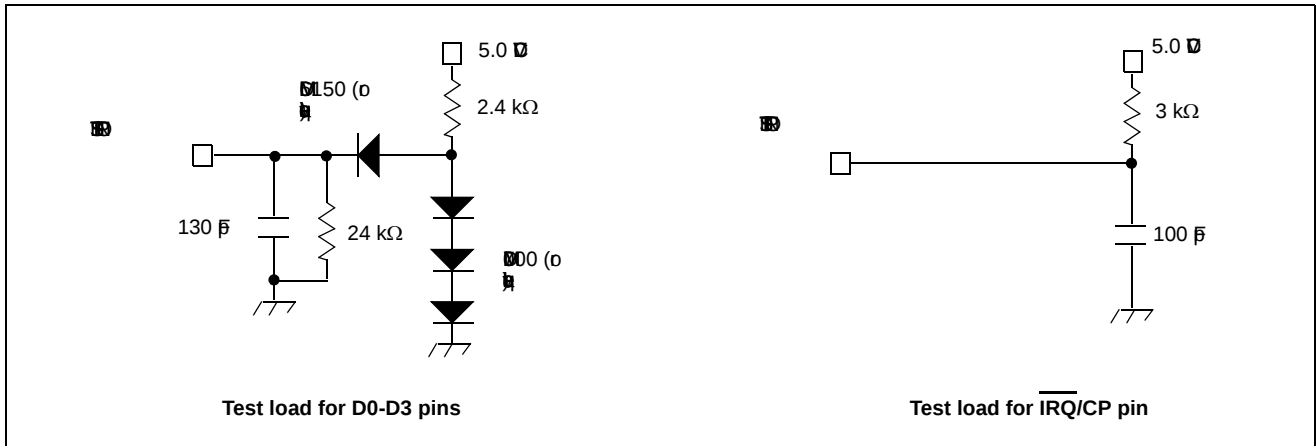


Figure 16 - Test Circuits

INITIALIZATION PROCEDURE									
Description:									
			RS0	Control WR	$\overline{RD}$		b3	Data b2	b1 b0
1)		1	0		X	X	X		
2)		1	1	0	0	0	0		
3)		1	1	0	0	0	0		
4)		1	1	0	1	0	0		
5)		1	1	0	0	0	0		
6)		1	0		X	X	X		

TYPICAL CONTROL SEQUENCE FOR BURST MODE APPLICATIONS									
Sequence:									
			RS0	$\overline{WR}$	$\overline{RD}$		b3	b2	b1 b0
1)		1	1	1	1	0	1		
2)		1	1		0	0	0		
3)		0	0	1	0	1	1		
4)									
5)		1	1	0	X	X	X		
-fb1 is set to 1.		0	0	1	0	1	0	1	
-fb2 is set to 1.		0	1	0	X	X	X		
-fb3 is set to 1.		0	1	0	X	X	X		
		0	0	1	0	1	0	1	

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (± 2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 17 - Application Notes

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	$V_D - V_S$	V_D		6	V
2	V	I	$V_S - 0.3$	$V_D + 0.3$	V
3	$I_D (V_S)$			10	A
4	T	T	-65	+150	°C
5	P	D		1000	mW

* See Figure 1

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym.	Min.	Typ.†	Max.	Units	Test Conditions
1	V	D	4.5	5.00	5.25	V	
2	T	O	-40		+8	°C	
3	f	E	3.5705	3.5745	3.58124	M	

† 25 °C

DC Electrical Characteristics - $V_S = 0V$

		Characteristics	Sym.	Min.	Typ.†	Max.	Units	Test Conditions
1	S U P	V	D	4.5	5.0	5.25	V	
2		I	D		10	11	A	
3		P	C			5.78	mW	
4	I N P U T S	$V_{DD} (S)$	V_{DD}	3.5			V	$V_{DD} = 5V$
5		$V_{DD} (S)$	V_{DD}			1.5	V	$V_{DD} = 5V$
6		V	S	2.2	2.3	2.5	V	$V_{DD} = 5V$
7	O U T P U T S	$V_{DD} (S)$ V	O			0.1	V	$V_{DD} = 5V$
8		$V_{DD} (S)$ V	θ	4.9			V	$V_{DD} = 5V$
9		$I_{DD} (R)$ I	D		1	10	μA	$V_{DD} = 2.4V$
10		$V_{DD} (R)$ V	R	2.4	2.5	2.6	V	$V_{DD} = 5V$
11		$V_{DD} (R)$ R	θ		1.3		k Ω	
12	D i g i t a l	V	L			0.8	V	
13		V	H	2.0			V	
14		I	Z			10	μA	$V_{DD} = 5V$
15	D B	I	θ	-1.4	-6.6		A V	$V_{DD} = 2.4V$
16		I	D	2.0	4.0		A V	$V_{DD} = 0.4V$

DC Electrical Characteristics (continued) - $V_S = 0V$

		Characteristics	Sym.	Min.	Typ. [†]	Max.	Units	Test Conditions
17	I_{B1}	I_{B1}	I_B	-0.5	-3.0		μA	$V_S = 4.6V$
18	I_{B2}	I_{B2}	I_B	2	4		μA	$V_S = 0.4V$
19	I_{B3}	I_{B3}	I_B	4	16		μA	$V_S = 0.4V$

† Typical values at $T_A = 25^\circ C$, $V_D = 5V$, $R_L = 10k\Omega$
 * I_{B1} and I_{B2} are measured with $V_{B1} = V_{B2} = 0V$

Electrical Characteristics Gain Setting Amplifier - Voltages are with respect to ground (VSS) unless otherwise stated, VSS= 0V.

		Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	I_{B1}	I_{B1}	I_B			100	μA	$V_S \leq V_N \leq V_D$
2	I_{B2}	I_{B2}	I_B	10			$M\Omega$	
3	I_{B3}	I_{B3}	I_B			25	μA	
4	I_{B4}	I_{B4}	I_B			1	$k\Omega$	
5	I_{B5}	I_{B5}	I_B					
6	I_{B6}	I_{B6}	I_B	40			μA	$C_L = 20p$
7	I_{B7}	I_{B7}	I_B				μA	$C_L = 20p$
8	I_{B8}	I_{B8}	I_B	0.5		$V_D - 0.5$	V	$R_L \geq 100k\Omega$, V_S
9	I_{B9}	I_{B9}	I_B			100	μA	$V_S = 0$
10	I_{B10}	I_{B10}	I_B	50			$k\Omega$	$V_O = 4V$
11	I_{B11}	I_{B11}	I_B	1.0		$V_D - 1.0$	V	$R_L = 50k\Omega$

† Typical values at $T_A = 25^\circ C$, $V_D = 5V$, $R_L = 10k\Omega$
 * I_{B1} and I_{B2} are measured with $V_{B1} = V_{B2} = 0V$

MT8888C AC Electrical Characteristics [†] - Voltages are with respect to ground (VSS) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ. [†]	Max.	Units	Notes*
1	R_X	R_X		-29		+1	μA	1,2,3,5,6
				25		69	μA	1,2,3,5,6

† Typical values at $T_A = 25^\circ C$, $V_D = 5V$, $R_L = 10k\Omega$



AC Electrical Characteristics[†] - Voltages are with respect to ground (V_{SS}) unless otherwise stated. f_C=3.579545 MHz

		Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Notes*
1	R X	$\overline{f_{CLK}}$		8	B	2,3,6,9		
2		$\overline{f_{CLK}}$		8	B	2,3,6,9		
3		$\overline{f_{CLK}}$		$\pm 1.5\%$	± 2H			2,3,5
4		$\overline{f_{CLK}}$		$\pm 3.5\%$				2,3,5
5		$\overline{f_{CLK}}$		-16	B	2,3,4,5,9,10		
6		$\overline{f_{CLK}}$		-12	B	2,3,4,5,9,10		
7		$\overline{f_{CLK}}$		22	B	2,3,4,5,9		

† At 25°C, V_{DD} = 5.0V, V_{SS} = 0V.
[‡] B = Binary, H = Hexadecimal, D = Decimal.
 * Notes: 1. See Figure 1 for test conditions.

AC Electrical Characteristics[†] - Call Progress - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Conditions
1	$\overline{f_{CLK}}$	A	310		500	H @ 25°C	
2	$\overline{f_{CLK}}$	B		20		H @ 25°C	
3	$\overline{f_{CLK}}$	H		540		H @ 25°C	
4	$\overline{f_{CLK}}$		-30			B	

† At 25°C, V_{DD} = 5.0V, V_{SS} = 0V.
[‡] B = Binary, H = Hexadecimal, D = Decimal.

AC Electrical Characteristics[†] - DTMF Reception - Typical DTMF tone accept and reject requirements. Actual values are user selectable as per Figures 5, 6 and 7.

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Conditions
1	$\overline{f_{CLK}}$	B		40		B	
2	$\overline{f_{CLK}}$	B		20		B	
3	$\overline{f_{CLK}}$	D		40		B	
4	$\overline{f_{CLK}}$	D		20		B	

† At 25°C, V_{DD} = 5.0V, V_{SS} = 0V.
[‡] B = Binary, H = Hexadecimal, D = Decimal.



AC Electrical Characteristics[†] - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Conditions
1	T O N E I N	t_{ON}	θ	3	11	14	ns	V _{DD} = 1.8V
2		t_{OFF}	θ	0.5	4	5	ns	V _{DD} = 1.8V
3		t_{R}	θ		13		μs	V _{DD} = 1.8V
4		t_{F}	θ		8		μs	V _{DD} = 1.8V
5	T O N E O U T	t_{ON}	θ	50		52	ns	V _{DD} = 1.8V
6		t_{OFF}	θ	50		52	ns	V _{DD} = 1.8V
7		t_{R}	θ	100		104	ns	V _{DD} = 1.8V
8		t_{F}	θ	100		104	ns	V _{DD} = 1.8V
9		V_{OL}	θ	-6.1		-2.1	mV	R _L = 10k Ω
10		V_{OH}	θ	-81		-4.1	mV	R _L = 10k Ω
11		P_{D}	P	0	2	3	mW	R _L = 10k Ω
12		V_{IS}	θ	-35		25	mV	
13								R _L = 10k Ω
14		f_{osc}	D		±0.7	±1.5	%	f _C = 3.5945 MHz
15		R_{D}	Ω	10		50	kΩ	
16	X T A L	f_{osc}	C	3.579 352	3.581		MHz	
17		t_{ON}	θ			110	ns	V _{DD} = 1.8V
18		D	C	40	50	60	%	V _{DD} = 1.8V
19		C	D			30	pF	

† At 25°C

‡ At 25°C

AC Electrical Characteristics[†] - MPU Interface - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Conditions
1	$\overline{\text{RD}}$	f_{osc}	θ		4.0		MHz	V _{DD} = 1.8V
2	$\overline{\text{RD}}$	t_{ON}	θ		250		ns	V _{DD} = 1.8V
3	$\overline{\text{RD}}$	t_{R}	θ			20	ns	V _{DD} = 1.8V
4	$\overline{\text{RD}}$	t_{F}	θ	23			ns	V _{DD} = 1.8V
5	$\overline{\text{RD}}$	t_{OFF}	θ	26			ns	V _{DD} = 1.8V
6	$\overline{\text{RD}}$	t_{R}	θ	22			ns	V _{DD} = 1.8V
7	$\overline{\text{RD}}$	t_{F}	θ			100	ns	V _{DD} = 1.8V
8	$\overline{\text{RD}}$	t_{OFF}	θ	150			ns	V _{DD} = 1.8V
9	$\overline{\text{RD}}$	t_{R}	θ		100		ns	V _{DD} = 1.8V
10	$\overline{\text{RD}}$	t_{F}	θ	45			ns	V _{DD} = 1.8V
11	$\overline{\text{RD}}$	t_{OFF}	θ	10			ns	V _{DD} = 1.8V
12	$\overline{\text{RD}}$	C	N		5		pF	



AC Electrical Characteristics[†]- MPU Interface (continued)- Voltages are with respect to ground (V_{SS}), unless otherwise

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Conditions
13	$\overline{RD}/\overline{WE}$	C ₀		5		pF	

[†]At V_{DD} = 5.0V, T_A = 25°C
[‡]Typical values are at V_{DD} = 5.0V, T_A = 25°C

Notes:

1. $\overline{RD}/\overline{WE}$ is 600 nS
2. $\overline{RD}/\overline{WE}$ is 1.6 nS
3. $\overline{RD}/\overline{WE}$ is 10 nS
4. $\overline{RD}/\overline{WE}$ is 1.6 nS
5. $\overline{RD}/\overline{WE}$ is 1.6 nS
6. $\overline{RD}/\overline{WE}$ is $\pm 1.5\% \pm 2$ nS
7. $\overline{RD}/\overline{WE}$ is 1.6 nS
8. $\overline{RD}/\overline{WE}$ is 1.6 nS (±2%).
9. $\overline{RD}/\overline{WE}$ is 1.6 nS
10. $\overline{RD}/\overline{WE}$ is 1.6 nS
11. $\overline{RD}/\overline{WE}$ is 1.6 nS

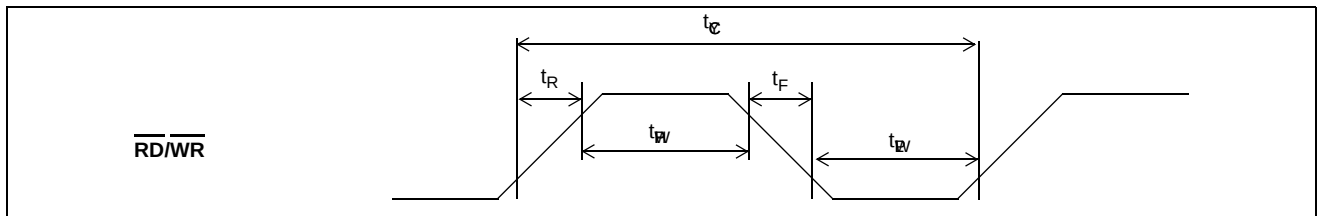


Figure 18 - RD/WR Clock Pulse

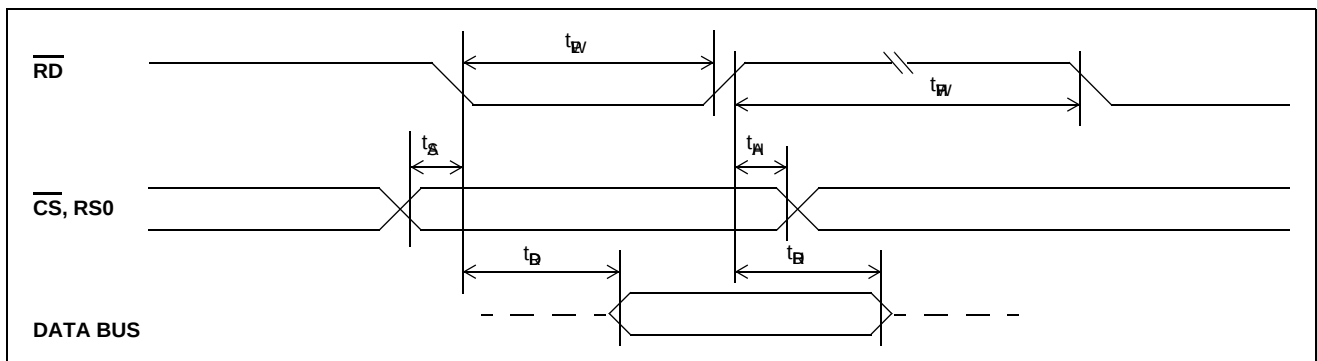


Figure 19 - 8031/8051/8085 Read Timing Diagram

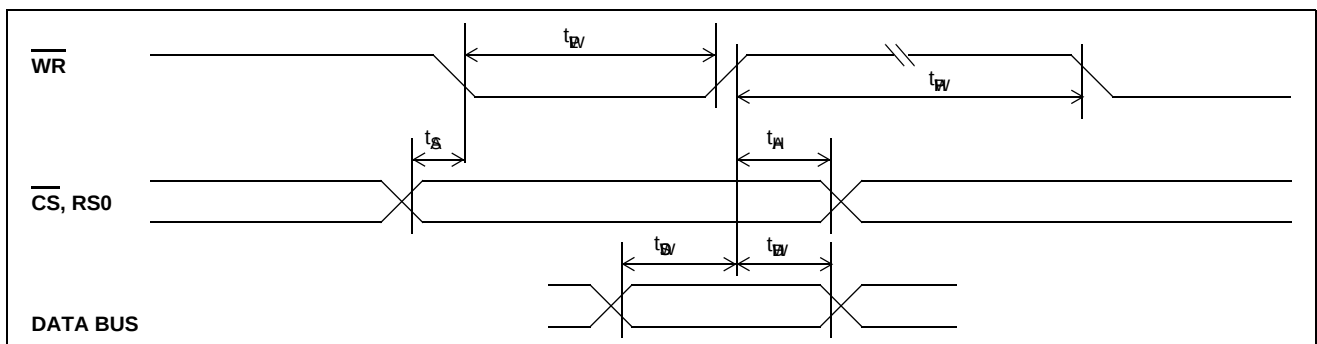
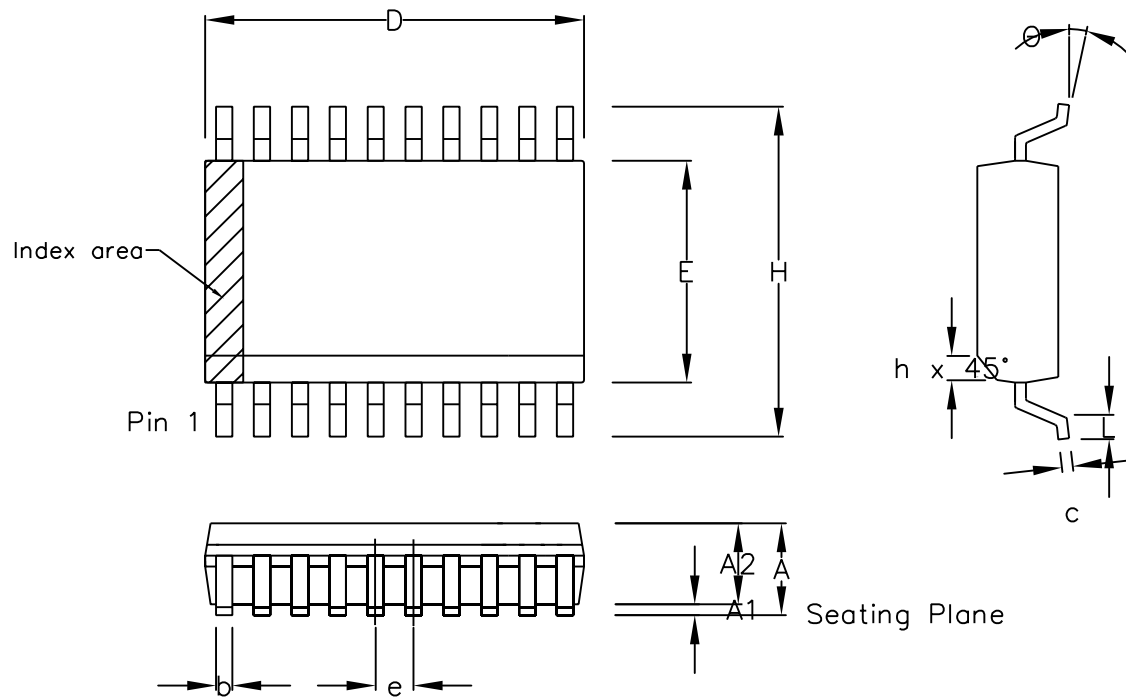


Figure 20 - 8031/8051/8085 Write Timing Diagram





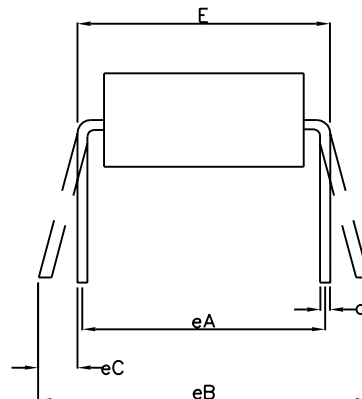
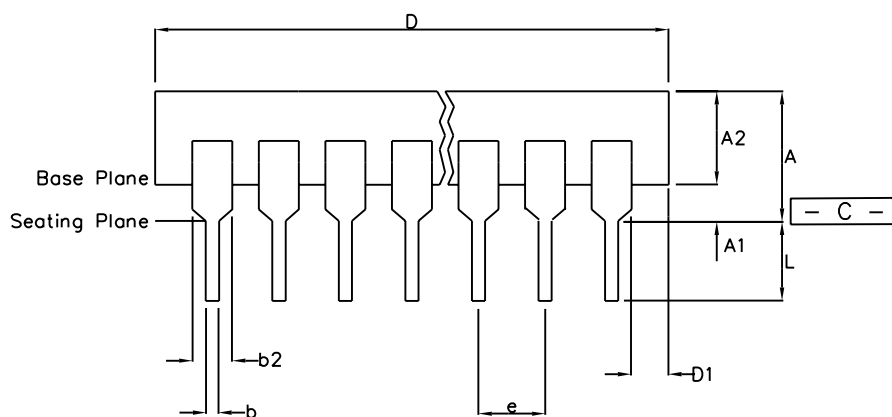
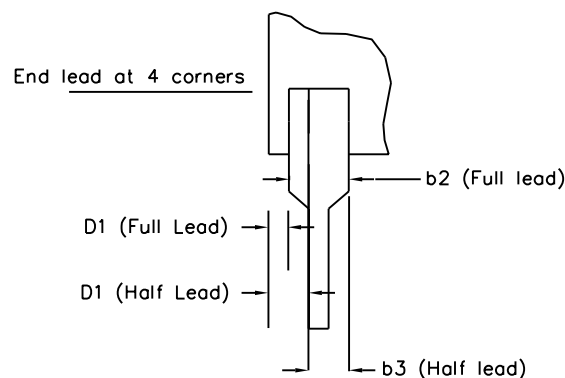
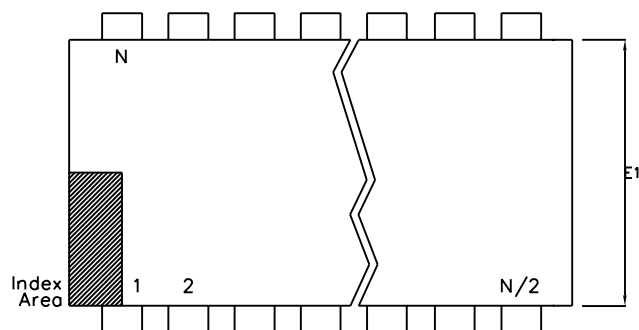
Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches		
	MIN	Nominal	MAX	MIN	Nominal	MAX
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2	2.25		2.35	0.089		0.092
D	12.60		13.00	0.496		0.512
H	10.00		10.65	0.394		0.419
E	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
e	1.27 BSC.			0.050 BSC.		
b	0.33		0.51	0.013		0.020
c	0.23		0.32	0.009		0.013
θ	0°		8°	0°		8°
h	0.25		0.75	0.010		0.029
	Pin features					
N	20					
Conforms to JEDEC MS-013AC Iss. C						

Notes:

1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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ISSUE	1	2	3		Previous package codes MP / S	Package Outline for 20 lead SOIC (0.300" Body Width)
ACN	6746	201941	213098			
DATE	7Apr95	27Feb97	15Jul02			GPD00015
APPRD.						





	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	24.89	26.92	0.980	1.060
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54	BSC	0.100	BSC
eA	7.62	BSC	0.300	BSC
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	20		20	
Conforms to Jedec MS-001AD Issue D				

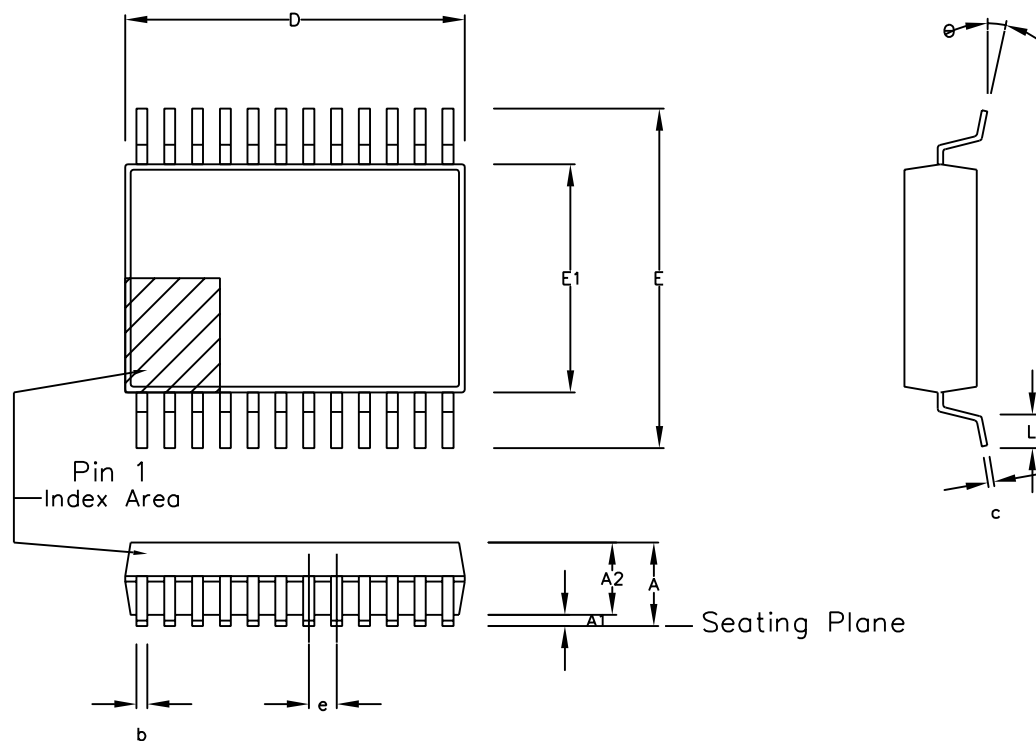
Notes:

- Dimensions D, D1 & E1 do not include mould flash or protrusions.
- Dimensions E & eA are measured with leads constrained to be perpendicular to datum $\text{--- } \bar{C} \text{ ---}$
- Dimensions eB & eC are measured with the leads unconstrained
- Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
- N is the maximum of terminal positions.

This drawing supersedes: -
UK drawing # 418/ED/39502/005

© Zarlink Semiconductor 2002 All rights reserved.					Package Code DA	
ISSUE	1	2			Previous package codes DP / E	Package Outline for 20 lead PDIP
ACN	202562	213107				
DATE	9Jun97	15Jul02				GPD00347
APPRD.						





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches		
	MIN	Nominal	MAX	MIN	Nominal	MAX
A	1.70		2.00	0.067		0.079
A1	0.05		0.20	0.002		0.008
A2	1.65		1.85	0.065		0.073
D	7.90		8.50	0.311		0.335
E	7.40		8.20	0.291		0.323
E1	5.00		5.60	0.197		0.220
L	0.55		0.95	0.022		0.037
e	0.65 BSC.			0.026 BSC.		
b	0.22		0.38	0.009		0.015
c	0.09		0.25	0.004		0.010
θ	0°		8°	0°		8°
	Pin features					
N	24					
Conforms to JEDEC MO-150 AG Iss. B						

This drawing supersedes: –
418/ED/51481/003 (UK)

Notes:

1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

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ISSUE	1	2	3		Previous package codes	Package Outline for 24 lead SSOP (5.3mm Body Width)
ACN	201934	205233	213104		NP / N	
DATE	27Feb97	25Sep98	15Jul02			
APPRD.						GPD00295





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