Integrated DTMF Transceiver with Intel Micro Interface

Features

- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]-30 [illegible]

Applications

- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]

Description

[illegible]

Ordering Information

[illegible] 20 [illegible]
[illegible] 20 [illegible]
[illegible] 24 [illegible]
[illegible] 28 [illegible]
[illegible] 20 [illegible]
[illegible] 20 [illegible]
[illegible] 24 [illegible]
[illegible] 28 [illegible]
[illegible] 28 [illegible]
[illegible] 20 [illegible]
[illegible] 20 [illegible] T
[illegible] 28 [illegible]

*[illegible]

-40°C to +85°C

[illegible]

[illegible]

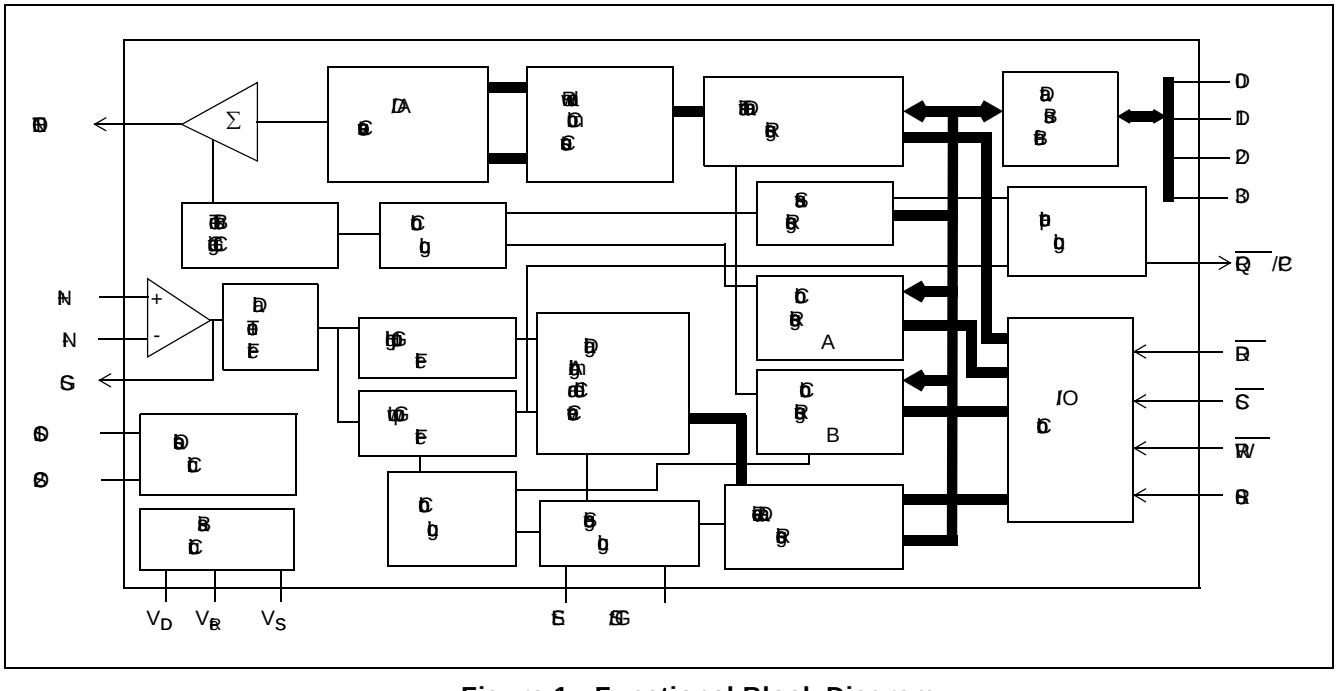


Figure 1 - Functional Block Diagram

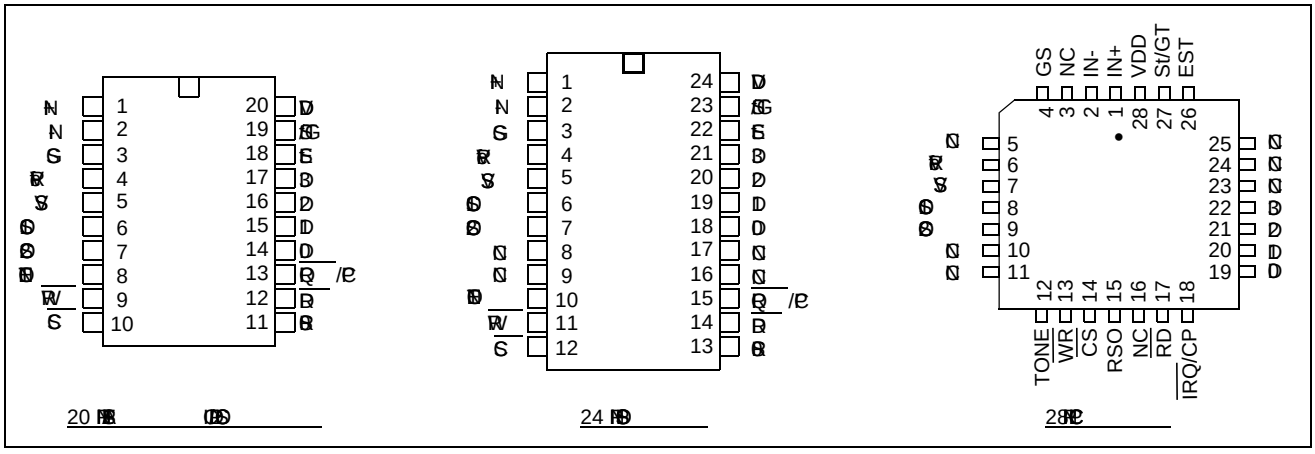


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
20	24	28		
1	1	1		**Non-inverting**
2	2	2		**Inverting**
3	3	4		**Gain Select.**
4	4	6		**Reference Voltage** (V /2).
5	5	7		(0 V).
6	6	8		4.7 M Ω
7	7	9		**Oscillator** 3.579545
8	10	12		
9	11	13		**Write**
10	12	14		**Chip Select** 14.
11	13	15		**Register Select**
12	14	17		**Read**
13	15	18	/CP	**Interrupt Request/Call Progress**
14-17	18-21	19-22	D0-3	**Microprocessor Data Bus.** =1 =1.

Pin Description (continued)

Pin #			Name	Description
20	24	28		
18	22	26		**Early Steering**
19	23	27		**Steering Input/Guard Time**
20	24	28	V_D	
	8,9 16,17	3,5,10, 11,16, 23,25		

1.0 Functional Description

2.0 Input Configuration

3.0 Receiver Section

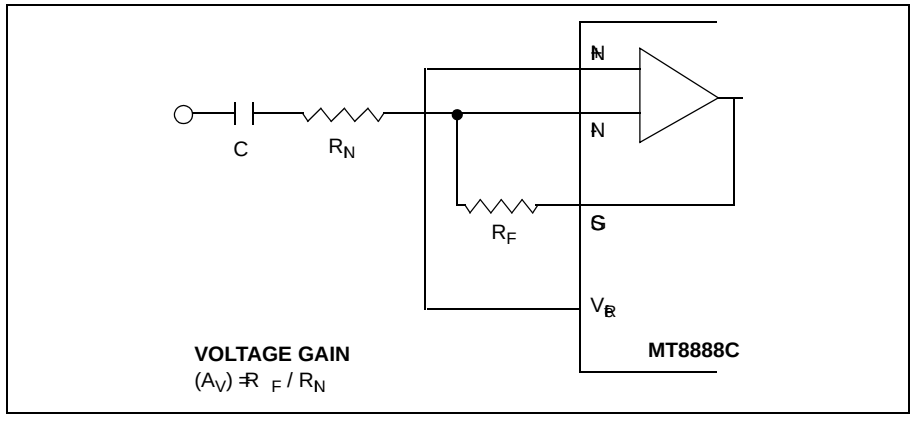


Figure 3 - Single-Ended Input Configuration

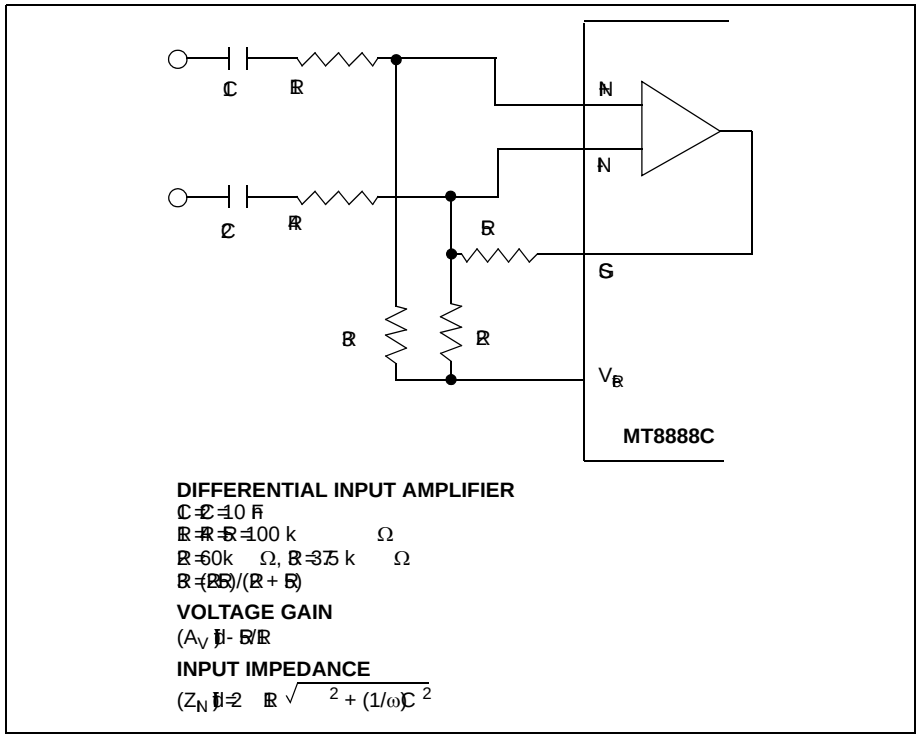


Figure 4 - Differential Input Configuration

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	147	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	147	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	147	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	147	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

Table 1 - Functional Encode/Decode Table

4.0 Steering Circuit

[illegible]

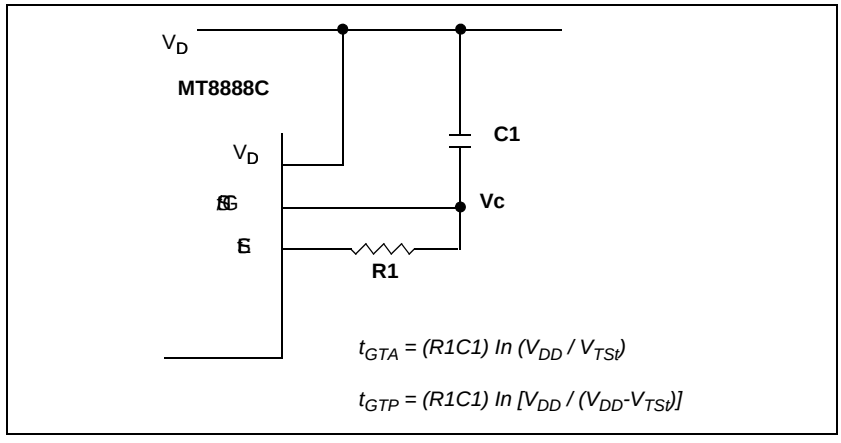


Figure 5 - Basic Steering Circuit

5.0 Guard Time Adjustment

[illegible]

$$t_{REC} \geq t_{DPmax} + t_{GTPmax} - t_{DAmin}$$

$$t_{\overline{REC}} \leq t_{DPmin} + t_{GTPmin} - t_{DAmax}$$

$$t_{ID} \geq t_{DAmax} + t_{GTAmax} - t_{DPmin}$$

$$t_{DO} \leq t_{DAmin} + t_{GTAmin} - t_{DPmax}$$

[illegible]

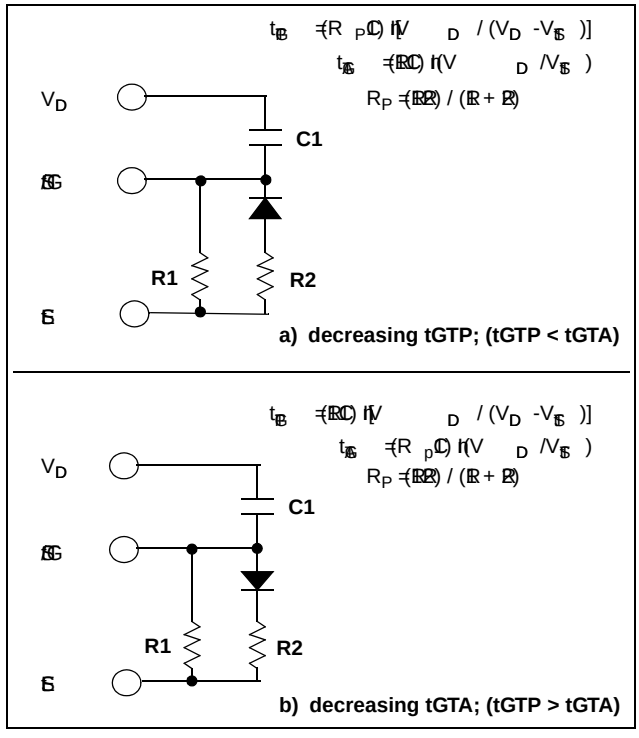


Figure 6 - Guard Time Adjustment

6.0 Call Progress Filter

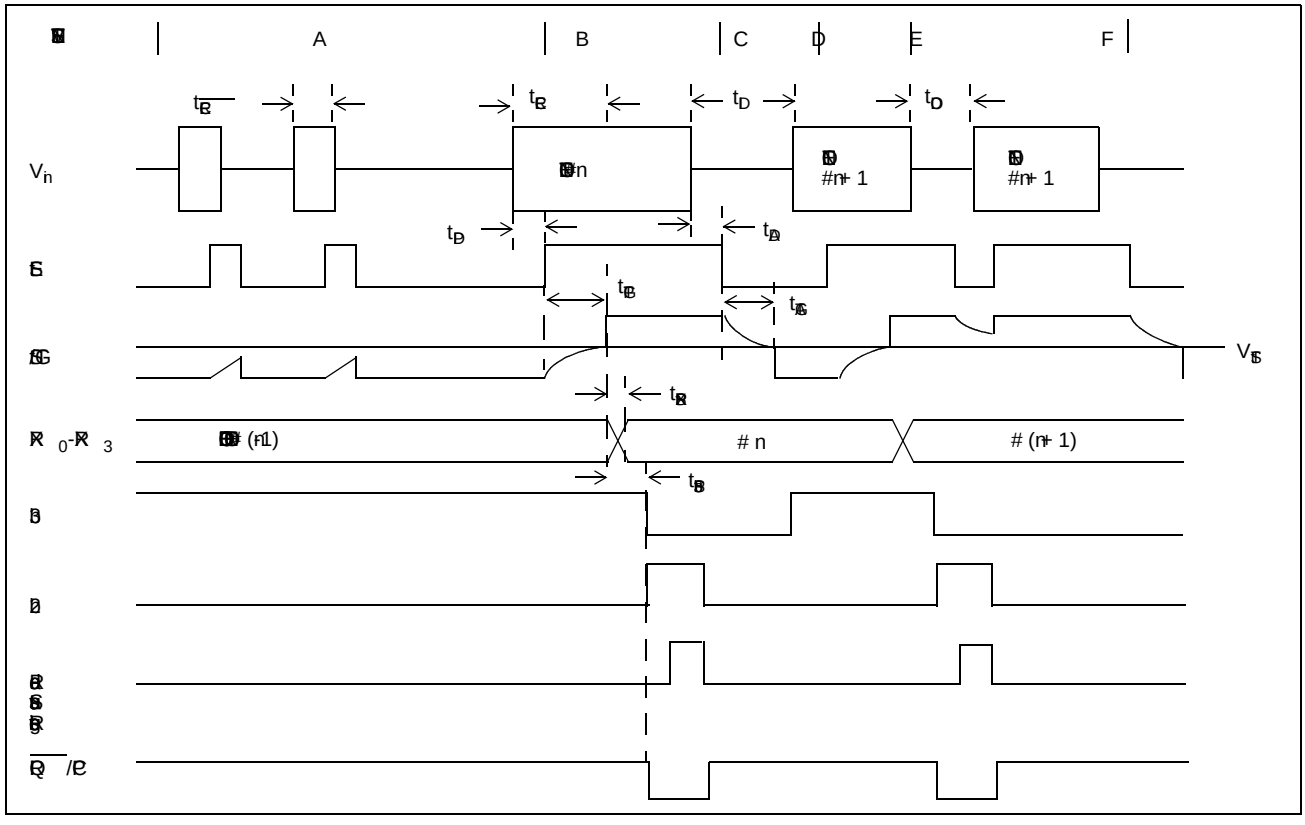


Figure 7 - Receiver Timing Diagram

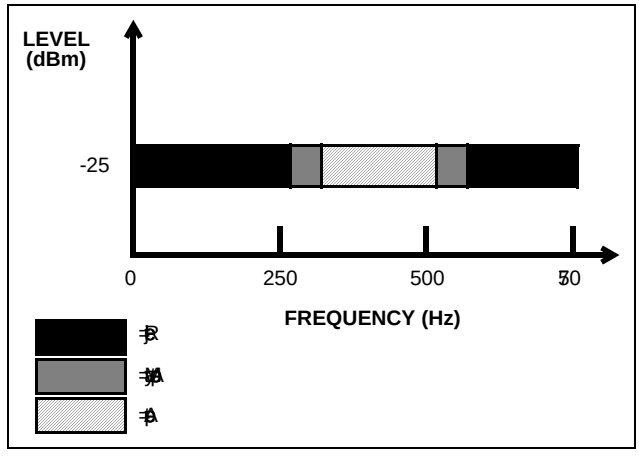


Figure 8 - Call Progress Response

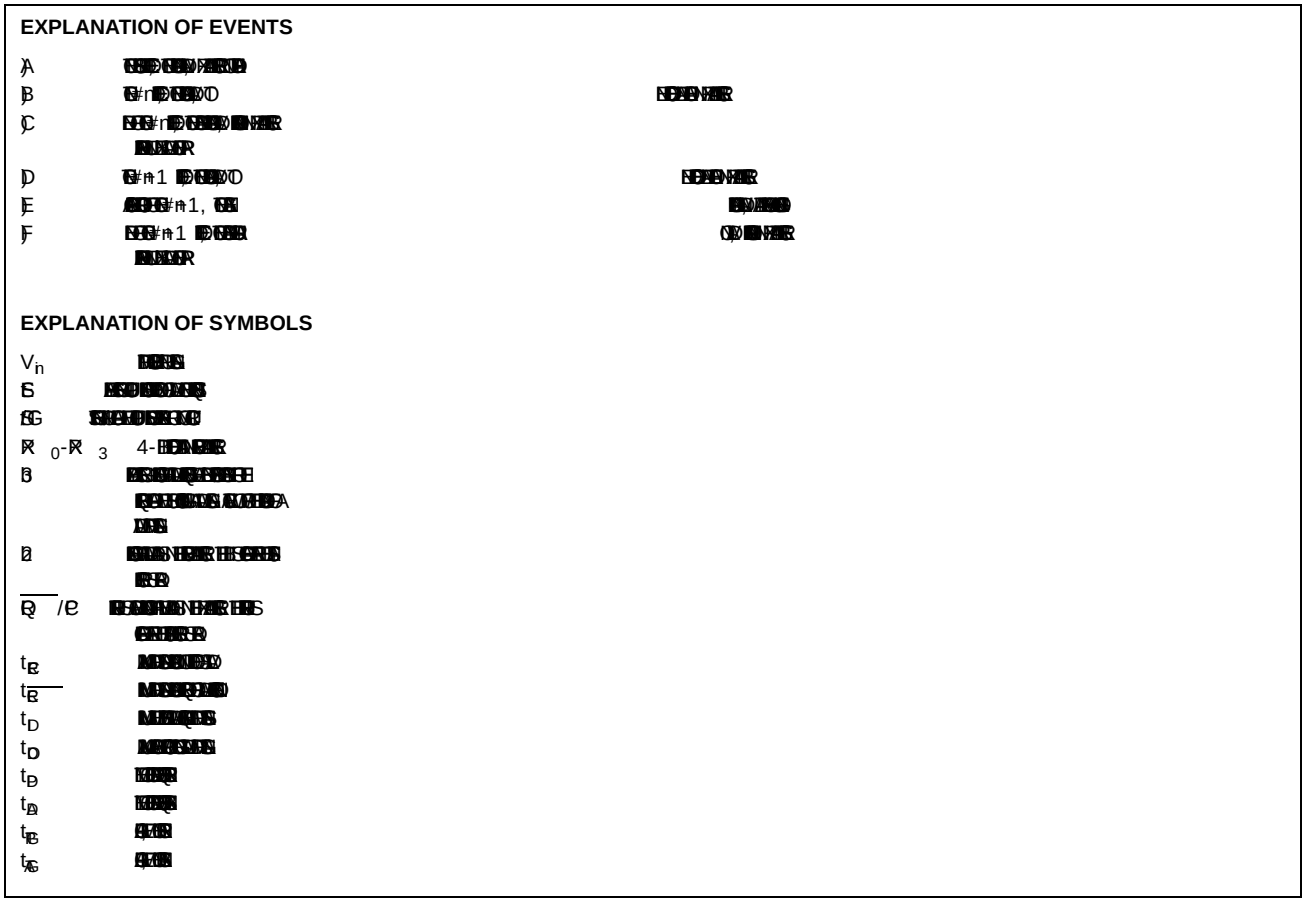


Figure 9 - Description of Timing Events

7.0 DTMF Generator

[illegible]

[illegible]

[illegible]

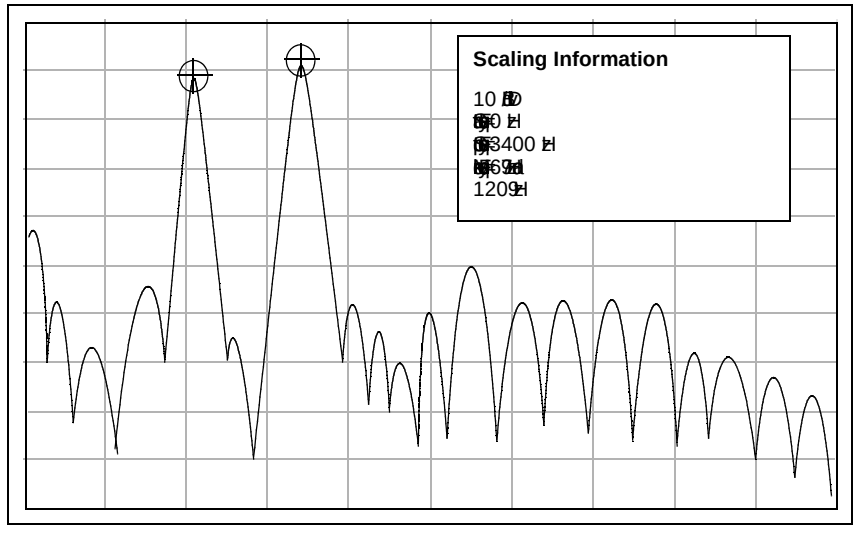


Figure 10 - Spectrum Plot

8.0 Burst Mode

±1 µs

±2 s

not

9.0 Single Tone Generation

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	697	691	+0.30
L2	770	766.2	-0.49
L3	852	847	-0.54
L4	941	948	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	147	147.9	-0.35
H4	1633	1645.0	+0.73

Table 2 - Actual Frequencies Versus Standard Requirements

10.0 Distortion Calculations

single tone

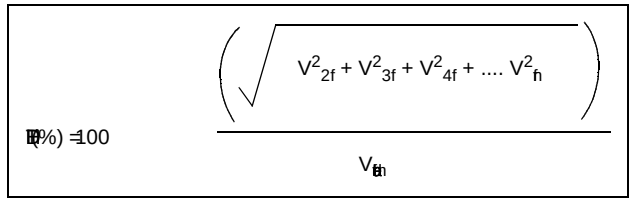


Figure 11 - Equation 1. THD (%) For a Single Tone

dual tone

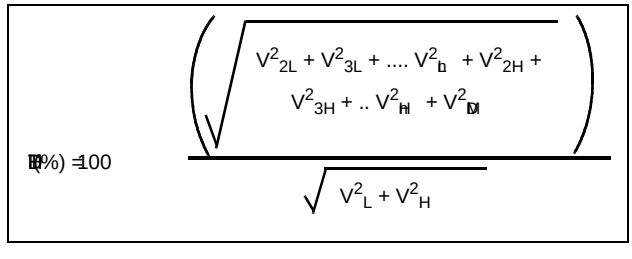


Figure 12 - Equation 2. THD (%) For a Dual Tone

11.0 DTMF Clock Circuit

3.579545 MHz

±0.1%

150 Ω

2 mW

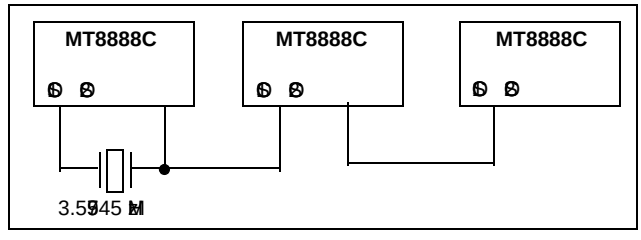


Figure 13 - Common Crystal Connection

12.0 Microprocessor Interface

RS0	$\overline{WR}$	$\overline{RD}$	FUNCTION
0	0	1	[illegible]
0	1	0	[illegible]
1	0	1	[illegible]
1	1	0	[illegible]

Table 3 - Internal Register Functions

b3	b2	b1	b0
[illegible]	[illegible]	[illegible]	[illegible]

Table 4 - CRA Bit Positions

b3	b2	b1	b0
[illegible]	[illegible]	[illegible]	[illegible]

Table 5 - CRB Bit Positions

BIT	NAME	DESCRIPTION
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

Table 6 - Control Register A Description

BIT	NAME	DESCRIPTION
0		
1		
2		
3		

Table 7 - Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
0			
1			
2			
3			

Table 8 - Status Register Description

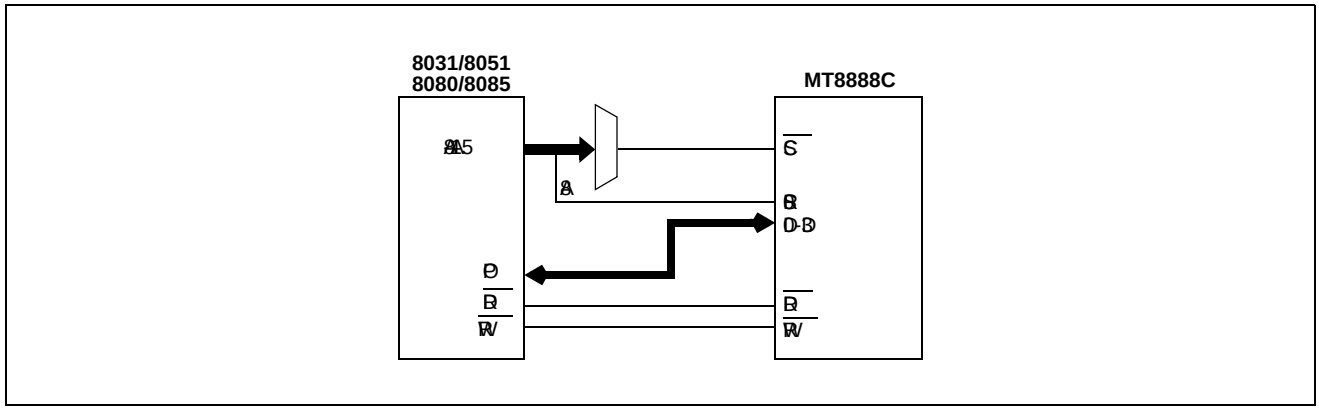


Figure 14 - MT8888C Interface Connections for Various Intel Micros

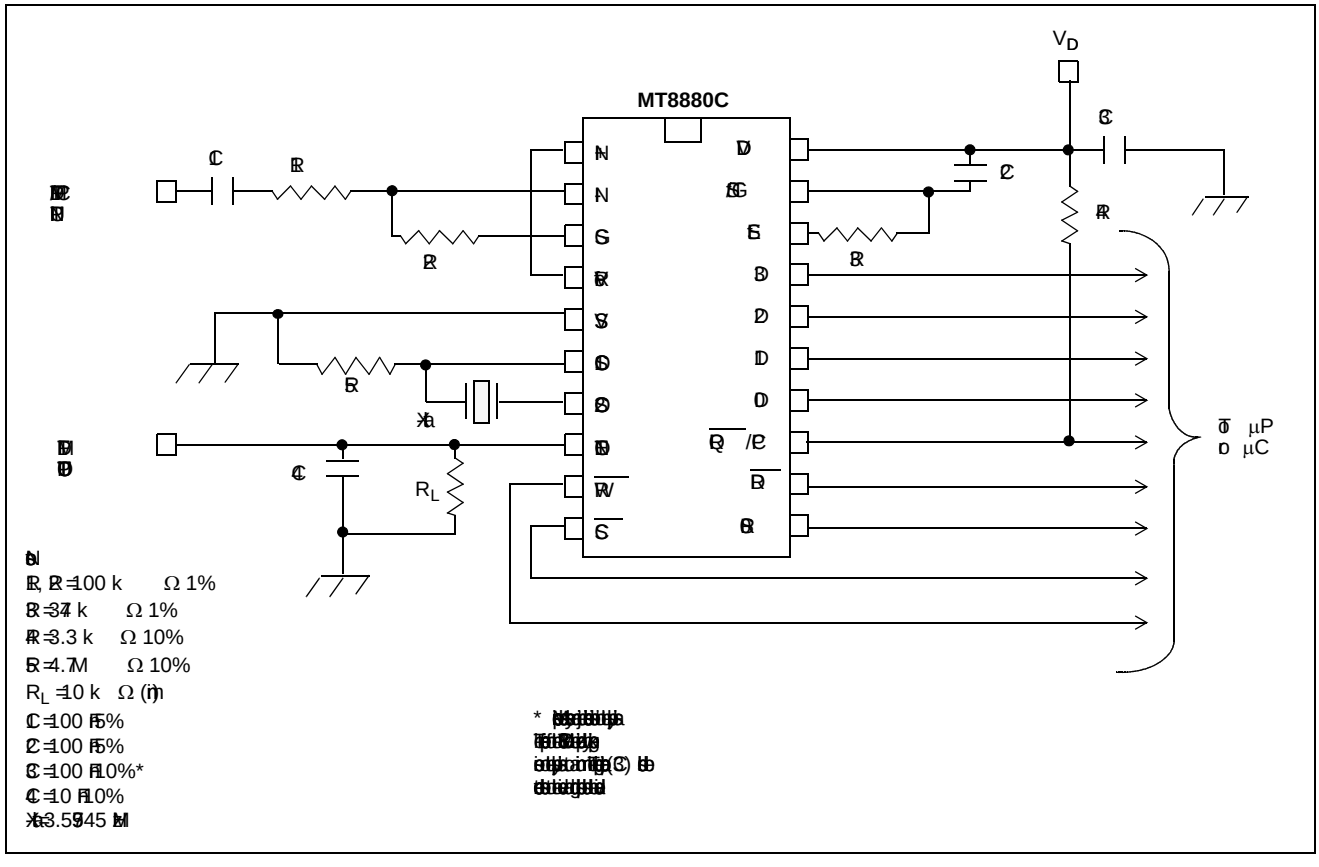
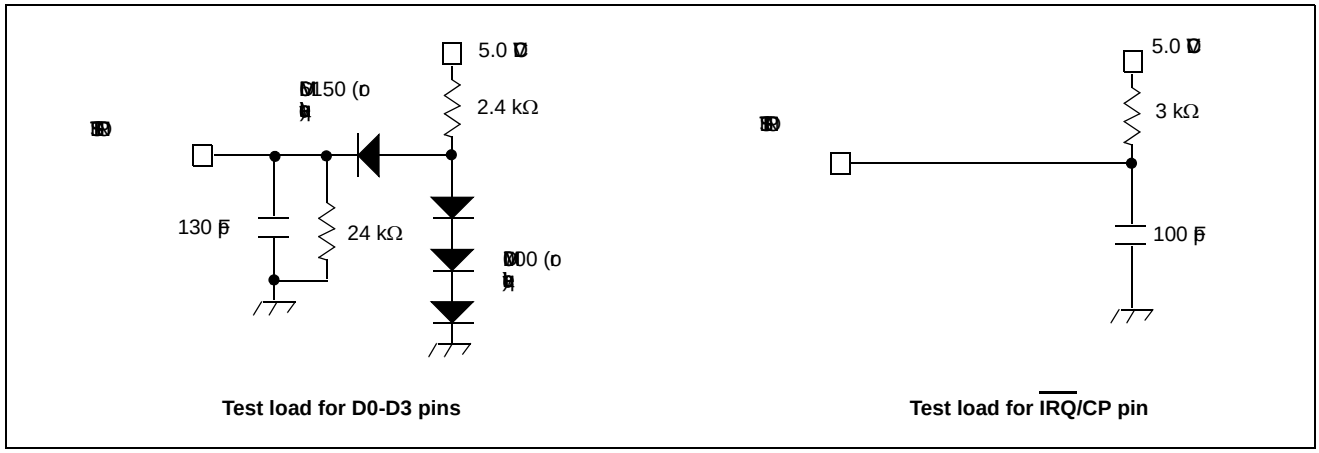


Figure 15 - Application Circuit (Single-Ended Input)



Test load for D0-D3 pins

Test load for $\overline{IRQ}$/CP pin

Figure 16 - Test Circuits

INITIALIZATION PROCEDURE

Description:

	Control RS0	WR	RD	Data b3	b2	b1	b0
1)	1	1	0	X	X	X	X
2)	1	0	1	0	0	0	0
3)	1	0	1	0	0	0	0
4)	1	0	1	1	0	0	0
5)	1	0	1	0	0	0	0
6)	1	1	0	X	X	X	X

TYPICAL CONTROL SEQUENCE FOR BURST MODE APPLICATIONS

Sequence:

	RS0	$\overline{WR}$	$\overline{RD}$	b3	b2	b1	b0
1)	1	0	1	1	1	0	1
2)	1	0	1	0	0	0	0
3)	0	0	1	0	1	1	1
4)							
5)	1	1	0	X	X	X	X
	0	0	1	0	1	0	1
	0	1	0	X	X	X	X
	0	1	0	X	X	X	X
	0	0	1	0	1	0	1

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (±2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 17 - Application Notes

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	D -VS	VD		6	V
2	V	I	VS -0.3	VD +0.3	V
3	VS)			10	mA
4	T	S	-65	+150	°C
5	P	D		1000	mW

* g

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	V	D	4.75	5.00	5.25	V	
2	T	O	-40		+85	°C	
3	f	C	3.5705	3.5945	3.5124	MHz	

‡ 25 °C

DC Electrical Characteristics - † - VS V

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUP	V	D	4.75	5.0	5.25	V	
2		I	D		7.0	11	mA	
3		P	C			57.8	mW	
4	INPUTS	(5)	VIH	3.5			V	
5		(5)	VD			1.5	V	
6		V	T	2.2	2.3	2.5	V	V D 5V
7	OUTPUTS	(8) V	O			0.1	V	
8		(8) V	H	4.9			V	
9		I	Z		1	10	µA	V 2.4 V
10		V V	R	2.4	2.5	2.6	V	V D 5V
11		V R	R		1.3		kΩ	
12	Digital	V	L			0.8	V	
13		V	H	2.0			V	
14		I	Z			10	µA	V N V S V D
15		I	H	-1.4	-6.6		mA V	2.4V
16		I	D	2.0	4.0		mA V	0.4V

DC Electrical Characteristics (continued) - † - V_S [illegible]

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
17	[illegible]	[illegible] I	[illegible]	-0.5	-3.0		[illegible]	V [illegible] 4.6V
18	[illegible]	[illegible] I	D	2	4		[illegible]	V_D [illegible].4V
19	[illegible] / [illegible]	[illegible] I	D	4	16		[illegible]	V_D [illegible].4V

† [illegible]
‡ [illegible] 25 °C, V_D 5V [illegible]
* [illegible]

Electrical Characteristics Gain Setting Amplifier - Voltages are with respect to ground (VSS) unless otherwise stated, VSS= 0V.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	[illegible] I	N			100	[illegible]	$V_S \le V_N \le V_D$
2	[illegible] R	N	10			MΩ	
3	[illegible] V	[illegible]			25	[illegible]	
4	[illegible] R 50		[illegible]		1 [illegible]		
5	[illegible] 40	[illegible]					
6	[illegible] A	[illegible]	40			[illegible]	C_L = 20p
7	[illegible] 1.0		[illegible]		C		L = 20p
8	[illegible] V	O	0.5		V_D -0.5	V	$R_L \ge$ 100 kΩ [illegible] V_S
9	[illegible] C	L			100	[illegible]	[illegible] °
10	[illegible] R	L	50			kΩ	V_O = [illegible]
11	[illegible] V	[illegible]	1.0		V_D -1.0	V	R_L = 50k Ω

[illegible]
[illegible]

MT8888C AC Electrical Characteristics † - **Voltages are with respect to ground (V_{SS}) unless otherwise stated.**

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	R	[illegible] ([illegible]		-29		+1	[illegible]	1,2,3,5,6
	X	[illegible]		27.5		[illegible] 89	[illegible] [illegible]	1,2,3,5,6

† [illegible] [illegible] 15.

AC Electrical Characteristics † **- Voltages are with respect to ground (V_{SS}) unless otherwise stated. f_C=3.579545 MHz**

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	RX	[illegible]		8	[illegible]	2,3,6,9		
2		[illegible]		8	[illegible]	2,3,6,9		
3		[illegible]		±1.5%± 2Hz			2,3,5	
4		[illegible]		±3.5%				2,3,5
5		[illegible]		-16	[illegible]	2,3,4,5,9,10		
6		[illegible]		-12	[illegible]	2,3,4,5,7,9,10		
7		[illegible]		22	[illegible]	2,3,4,5,8,9		

†[illegible]
‡[illegible] 25 °C, V_D = 5 V, [illegible]
* *[illegible]

AC Electrical Characteristics† **- Call Progress** **- Voltages are with respect to ground (V_{SS}), unless otherwise stated.**

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	[illegible] f	A	310		500	Hz	@25 [illegible]
2	[illegible] f	R		20		Hz	@25 [illegible]
3	[illegible] f	R		540		Hz	@25 [illegible]
4	[illegible]		-30			[illegible]	

†[illegible]
‡[illegible] 25 °C, V_D = 5 V, [illegible]

AC Electrical Characteristics †**- DTMF Reception - Typical DTMF tone accept and reject requirements. Actual values are user selectable as per Figures 5, 6 and 7.**

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	[illegible] t	R		40		ms	
2	[illegible] t	R		20		ms	
3	[illegible] t	D		40		ms	
4	[illegible] t	D		20		ms	

†[illegible]
‡[illegible] 25 °C, V_D = 5 V, [illegible]

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	TONE IN	t		3	11	14		
2		t		0.5	4	5		
3		t			13		µs	
4		0-R 3			8		µs	
5	TONE OUT	t		50		52		
6		t		50		52		
7		t		100		104		
8		t		100		104		
9		V		-6.1		-2.1	R	R_L 10k Ω
10		V		-8.1		-4.1	R	R_L 10k Ω
11			P	0	2	3	R	R_L 10k Ω
12				-35		25		
13								R_L 10k Ω
14		f	D		±0.7	±1.5	%	f_C 3.579545
15		R		10		50	kΩ	
16	XTAL	f	C	3.579 3.579 3.581				
17		t				110		
18			C	40	50	60	%	
19		C				30		

†
‡ 25 °C

AC Electrical Characteristics† - MPU Interface - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	/ f			4.0			
2	/ t			250			
3	/	t_R t_F			20		
4	t		23				& 20
5	t		26				& 20
6	t		22				& 20
7	t				100		& 20
8	, t		150				& 20
9	, t			100			& 20
10	t		45				& 20
11	t		10				& 20
12	C			5			

AC Electrical Characteristics† **- MPU Interface (continued)-** **Voltages are with respect to ground (V_{SS}), unless otherwise**

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
13	[illegible]	[illegible]		5		[illegible]	

†[illegible]
‡[illegible] °C, V_D = 5 V, [illegible]

Notes:

1. [illegible]
2. [illegible]
3. [illegible]
4. [illegible]
5. [illegible]
6. [illegible] ± 1.5%, ±2 [illegible]
7. [illegible]
8. [illegible] ±2%).
9. [illegible]
10. [illegible]
11. [illegible]

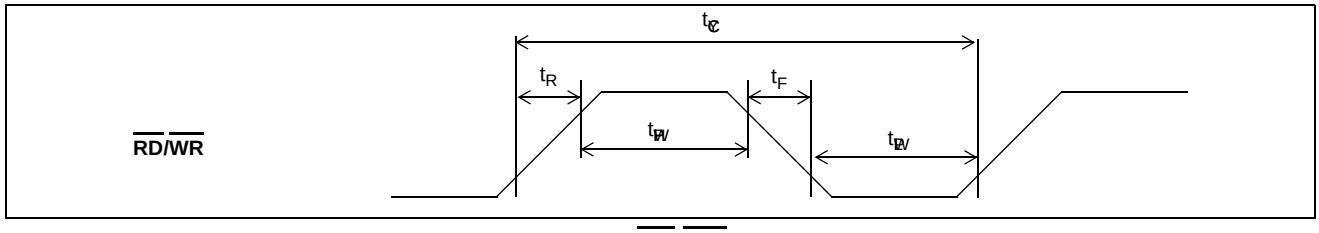


Figure 18 - $\overline{RD}/\overline{WR}$ Clock Pulse

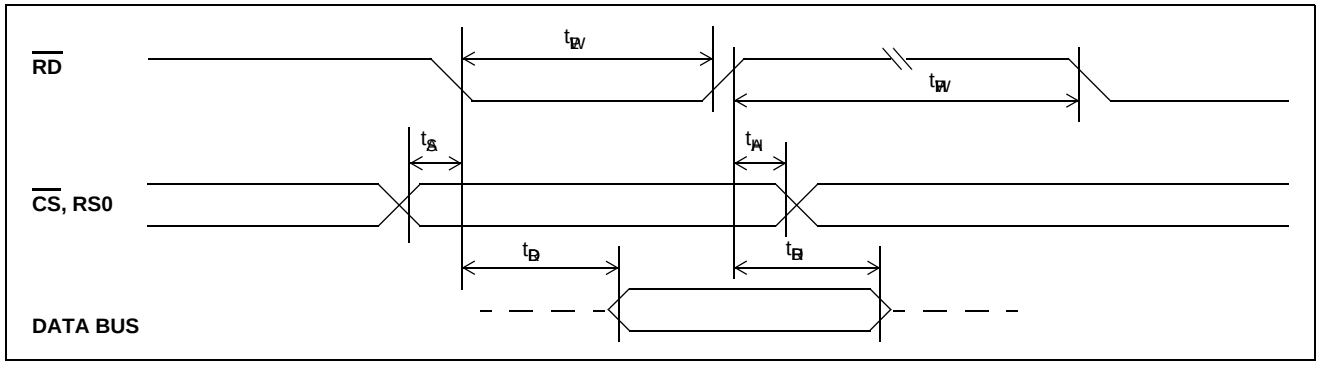


Figure 19 - 8031/8051/8085 Read Timing Diagram

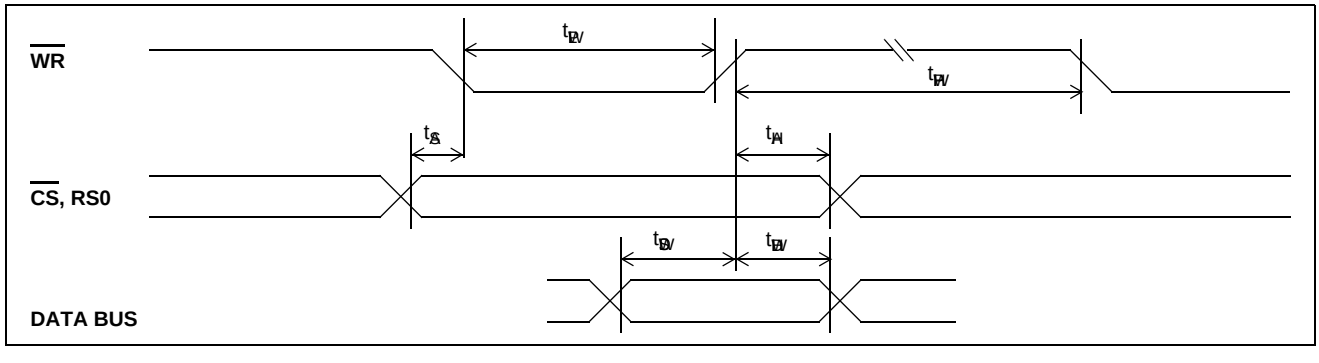
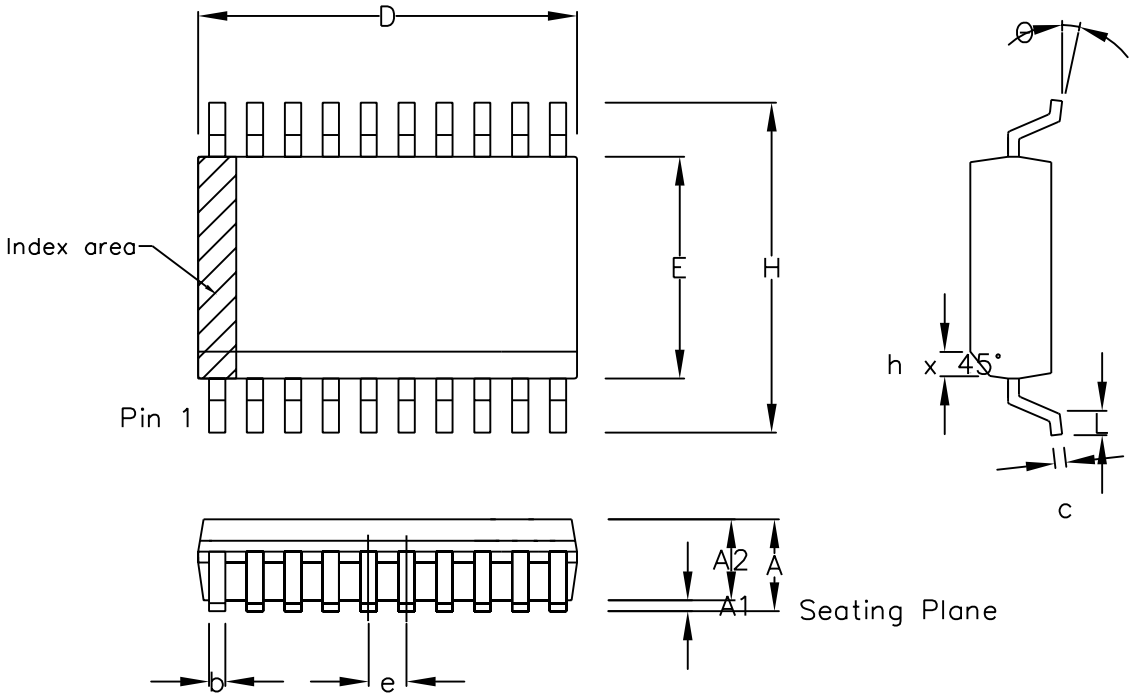


Figure 20 - 8031/8051/8085 Write Timing Diagram



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	12.60		13.00		0.496		0.512
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	20						
Conforms to JEDEC MS-013AC Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201941	213098	
DATE	7Apr95	27Feb97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

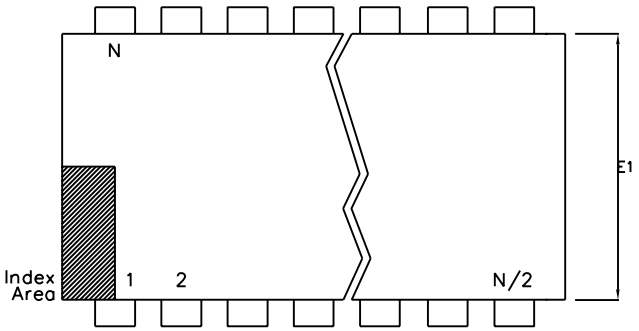
Previous package codes

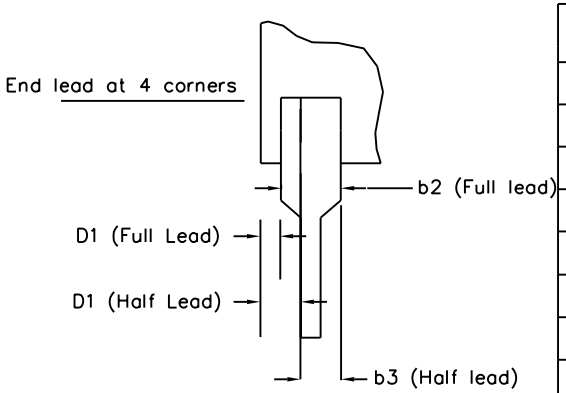
MP / S

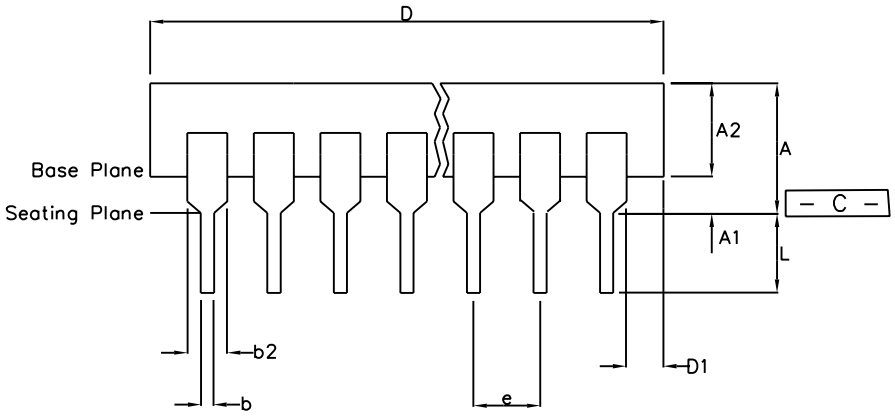
Package Code DC

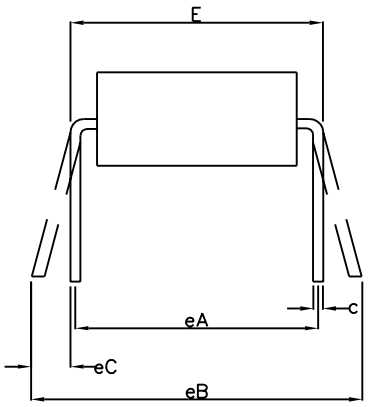
Package Outline for 20 lead SOIC (0.300" Body Width)

GPD00015









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	24.89	26.92	0.980	1.060
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	20		20	
Conforms to Jedec MS-001AD Issue D				

Notes:
1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
3. Dimensions eB & eC are measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

This drawing supersedes: –
UK drawing # 418/ED/39502/005

ISSUE	1	2		
ACN	202562	213107		
DATE	9Jun97	15Jul02		
APPRD.				

ZARLINK SEMICONDUCTOR

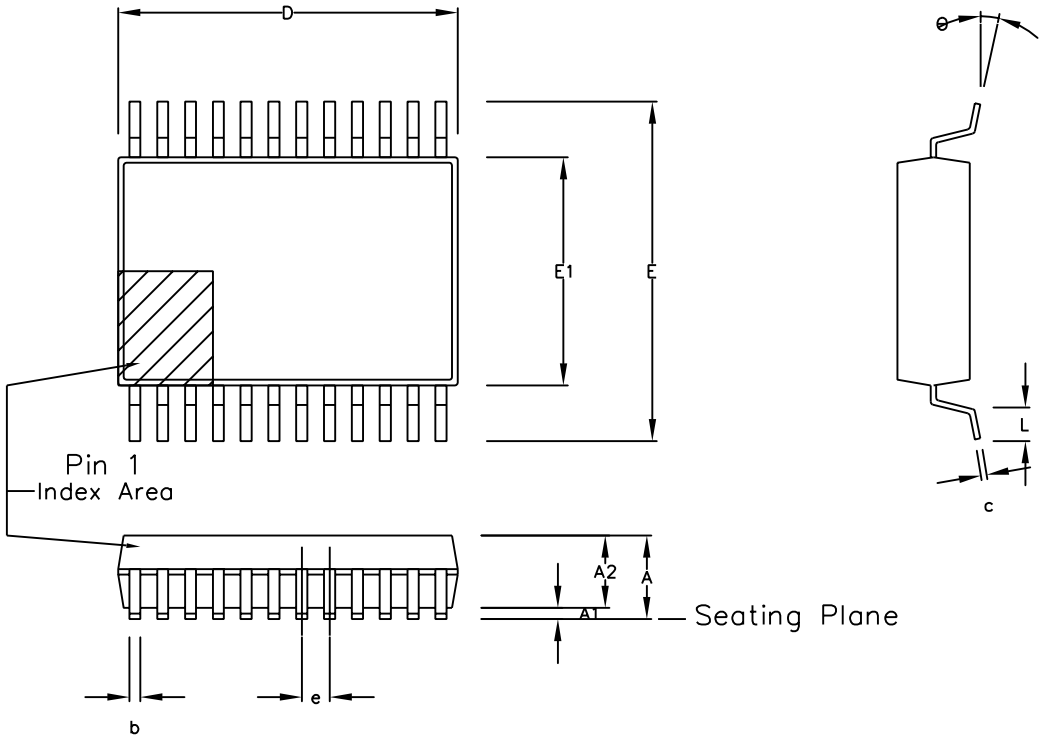
Previous package codes

DP / E

Package Code DA

Package Outline for 20 lead PDIP

GPD00347



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	7.90		8.50		0.311		0.335
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	24						
Conforms to JEDEC MO-150 AG Iss. B							

This drawing supersedes:-
418/ED/51481/003 (UK)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201934	205233	213104	
DATE	27Feb97	25Sep98	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for
24 lead SSOP
(5.3mm Body Width)

GPD00295

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www.zarlink.com

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