SY89831U

Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator with Internal Termination Precision Edge®

Features

- Guaranteed AC Performance over Temperature and Voltage
  - DC to 2.5 GHz throughput (Typical)
  - 350 ps Propagation Delay (IN-to-Q, Typical)
  - 5 ps within Device Skew (Typical)
  - 150 ps Rise/Fall Time (Typical)
- Ultra-low Jitter Design
  - 62 fs RMS Phase Jitter (Typical)
- Unique Patent-Pending Input Termination and VT Pin Accepts DC- and AC-coupled Differential Inputs
- 800 mV, 100K LVPECL Typical Output Swing
- Power Supply 2.5V ±5% or 3.3V ±10%
- Industrial Temperature Range: –40°C to +85°C
- Available in 3 mm × 3 mm 16-lead VQFN Package

Applications

- Processor Clock Distribution
- SONET Clock Distribution
- Fibre Channel Clock Distribution
- Gigabit Ethernet Clock Distribution

General Description

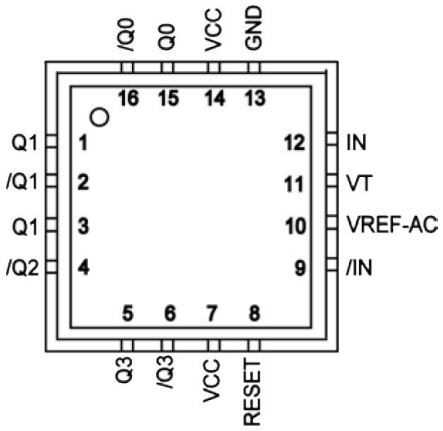
The SY89831UMG is a high-speed, 2 GHz differential LVPECL 1:4 fanout buffer optimized for ultra-low skew applications.

Within-device skew is guaranteed to be less than 20 ps (5 ps typical) over supply voltage and temperature. The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF-AC reference output is included for AC-coupled applications.

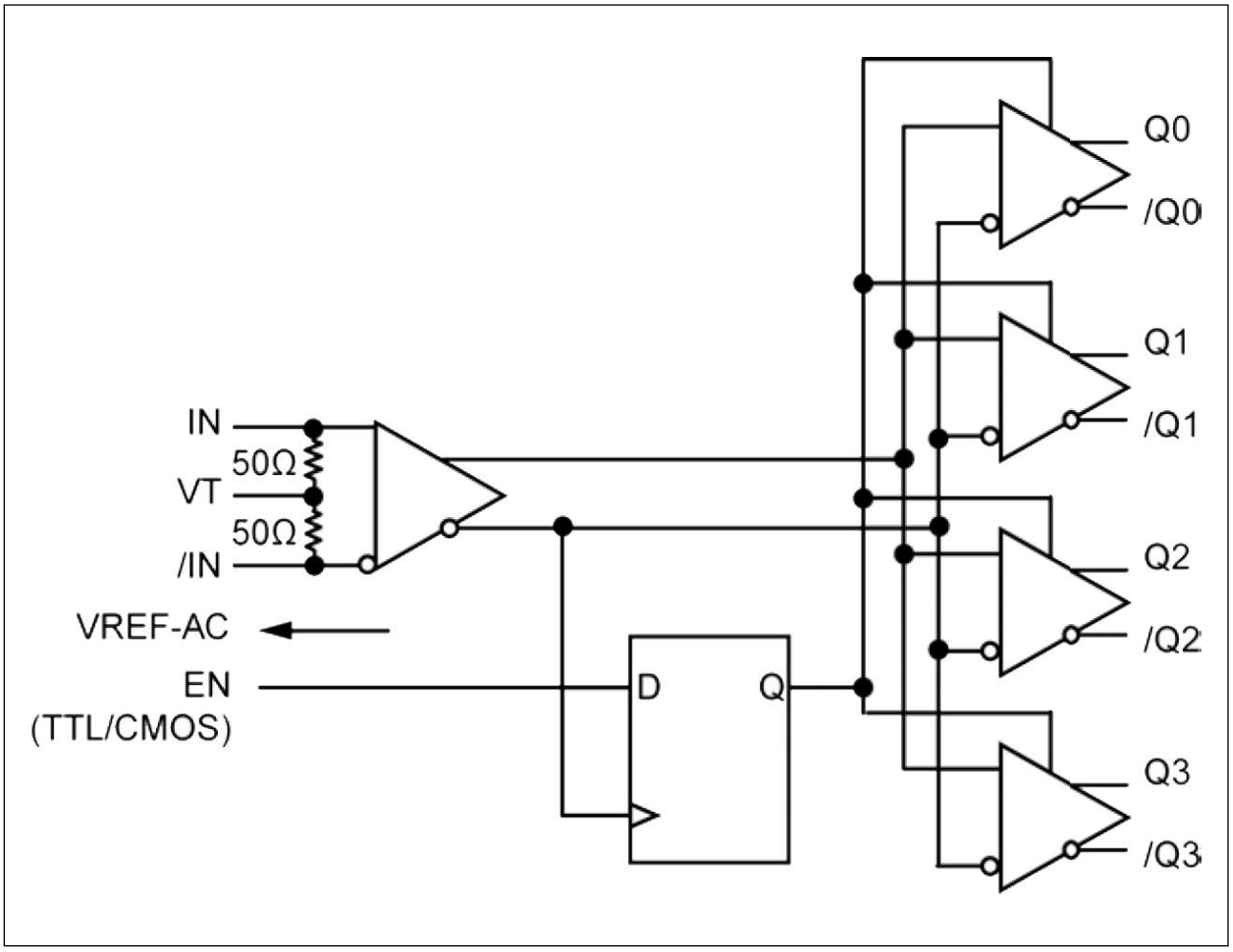
The SY89831UMG is a part of Microchip's high-speed clock synchronization family. For applications that require a different I/O combination, consult Microchip's website at www.microchip.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.

Package Type

SY89831U
16-Lead VQFN



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.5V
Continuous LVPECL Output Current (I_{OUT}) ..... 50 mA
Surge LVPECL Output Current (I_{OUT}) ..... 100 mA
Input Current, Source or Sink Current on (IN, /IN) ..... ±50 mA
VREF-AC Current, Source or Sink Current on (VT) ..... ±2 mA

Operating Ratings††

Supply Voltage Range ..... +2.37V to +3.6V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

All values applicable for when T_A = –40°C to +85°C unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply	V_{CC}	2.375	—	2.625	V	—
		3.0	—	3.6		
Power Supply Current	I_{CC}	—	47	70	mA	No load, max. V_{CC}
Input Resistance (IN to VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN to /IN)	$R_{DIFF-IN}$	90	100	110	Ω	—
Input HIGH Voltage (IN, /IN)	V_{IH}	1.2	—	V_{CC}	V	—
Input LOW Voltage (IN, /IN)	V_{IL}	0	—	V_{IH} – 0.1	V	—
Input Voltage Swing (IN, /IN)	V_{IN}	0.1	—	1.7	V	See Figure 6-1
Differential Input Voltage Swing |IN – /IN|	V_{DIFF_IN}	0.2	—	—	V	See Figure 6-2
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	—

Note 1: The circuit is designed to meet the DC specifications shown in this table after thermal equilibrium has been established.

TABLE 1-2: LVTTL/LVCMOS INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.375V to 3.60V; V_{EE} = 0V; T_A = –40°C to +85°C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input HIGH Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input LOW Voltage	V_{IL}	0	—	0.8	V	—
Input HIGH Current	I_{IH}	–125	—	20	µA	—
Input LOW Current	I_{IL}	–300	—	—	µA	—

TABLE 1-3: LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output HIGH Voltage (Q, /Q)	V_{OH}	V_{CC} – 1.145	—	V_{CC} – 0.895	V	—
Output LOW Voltage (Q, /Q)	V_{OL}	V_{CC} – 1.945	—	V_{CC} – 1.695	V	—
Output Voltage Swing (Q, /Q)	V_{OUT}	550	800	—	mV	See Figure 6-1
Differential Output Voltage Swing (Q, /Q)	V_{DIFF_OUT}	1100	1600	—	mV	See Figure 6-2

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-4: LVTTL/LVCMOS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input HIGH Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input LOW Voltage	V_{IL}	0	—	0.8	V	—
Input HIGH Current	I_{IH}	–125	—	30	µA	—
Input LOW Current	I_{IL}	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-5: AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to + 85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Frequency	f_{MAX}	2.0	2.5	—	GHz	V_{OUT} ≥ 450 mV
Propagation Delay IN to Q	t_{pd}	—	390	—	ps	V_{IN} ≥ 100 mV
		250	350	450		V_{IN} ≥ 800 mV
Within-Device Skew	t_{SKEW}	—	5	20	ps	Note 2
Part-to-Part Skew	t_{SKEW}	—	—	150	ps	Note 3
Set-up Time EN to IN, /IN	t_S	300	—	—	ps	Note 4
Hold Time EN to IN, /IN	t_H	300	—	—	ps	Note 4
RMS Phase Jitter	t_{JITTER}	—	62	—	fs	Output = 622 MHz, Integration Range 12 kHz–20 MHz
Output Rise/Fall Times (20% to 80%)	t_r, t_f	70	150	225	ps	At full output swing
Duty Cycle	α	48	50	52	%	Freq. < 630 MHz

Note 1: High-frequency AC parameters are guaranteed by design and characterization.

2: Within-device skew is measured between two different outputs under identical input transitions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

4: Set-up and hold times apply to synchronous applications that will enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

TABLE 1-6: TEMPERATURE SPECIFICATIONS

Note 1						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance (Note 1)						
Still Air	θ_{JA}	—	+60	—	°C/W	—
Junction to Board	θ_{JA}	—	+32	—	°C/W	—

Note 1: Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. The Ψ_{JB} and θ_{JA} values are determined for a 4-layer board at the still-air package thermal resistance, unless otherwise stated.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
15, 16	Q0, /Q0	Differential 100K LVPECL Outputs: These LVPECL outputs are the precision, low-skew copies of the inputs. Please refer to the “Truth Table” section for details. Unused output pairs may be left open. Terminate with 50Ω to VCC – 2V. See the “Output Termination Recommendations” section for more details.
1, 2	Q1, /Q1	
3, 4	Q2, /Q2	
5, 6	Q3, /Q3	
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable only occurs when the outputs are in a logic low state. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic high state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signs as small as 100 mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs default to an intermediate state if left open. Please refer to the “Input Interface Applications” section for more details.
10	VREF-AC	Reference Voltage: These outputs bias to VCC – 1.4V. They are used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect VREF-AC to the VT pin and bypass with a 0.01 µF low-ESR capacitor to VCC. See the “Input Interface Applications” section for more details. Maximum sink/source current is ±1.5 mA. Due to the limited drive capability, each VREF-AC pin should only drive its respective VT pin. If VREF-AC is used with a 2.5V supply, make sure the input swing is large enough to comply with the VIH min. spec.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See the “Input Interface Applications” section for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1 µF/0.01 µF low-ESR capacitors placed as close as possible to each VCC pin.

TABLE 2-2: TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0 (Note 1)	1 (Note 1)

Note 1: On the next negative transition of the input signal (IN).

3.0 TYPICAL PHASE NOISE

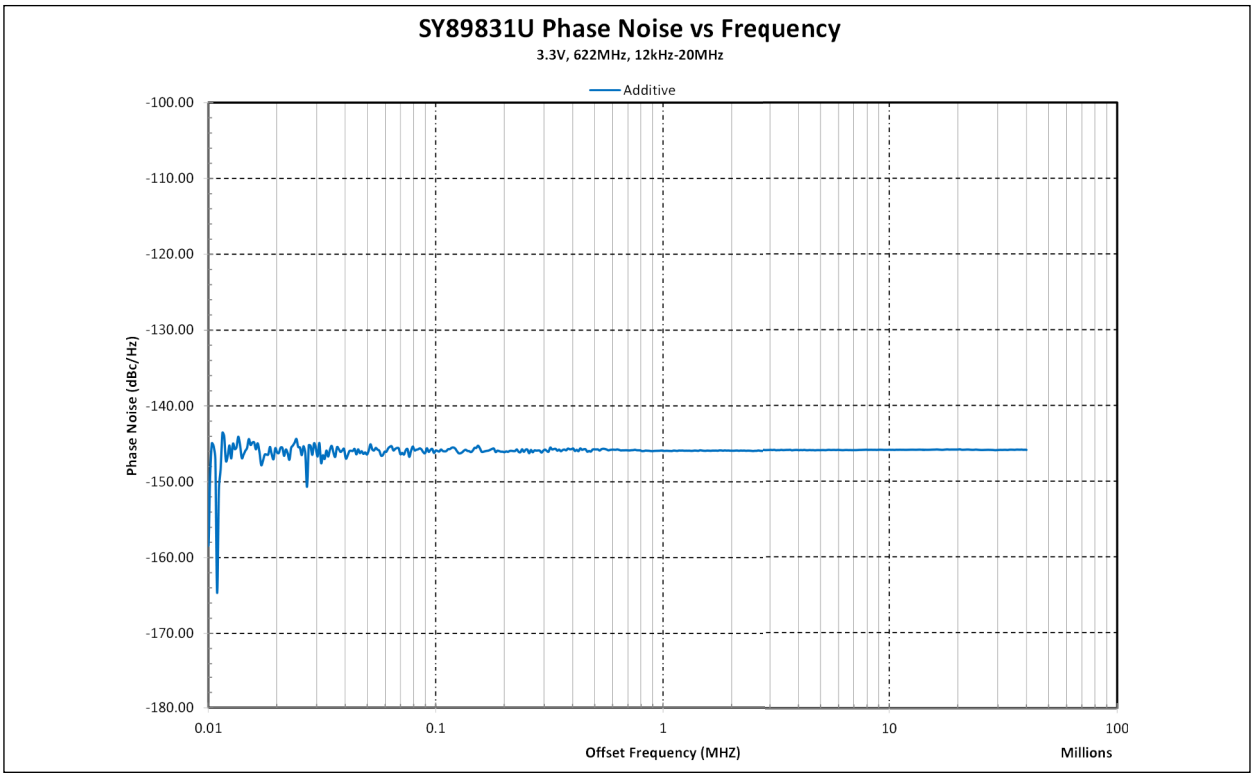


FIGURE 3-1: SY89831U PHASE NOISE VS. FREQUENCY: 3.3V, 622 MHZ, 12 KHZ-20 MHZ.

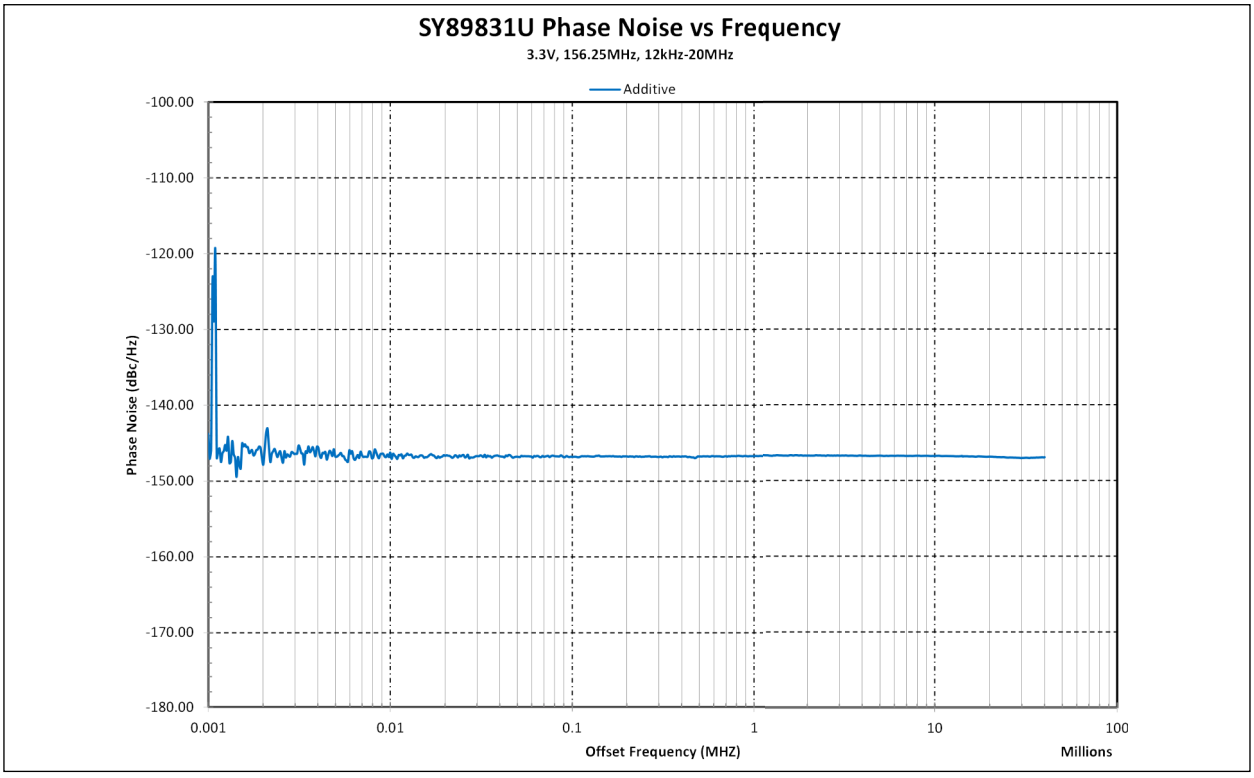


FIGURE 3-2: SY89831U PHASE NOISE VS. FREQUENCY: 3.3V, 156.25 MHZ, 12 KHZ-20 MHZ.

4.0 TYPICAL CHARACTERISTICS

V_{CC} = 3.3V; GND = 0V; R_L = 50Ω to V_{CC} – 2V; T_A = 25°C, unless otherwise noted.

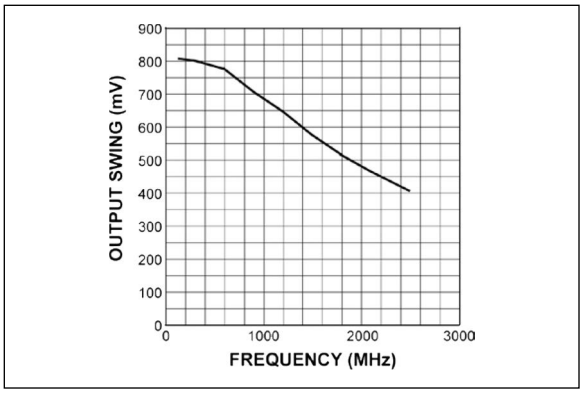


FIGURE 4-1: OUTPUT SWING VS. FREQUENCY.

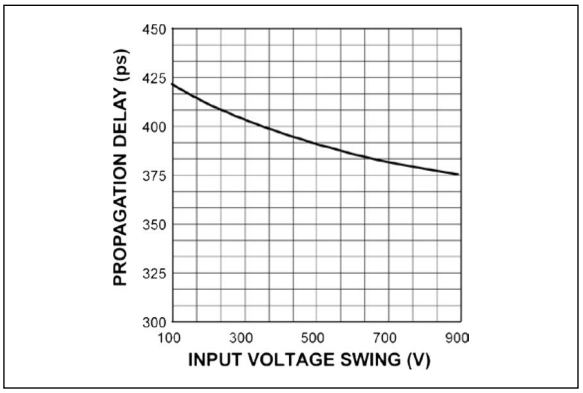


FIGURE 4-3: PROPAGATION DELAY VS. INPUT VOLTAGE SWING.

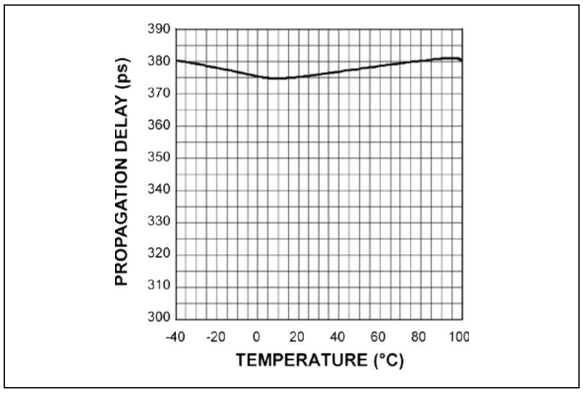


FIGURE 4-2: PROPAGATION DELAY VS. TEMPERATURE.

5.0 TYPICAL OUTPUT WAVEFORMS

V_{CC} = 3.3V; GND = 0V; V_{IN} = 800 mV; R_L = 50Ω to V_{CC} − 2V; T_A = 25°C, unless otherwise noted.

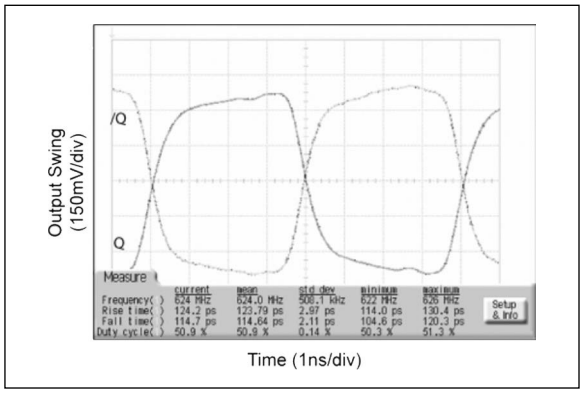


FIGURE 5-1: 155 MHZ OUTPUT.

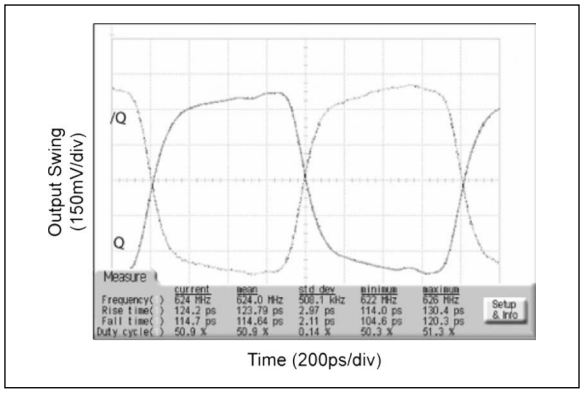


FIGURE 5-2: 622 MHZ OUTPUT.

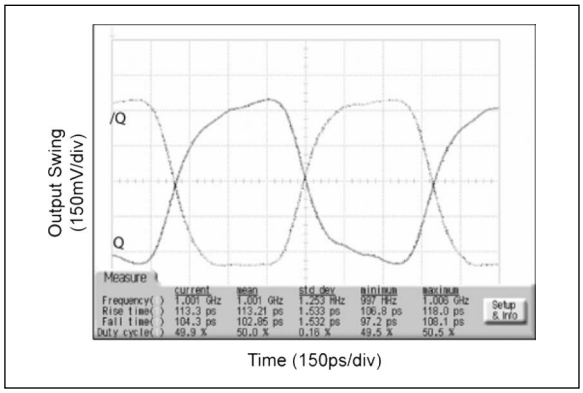


FIGURE 5-3: 1 GHZ OUTPUT.

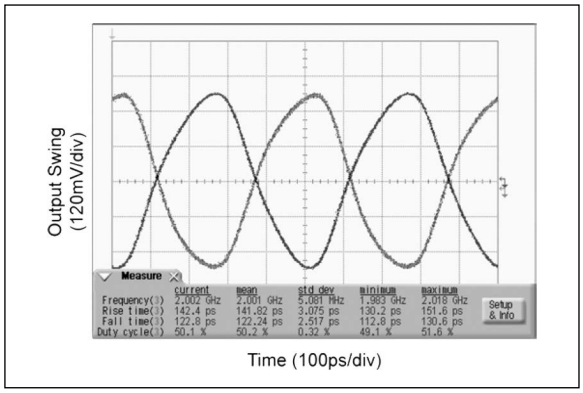


FIGURE 5-4: 2 GHZ OUTPUT.

6.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

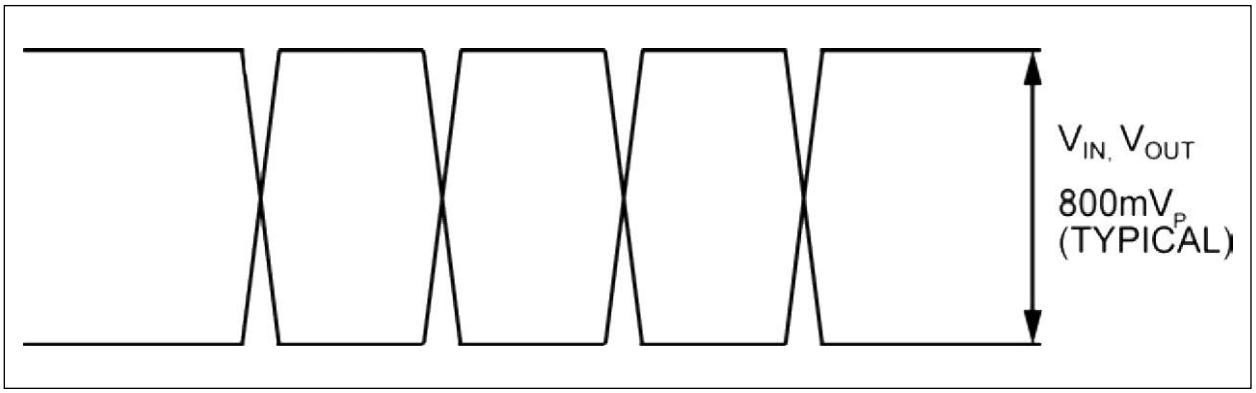


FIGURE 6-1: SINGLE-ENDED SWING.

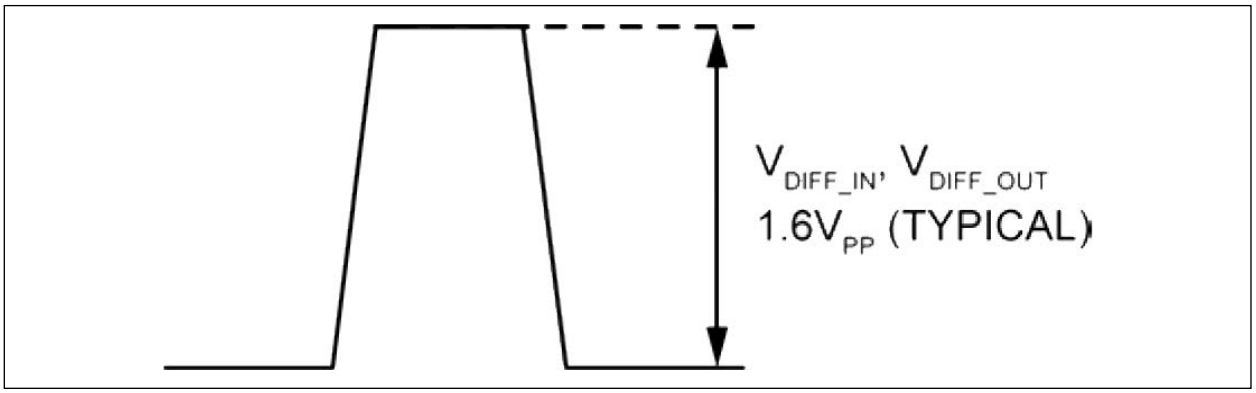


FIGURE 6-2: DIFFERENTIAL SWING.

7.0 INPUT AND OUTPUT STAGES

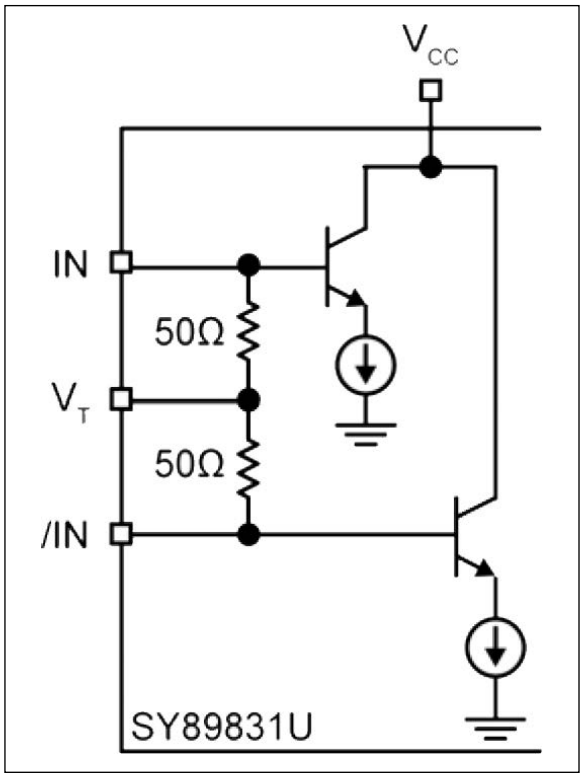


FIGURE 7-1: SIMPLIFIED DIFFERENTIAL.

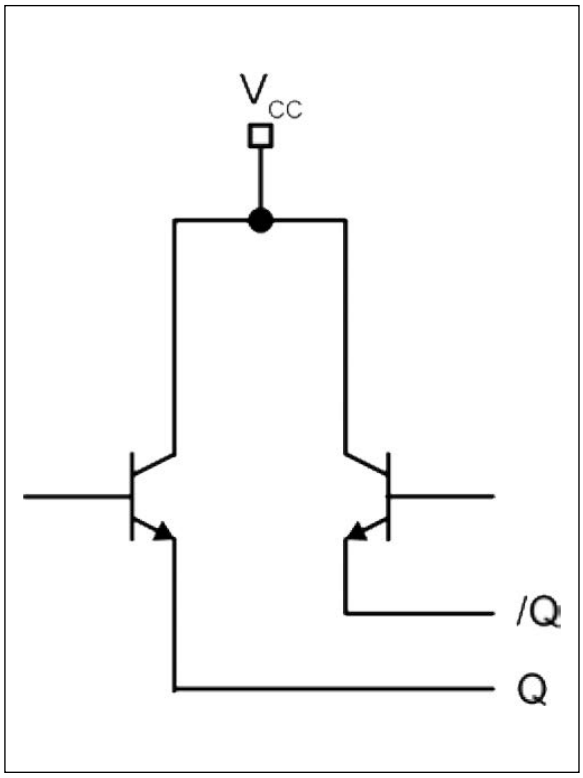


FIGURE 7-2: SIMPLIFIED LVPECL OUTPUT STAGE.

8.0 INPUT INTERFACE APPLICATIONS

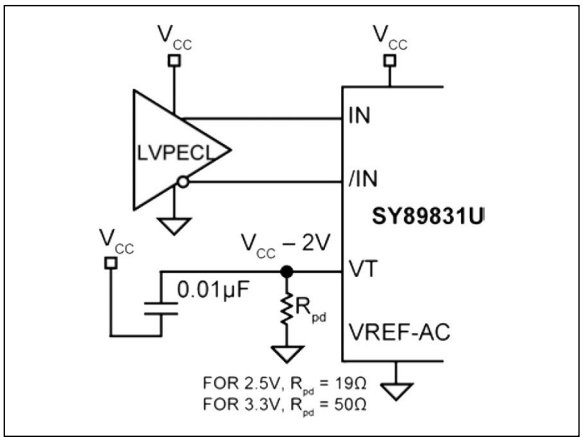


FIGURE 8-1: DC-COUPLED LVPECL INPUT INTERFACE.

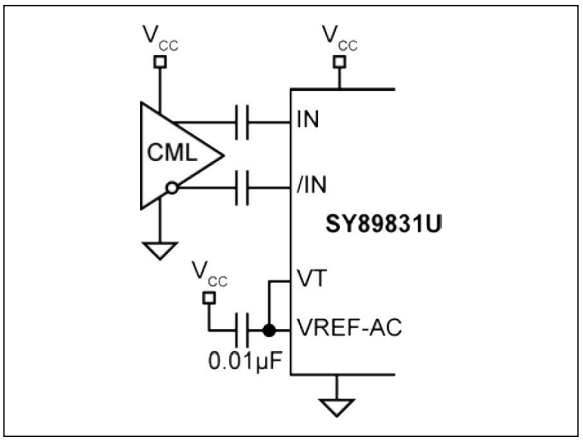


FIGURE 8-4: AC-COUPLED CML INPUT INTERFACE.

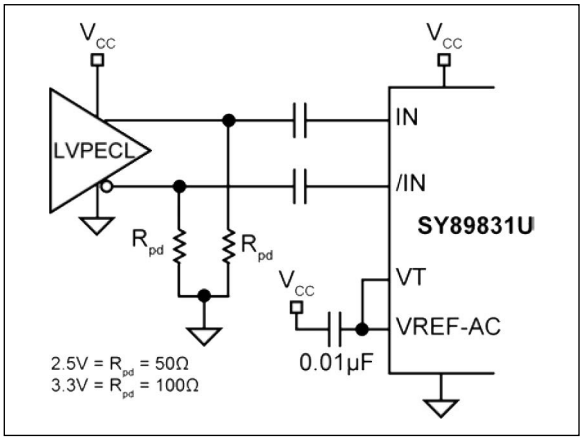


FIGURE 8-2: AC-COUPLED LVPECL INPUT INTERFACE.

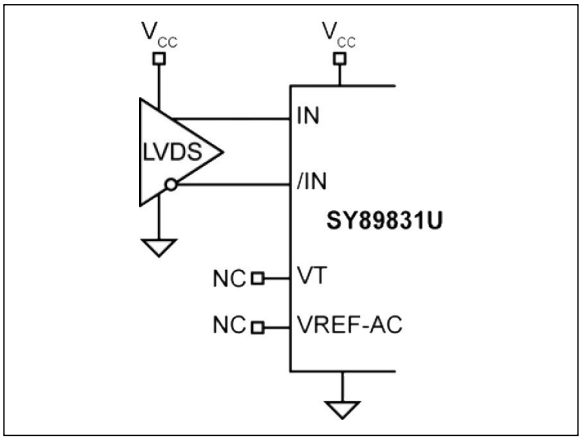


FIGURE 8-5: DC-COUPLED LVDS INPUT INTERFACE.

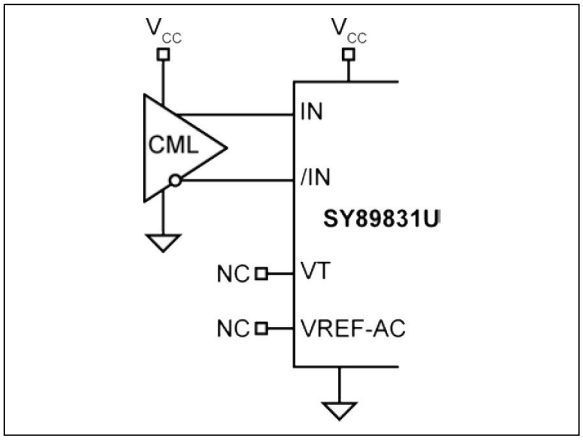


FIGURE 8-3: DC-COUPLED CML INPUT INTERFACE.

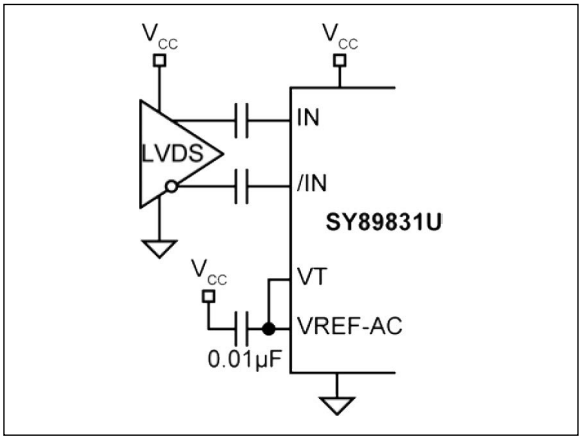


FIGURE 8-6: AC-COUPLED LVDS INPUT INTERFACE.

9.0 OUTPUT TERMINATION RECOMMENDATIONS

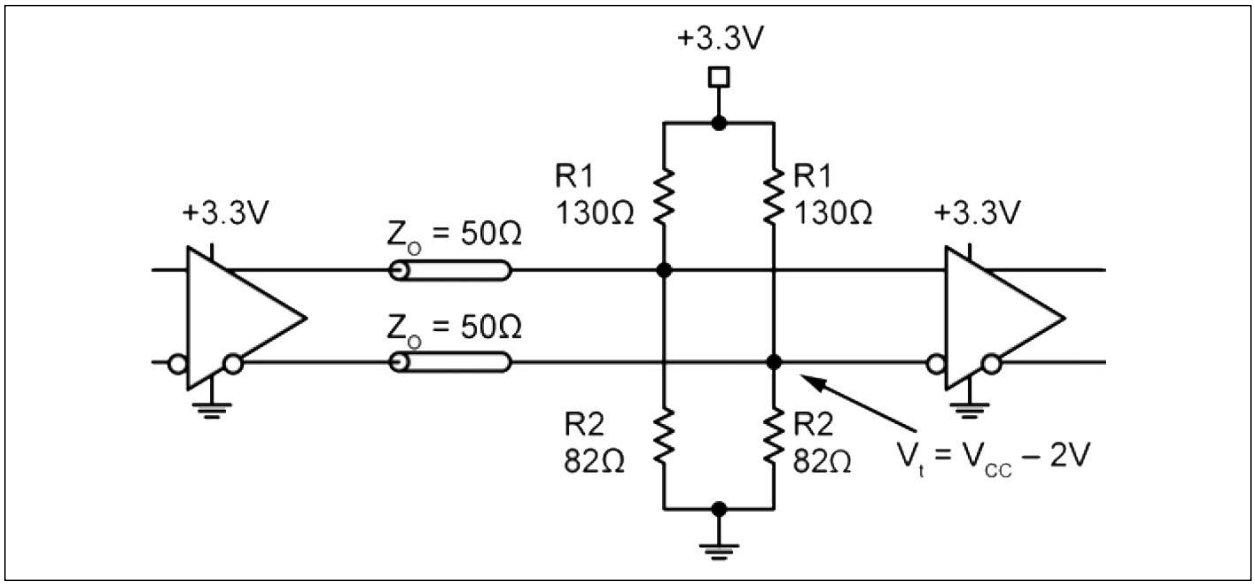


FIGURE 9-1: PARALLEL TERMINATION – THEVENIN EQUIVALENT

Note 1: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

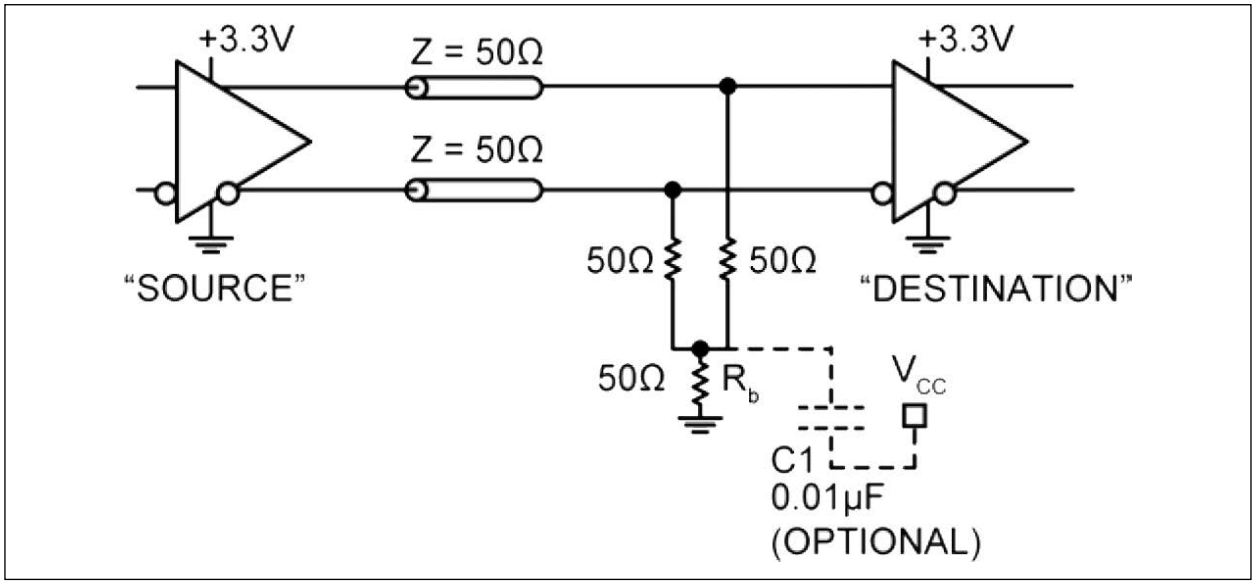


FIGURE 9-2: THREE-RESISTOR "Y-TERMINATION"

Note 1: Power-saving alternative to Thevenin termination.

2: Place termination resistors as close to destination inputs as possible.

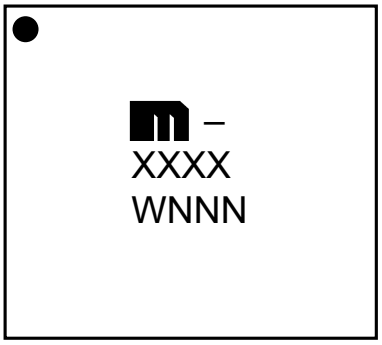
3: R_b resistor sets the DC bias voltage, equal to V_t. For +2.5V systems R_b = 19Ω

4: C1 is an optional bypass capacitor that compensates for any tr/tf mismatches.

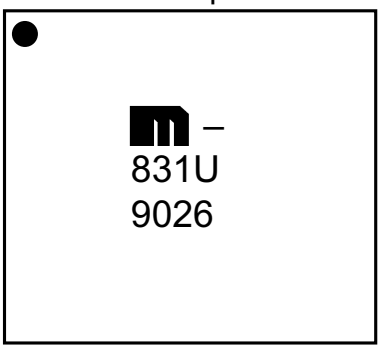
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

16-Lead VQFN*



Example*



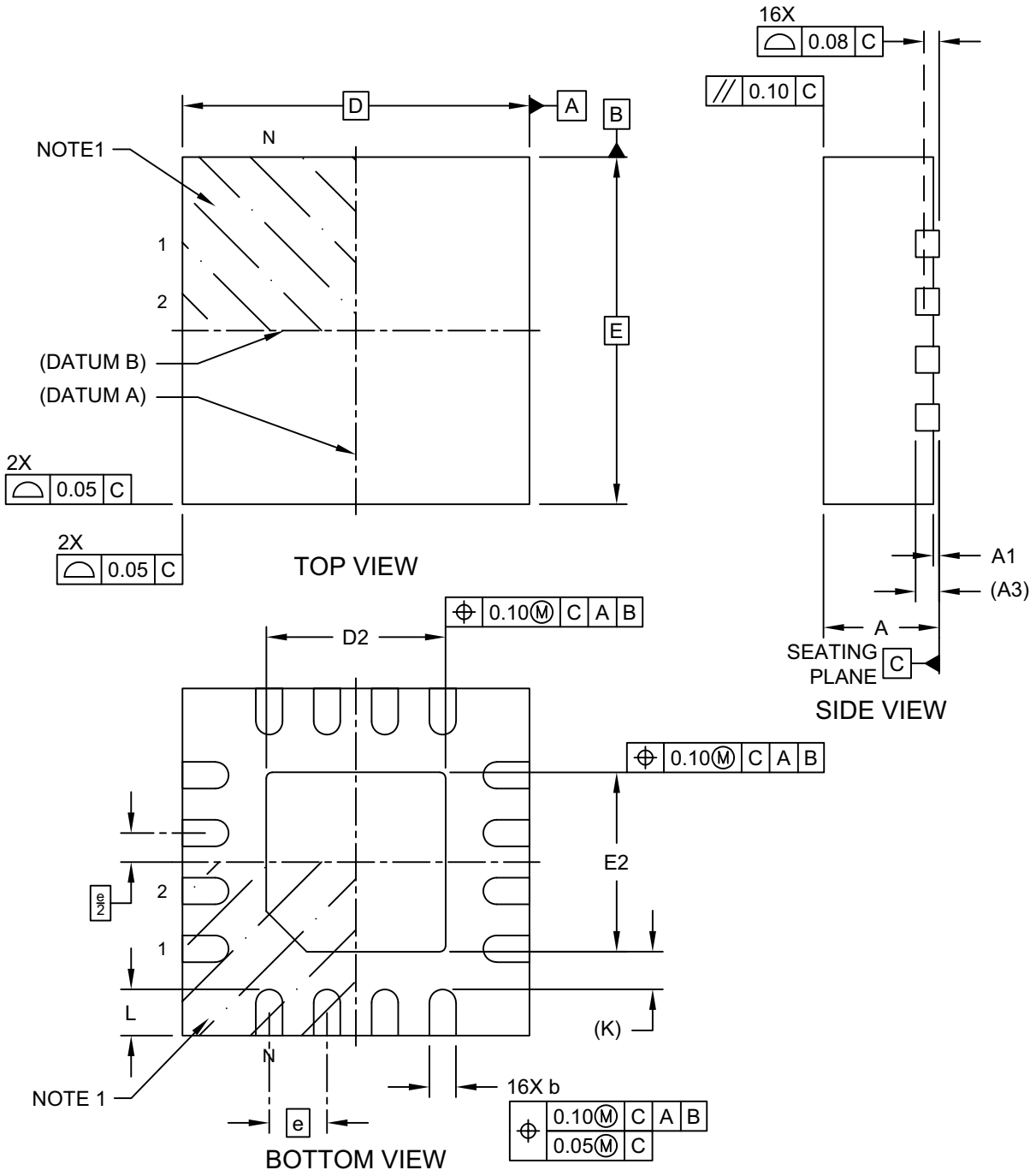
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

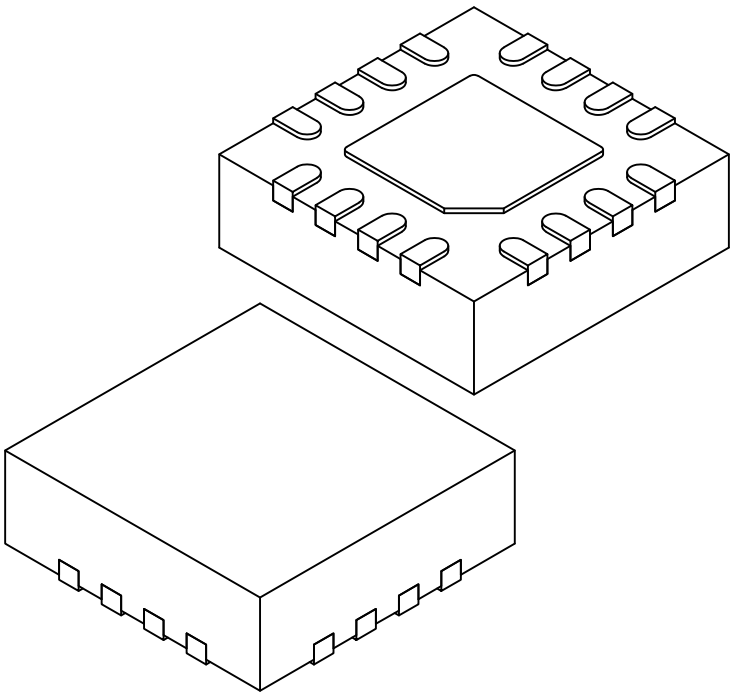
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

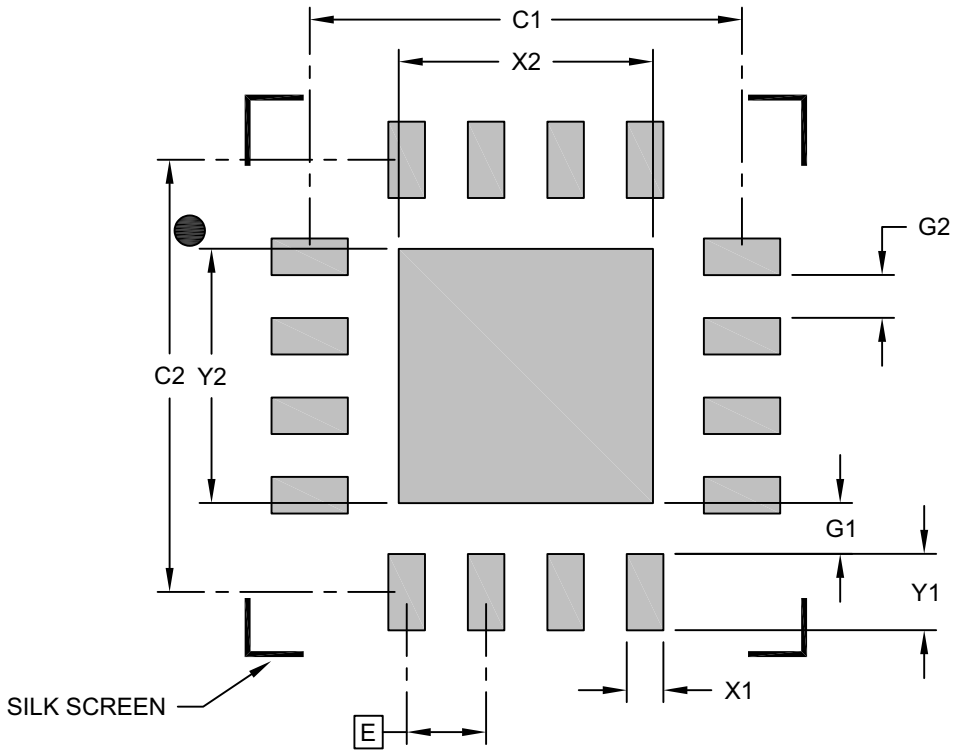
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2025)

- Converted Micrel data sheet for SY89831U to Microchip format as DS20006865A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY89831	=	Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator with Internal Termination Precision Edge®
Voltage Option:	U	=	2.5V/3.3V
Package:	M	=	16-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) **SY89831UMG**

2.5V/3.3, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY89831UMG-TR**

2.5V/3.3, 16-Lead VQFN, –40°C to 85°C, 1000/Reel

NOTES:

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ISBN: 979-8-3371-1259-6

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