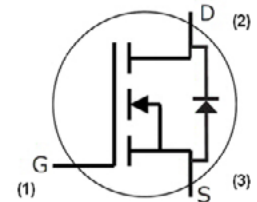


C3M0016120D

Silicon Carbide Power MOSFET C3M™ MOSFET Technology N-Channel Enhancement Mode

Features

- C3M™ Silicon Carbide (SiC) MOSFET technology
- High blocking voltage with low On-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant



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Part Number	Package	Marking
C3M0016120D	TO 247-3	C3M0016120D

Typical Applications

- Renewable energy
- High voltage DC/DC converters
- Switch Mode Power Supplies
- UPS

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			115	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19
				85		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
Pulsed Drain Current	I_{DM}			250		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			556	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	—	—	V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	Fig. 11
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6		$V_{DS} = V_{GS}, I_D = 23\text{ mA}$	
		—	2.0	—		$V_{DS} = V_{GS}, I_D = 23\text{ mA}, T_J = 175^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	μA	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	11.2	16	22.3	m Ω	$V_{GS} = 15\text{ V}, I_D = 75\text{ A}$	Fig. 4, 5, 6
		—	28.8	—		$V_{GS} = 15\text{ V}, I_D = 75\text{ A}, T_J = 175^\circ\text{C}$	
Transconductance	g_{fs}	—	53	—	S	$V_{DS} = 20\text{ V}, I_{DS} = 75\text{ A}$	Fig. 7
			47			$V_{DS} = 20\text{ V}, I_{DS} = 75\text{ A}, T_J = 175^\circ\text{C}$	
Input Capacitance	C_{iss}	—	6085	—	pF	$V_{GS} = 0\text{ V},$ $V_{DS} = 1000\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
Output Capacitance	C_{oss}	—	230	—			
Reverse Transfer Capacitance	C_{rss}	—	13	—			
C_{oss} Stored Energy	E_{oss}	—	130	—	μJ		Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	4.64	—	mJ	$V_{DS} = 800\text{ V}, V_{GS} = -4/+15\text{ V}, I_D = 75\text{ A},$ $R_{G(ext)} = 5\Omega, L = 65.7\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{off}	—	2.93	—			
Turn-On Switching Energy (External Diode)	E_{on}	—	7.79	—			
Turn Off Switching Energy (External Diode)	E_{off}	—	2.95	—			
Turn-On Delay Time	$t_{d(on)}$	—	174	—	ns	$V_{DS} = 800\text{ V}, V_{GS} = -4/25\text{ V}$ $R_{G(ext)} = 5\Omega, I_D = 75\text{ A}, L = 65.7\text{ }\mu\text{H}$ Timing relative to V_{DS} , Inductive load	Fig. 27
Rise Time	t_r	—	28	—			
Turn-Off Delay Time	$t_{d(off)}$	—	84	—			
Fall Time	t_f	—	27	—			
Internal Gate Resistance	$R_{G(int)}$	—	2.6	—	Ω	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	Q_{gs}	—	70	—	nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/25\text{ V}$ $I_D = 75\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	60	—			
Total Gate Charge	Q_g	—	207	—			



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	4.6	—	V	$V_{GS} = -4\text{ V}, I_{SD} = 37.5\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2	—		$V_{GS} = -4\text{ V}, I_{SD} = 37.5\text{ A}, T_J = 175^\circ\text{C}$	
Continuous Diode Forward Current	I_S	—	112	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
Diode Pulse Current	I_{SM}	—	250		$V_{GS} = -4\text{ V}$, pulse width t_P limited by $T_{j\max}$	
Reverse Recover Time	t_{rr}	96	—	nS	$V_{GS} = -4\text{ V}, I_{SD} = 75\text{ A}, V_R = 800\text{ V}$ $di_F/dt = 900\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	604	—	nC		
Peak Reverse Recovery Current	I_{rrm}	15	—	A		
Reverse Recovery time	t_{rr}	58	—	nS	$V_{GS} = -5\text{ V}, I_{SD} = 75\text{ A}, V_R = 800\text{ V}$ $di_F/dt = 1400\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	672	—	nC		
Peak Reverse Recovery Current	I_{rrm}	22	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.27	$^\circ\text{C}/\text{W}$	Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40		

Typical Performance

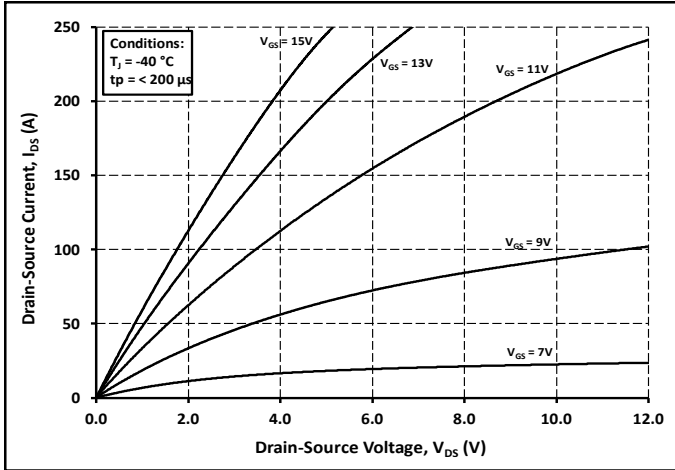


Figure 1. Output Characteristics $T_j = -40^\circ\text{C}$

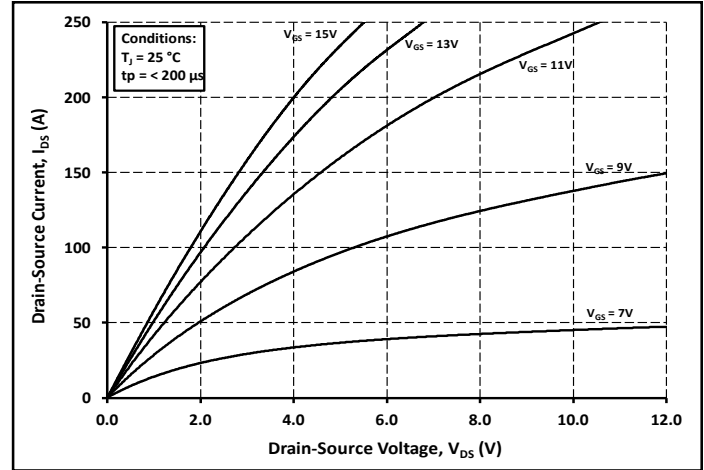


Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$

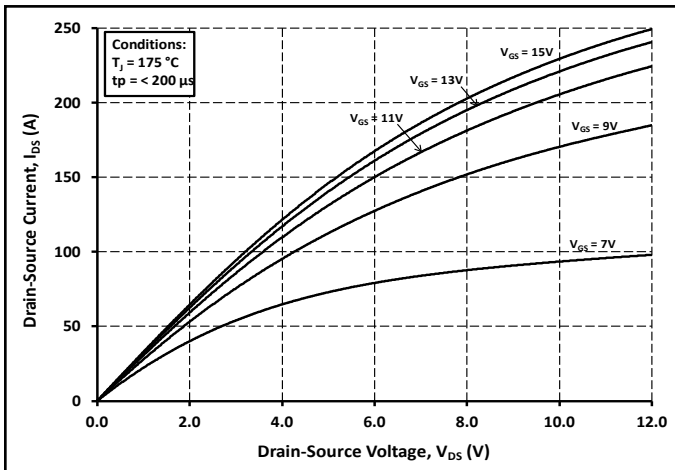


Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$

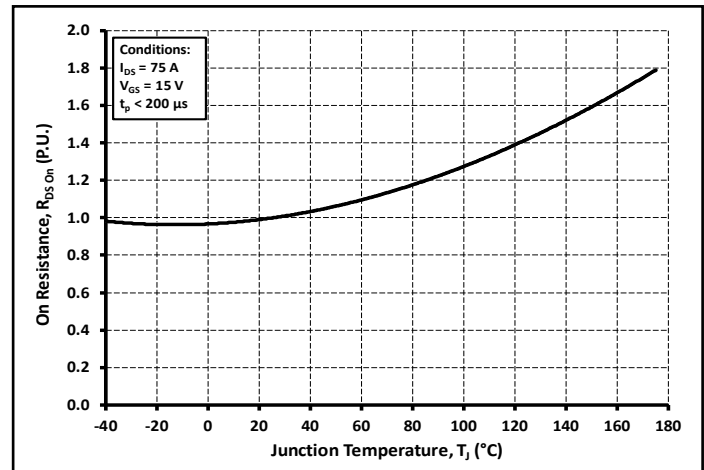


Figure 4. Normalized On-Resistance vs. Temperature

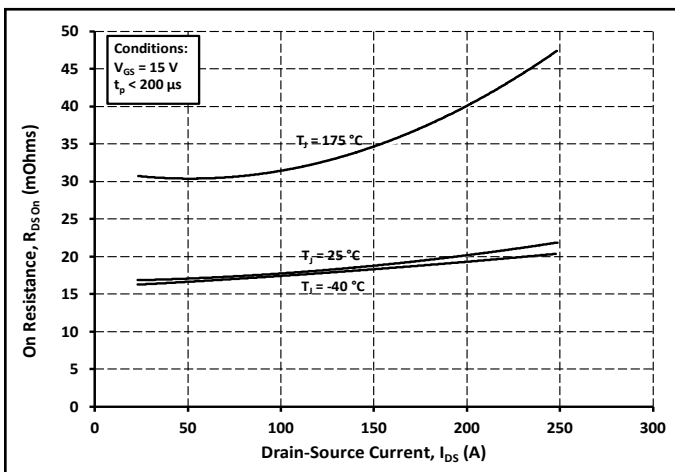


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

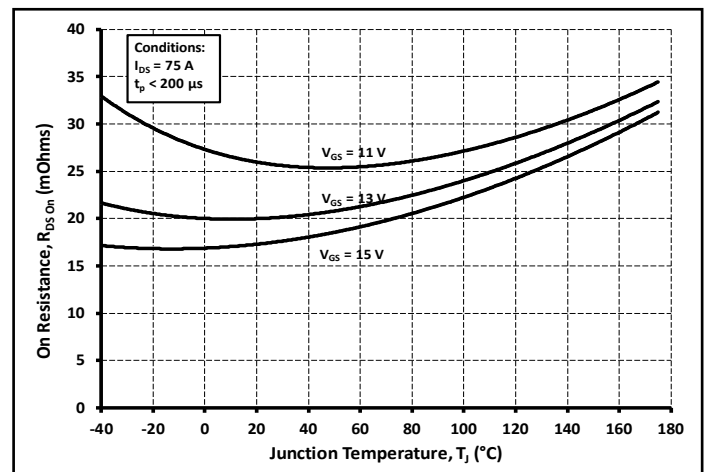


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

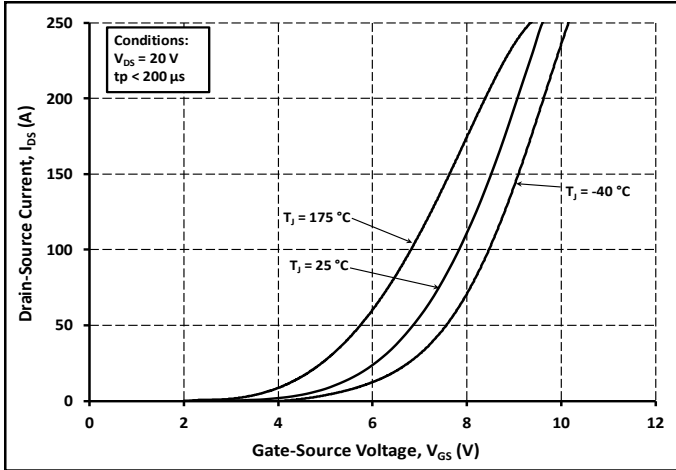


Figure 7. Transfer Characteristic for Various Junction Temperatures

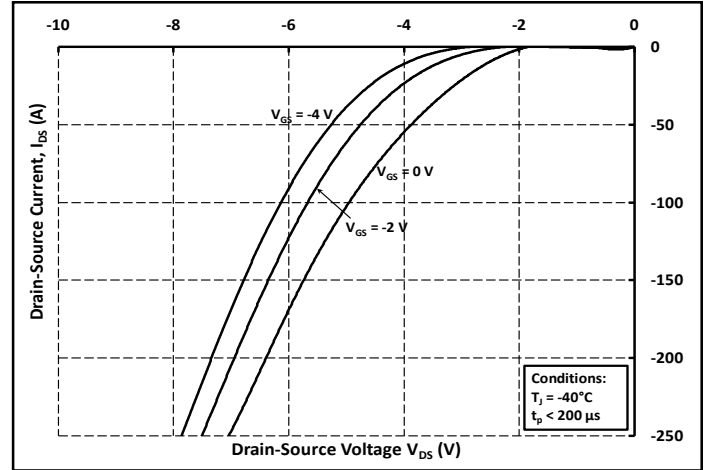


Figure 8. Body Diode Characteristic at -40°C

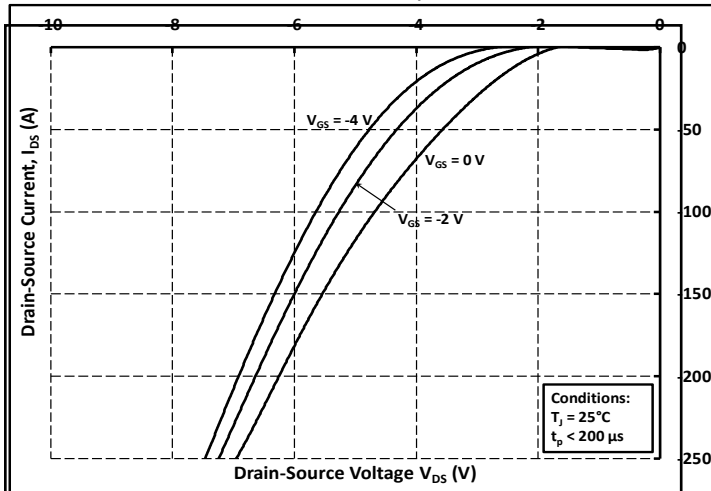


Figure 9. Body Diode Characteristic at 25°C

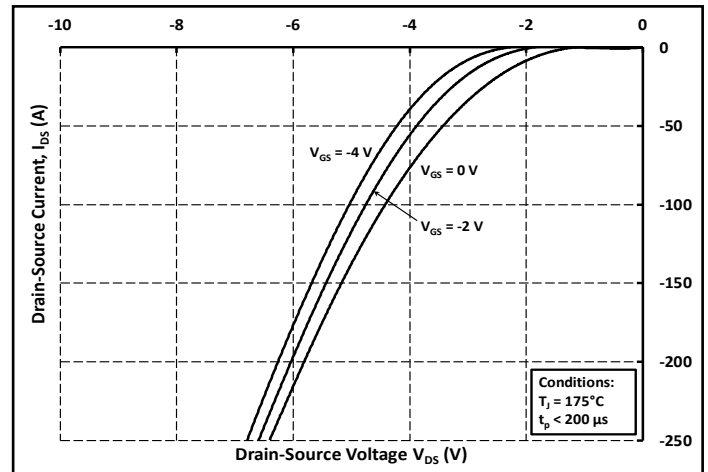


Figure 10. Body Diode Characteristic at 175°C

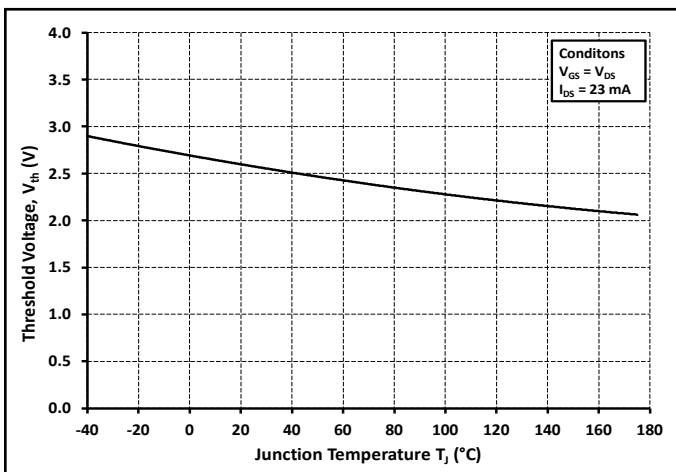


Figure 11. Threshold Voltage vs. Temperature

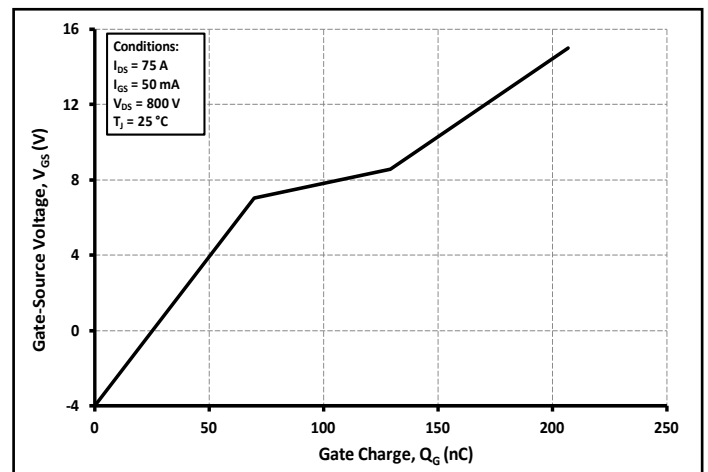


Figure 12. Gate Charge Characteristics

Typical Performance

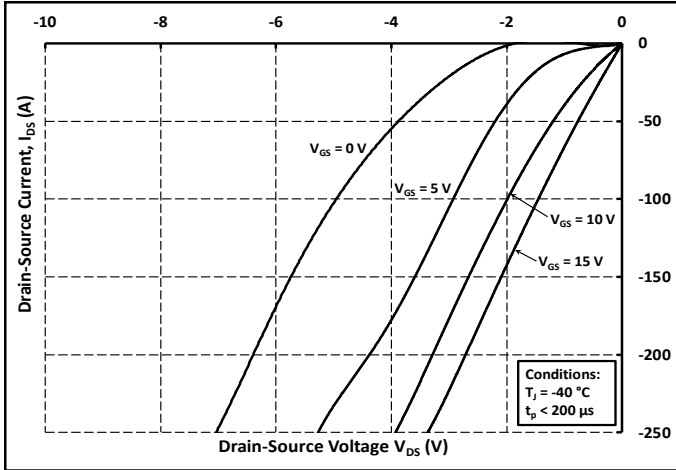


Figure 13. 3rd Quadrant Characteristic at -40°C

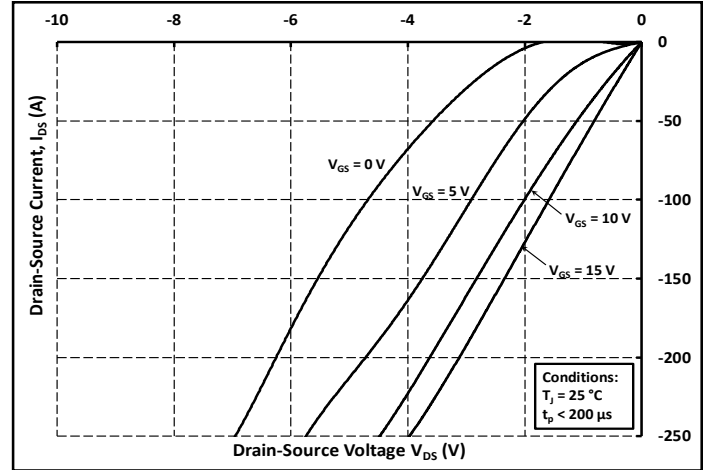


Figure 14. 3rd Quadrant Characteristic at 25°C

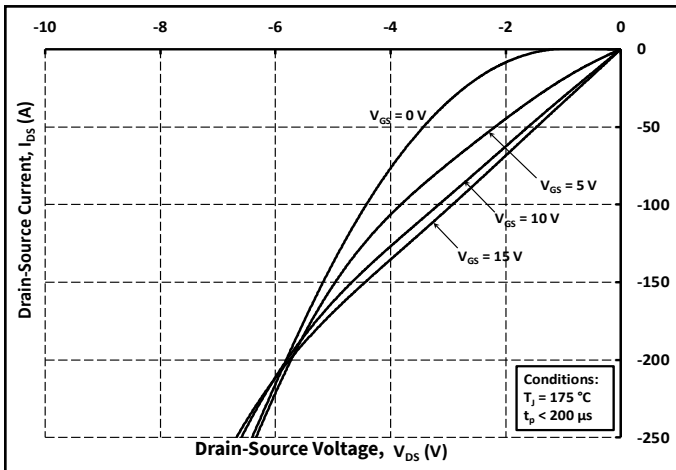


Figure 15. 3rd Quadrant Characteristic at 175°C

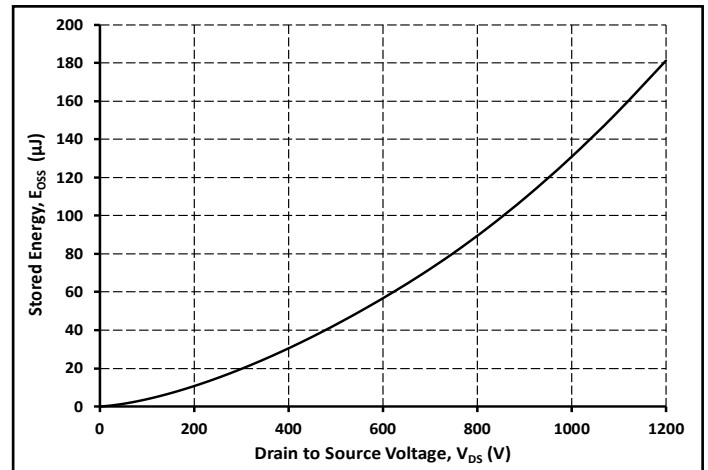


Figure 16. Output Capacitor Stored Energy

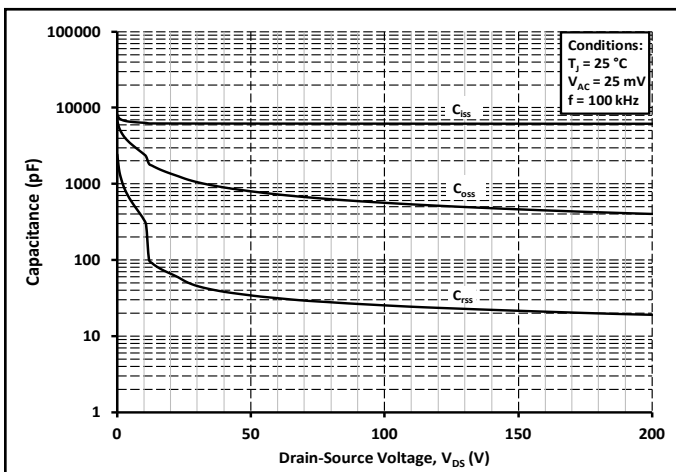


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

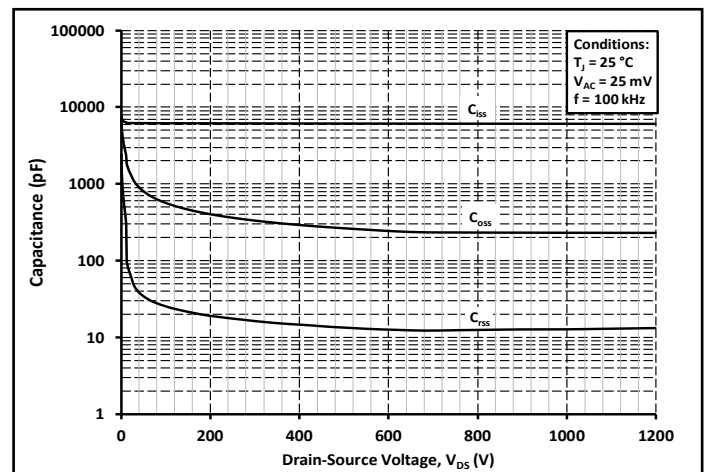


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200 V)

Typical Performance

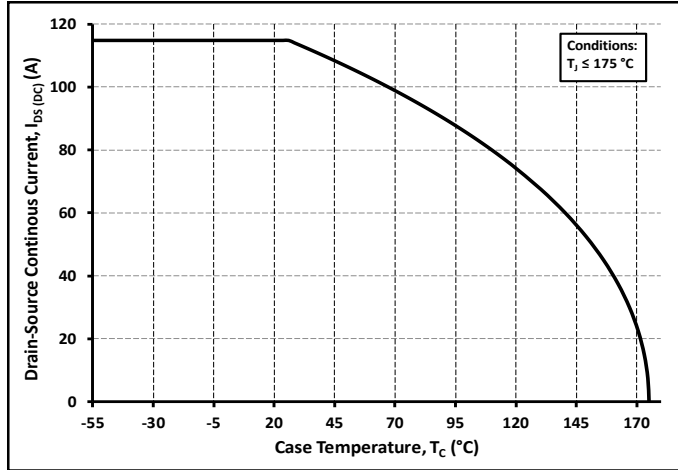


Figure 19. Continuous Drain Current Derating vs. Case Temperature

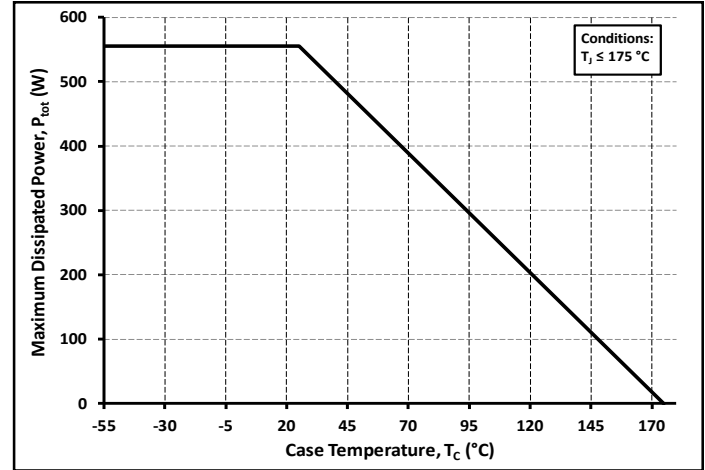


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

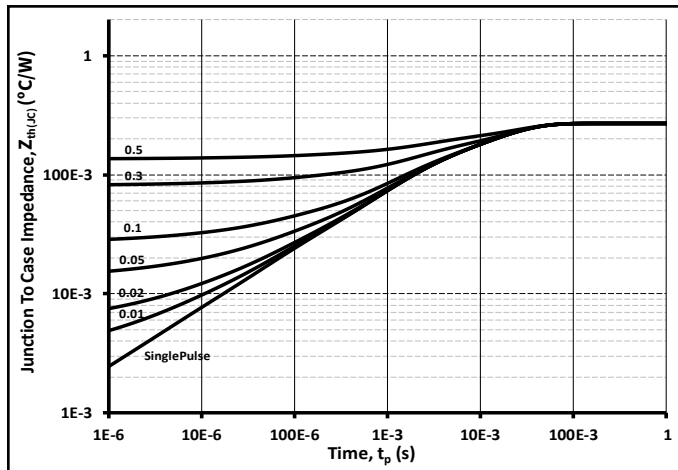


Figure 21. Transient Thermal Impedance (Junction - Case)

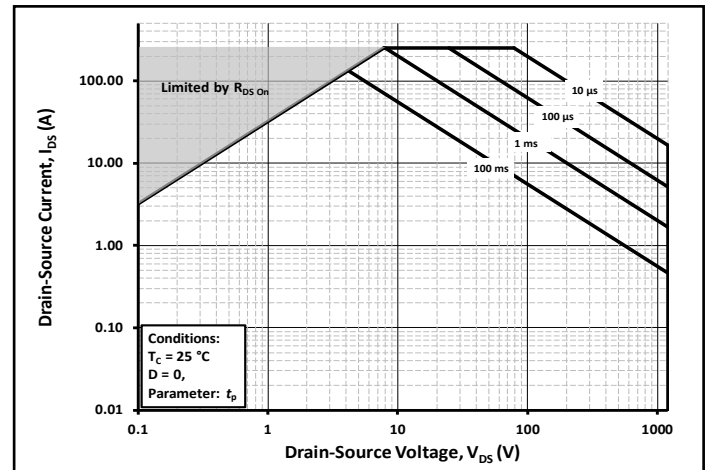


Figure 22. Safe Operating Area

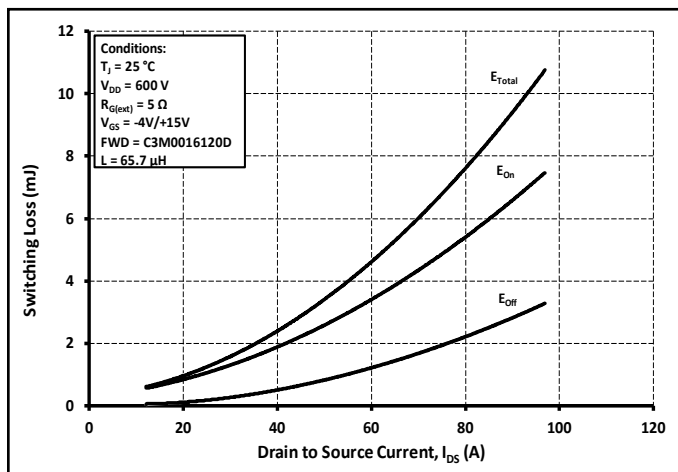


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600 \text{ V}$)

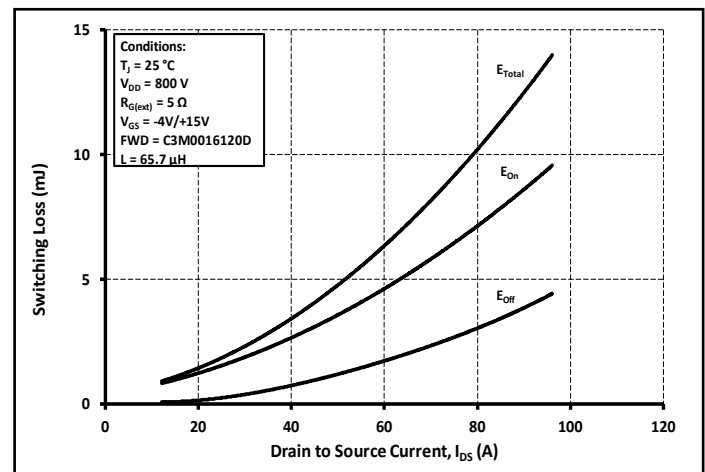


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800 \text{ V}$)

Typical Performance

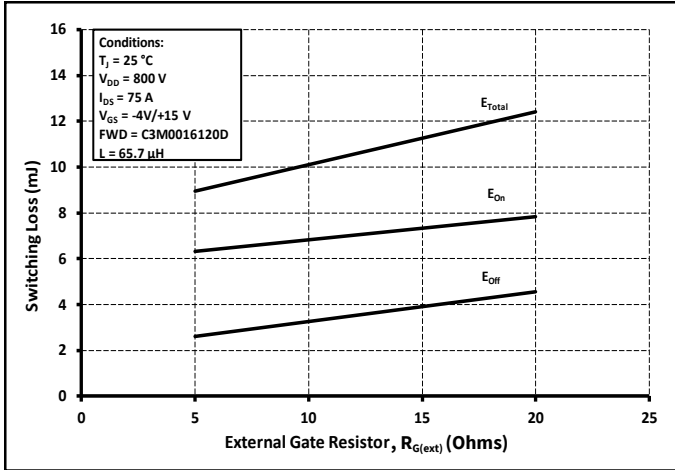


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

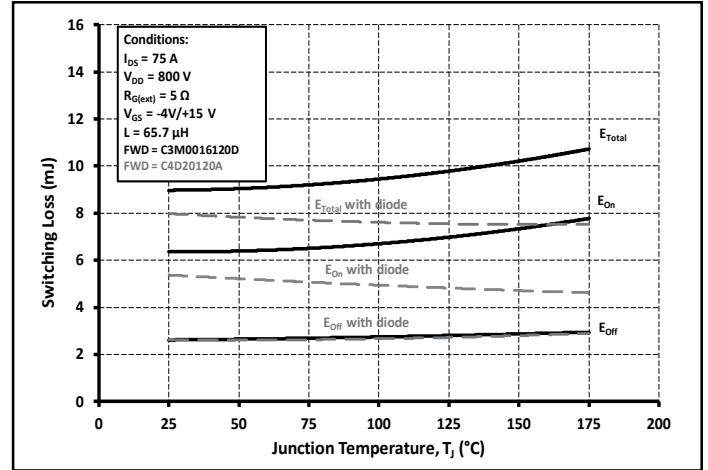


Figure 26. Clamped Inductive Switching Energy vs. Temperature

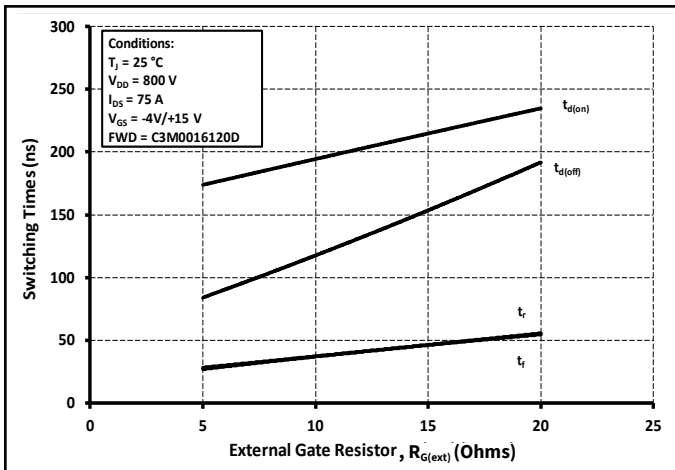


Figure 27. Switching Times vs. $R_{G(ext)}$

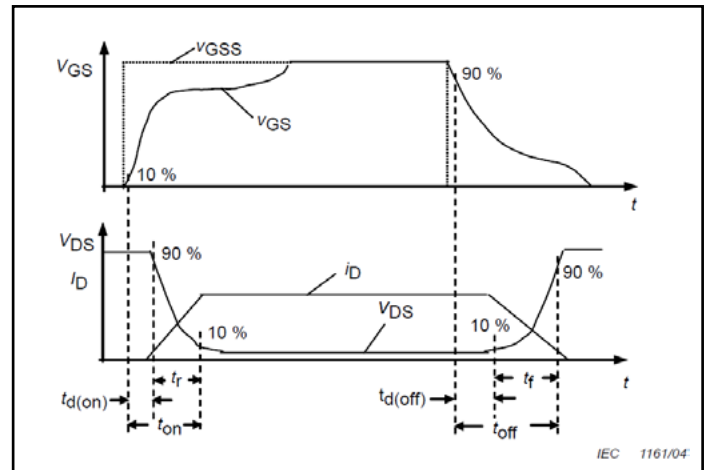


Figure 28. Switching Times Definition

Test Circuit Schematic

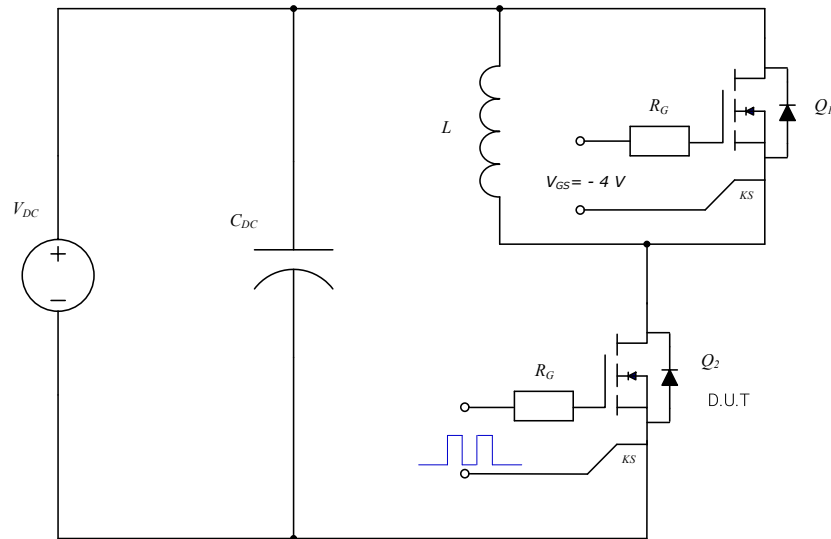
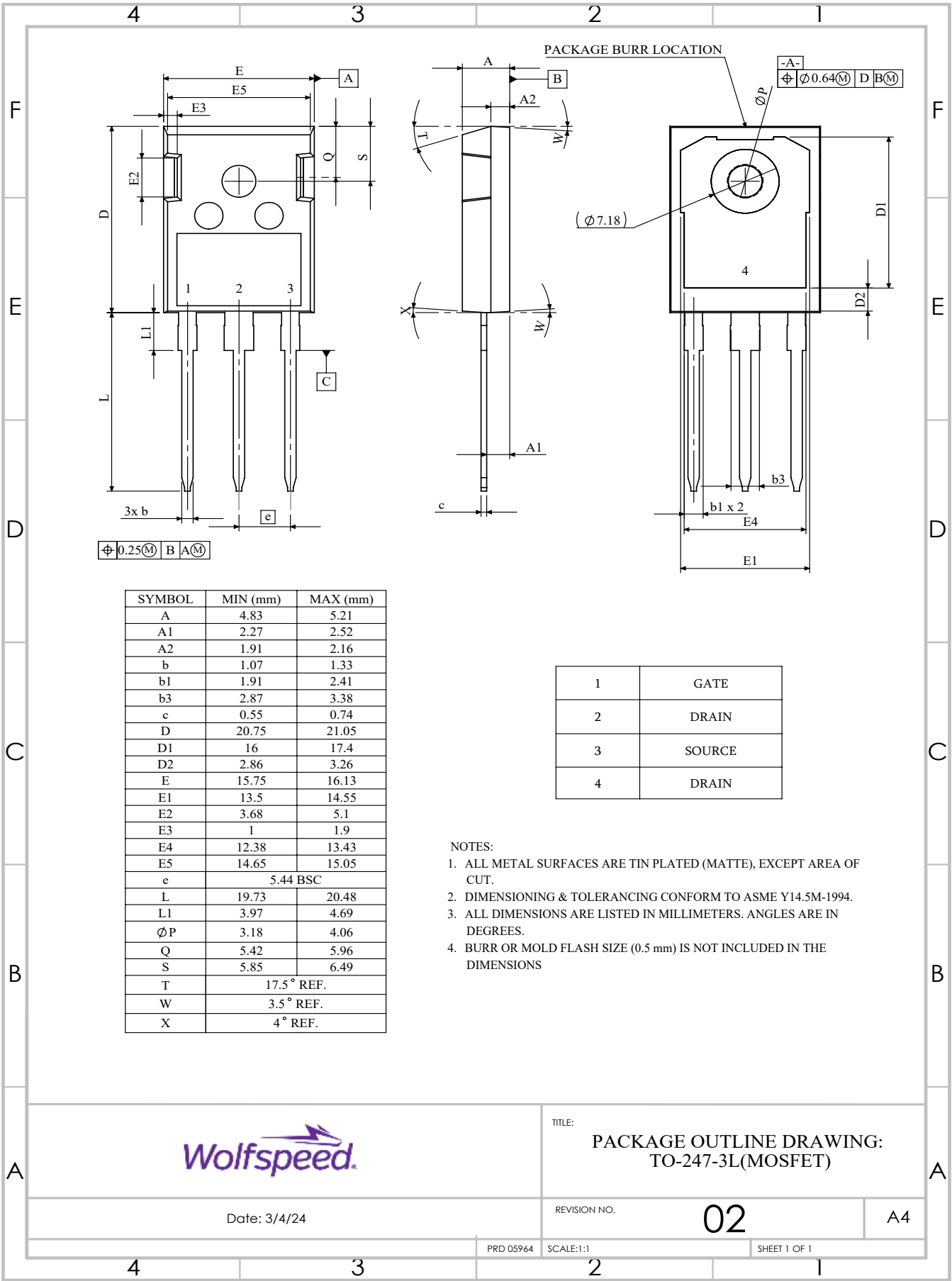


Figure 29. Clamped Inductive Switching Waveform Test Circuit

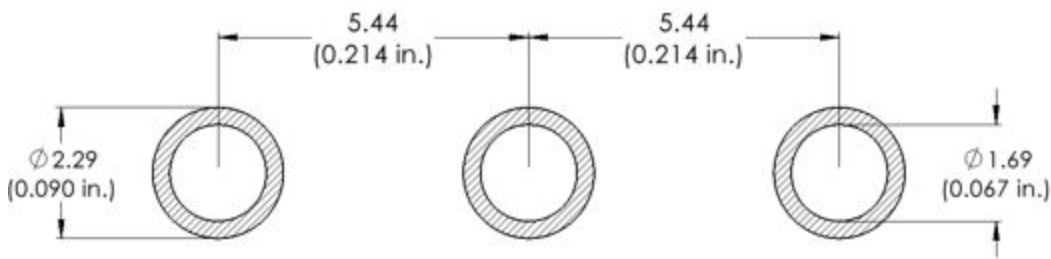
Note:

³ Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions – Package TO-247-3



Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
-	August-2019	N/A
1	January-2024	Updated Wolfspeed branding, package drawing, package image, and solder pad layout, added Revision History Table, Table 1 layout revised
2	September - 2024	Legal Disclaimer, POD, Diode Pulse Current Symbol

Related Links

- [SPICE Models](#)
- [SiC MOSFET Isolated Gate Driver reference design](#)
- [SiC MOSFET Evaluation Board](#)



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Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power