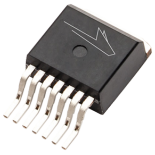
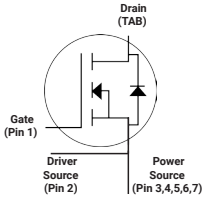
# C3M0075120J

## Silicon Carbide Power MOSFET
## C3M™ MOSFET Technology
## N-Channel Enhancement Mode



TO-263-7




Package Types: TO-263-7
PN's: C3M0075120J

### Features

- 3rd generation SiC MOSFET technology
- Low impedance package with driver source pin
- 7 mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ($Q_{rr}$)
- Halogen free, RoHS compliant

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### Typical Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch mode power supplies

### Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

### Key Parameters

| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions | Note |
|---|---|---|---|---|---|---|---|
| Drain - Source Voltage | $V_{DS}$ | | | 1200 | V | $T_C$ = 25°C | |
| Maximum Gate - Source Voltage | $V_{GS(max)}$ | -8 | | +19 | | Transient | |
| Operational Gate-Source Voltage | $V_{GS\ op}$ | | -4/15 | | | Static | Note 1 |
| DC Continuous Drain Current | $I_D$ | | | 30 | A | $V_{GS}$ = 15 V, $T_C$ = 25 °C, $T_J$ ≤150 °C | Fig. 19 Note 2 |
| | | | | 19.7 | | $V_{GS}$ = 15 V, $T_C$ = 100 °C, $T_J$ ≤150 °C | |
| Pulsed Drain Current | $I_{DM}$ | | | 80 | | $t_{Pmax}$ limited by $T_{jmax}$ $V_{GS}$ = 15V, $T_C$ = 25 °C | Fig. 22 |
| Power Dissipation | $P_D$ | | | 113.6 | W | $T_C$ = 25 °C, $T_J$ = 150 °C | Fig. 20 |
| Operating Junction and Storage Temperature | $T_J$, $T_{stg}$ | | | -55 to +150 | °C | | |
| Solder Temperature | $T_L$ | | | 260 | | According to JEDEC J-STD-020 | |

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

## Electrical Characteristics ($T_C$ = 25 °C Unless Otherwise Specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.8 | 2.5 | 3.6 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 5 mA | Fig. 11 |
| | | | 2.2 | | | $V_{DS}$ = $V_{GS}$, $I_D$ = 5 mA, $T_J$ = 150 °C | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | | 1 | 50 | µA | $V_{DS}$ = 1200 V, $V_{GS}$ = 0 V | |
| Gate-Source Leakage Current | $I_{GSS}$ | | 10 | 250 | nA | $V_{GS}$ = 15 V, $V_{DS}$ = 0 V | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | | 75 | 90 | mΩ | $V_{GS}$ = 15 V, $I_D$ = 20 A | Fig. 4, 5, 6 |
| | | | 100 | | | $V_{GS}$ = 15 V, $I_D$ = 20 A, $T_J$ = 150 °C | |
| Transconductance | $g_{fs}$ | | 12 | | S | $V_{DS}$ = 20 V, $I_{DS}$ = 20 A | Fig. 7 |
| | | | 13 | | | $V_{DS}$ = 20 V, $I_{DS}$ = 20 A, $T_J$ = 150 °C | |
| Input Capacitance | $C_{iss}$ | | 1390 | | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 1000 V<br>f = 1 MHz<br>$V_{AC}$ = 25 mV | Fig. 17, 18 |
| Output Capacitance | $C_{oss}$ | | 58 | | | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 2 | | | | |
| $C_{oss}$ Stored Energy | $E_{oss}$ | | 33 | | µJ | | Fig. 16 |
| Turn-On Switching Energy (Body Diode FWD) | $E_{ON}$ | | 200 | | µJ | $V_{DS}$ = 800 V, $V_{GS}$ = -4 V/15 V, $I_D$ = 20 A,<br>$R_{G(ext)}$ = 0 Ω, L = 156 µH, $T_J$ = 150 °C | Fig. 26, 29 |
| Turn-Off Switching Energy (Body Diode FWD) | $E_{OFF}$ | | 90 | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | | 7 | | ns | $V_{DD}$ = 800 V, $V_{GS}$ = -4 V/15 V<br>$I_D$ = 20 A, $R_{G(ext)}$ = 0 Ω,<br>Timing Relative to $V_{DS}$ Inductive Load | Fig. 27, 28, 29 |
| Rise Time | $t_r$ | | 15 | | | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 24 | | | | |
| Fall Time | $t_f$ | | 8 | | | | |
| Internal Gate Resistance | $R_{G(int)}$ | | 9 | | Ω | f = 1 MHz, $V_{AC}$ = 25 mV | |
| Gate to Source Charge | $Q_{gs}$ | | 18 | | nC | $V_{DS}$ = 800 V, $V_{GS}$ = -4 V/15 V<br>$I_D$ = 20 A<br>Per IEC60747-8-4 pg 21 | Fig. 12 |
| Gate to Drain Charge | $Q_{gd}$ | | 12 | | | | |
| Total Gate Charge | $Q_g$ | | 48 | | | | |

## Reverse Diode Characteristics ($T_C$ = 25 °C Unless Otherwise Specified)

| Parameter | Symbol | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$ | 4.5 | | V | $V_{GS}$ = -4 V, $I_{SD}$ = 10 A | Fig. 8, 9, 10 |
| | | 4.0 | | | $V_{GS}$ = -4 V, $I_{SD}$ = 10 A, $T_J$ = 150 °C | |
| Continuous Diode Forward Current | $I_S$ | | 22.4 | A | $V_{GS}$ = -4 V | |
| Diode Pulse Current | $I_{S,\ pulse}$ | 80 | | | $V_{GS}$ = -4 V, Pulse Width $t_P$ Limited by $T_{jmax}$ | |
| Reverse Recovery Time | $t_{rr}$ | 25 | | ns | $V_{GS}$ = -4 V, $I_{SD}$ = 20 A , $V_R$ = 800 V dif/dt = 1925 A/µs, $T_J$ = 25 °C | Fig. 29 |
| Reverse Recovery Charge | $Q_{rr}$ | 109 | | nC | | |
| Peak Reverse Recovery Current | $I_{rrm}$ | 11 | | A | | |

## Thermal Characteristics

| Parameter | Symbol | Typ. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|
| Thermal Resistance from Junction to Case | $R_{\theta JC}$ | 1.1 | °C/W | | Fig. 21 |
| Thermal Resistance from Junction to Ambient | $R_{\theta JA}$ | 40 | | | |

## Typical Performance

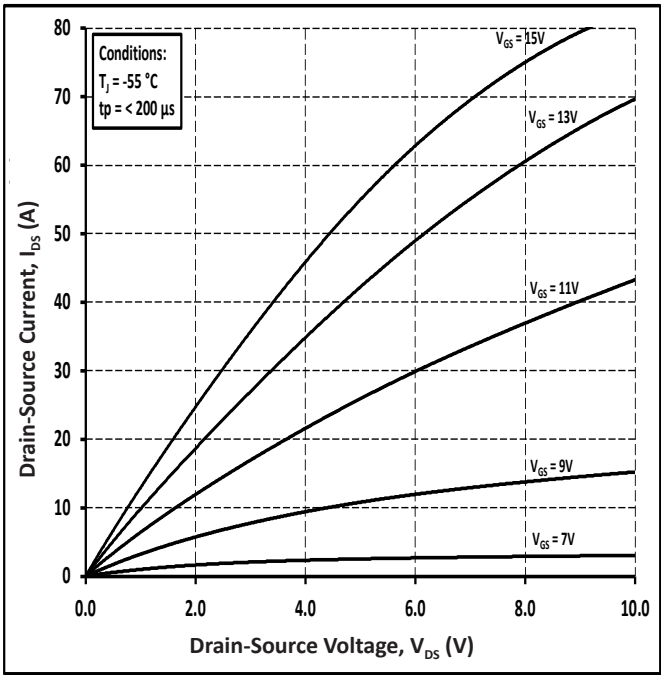



Figure 1. Output Characteristics $T_J$ = -55 °C

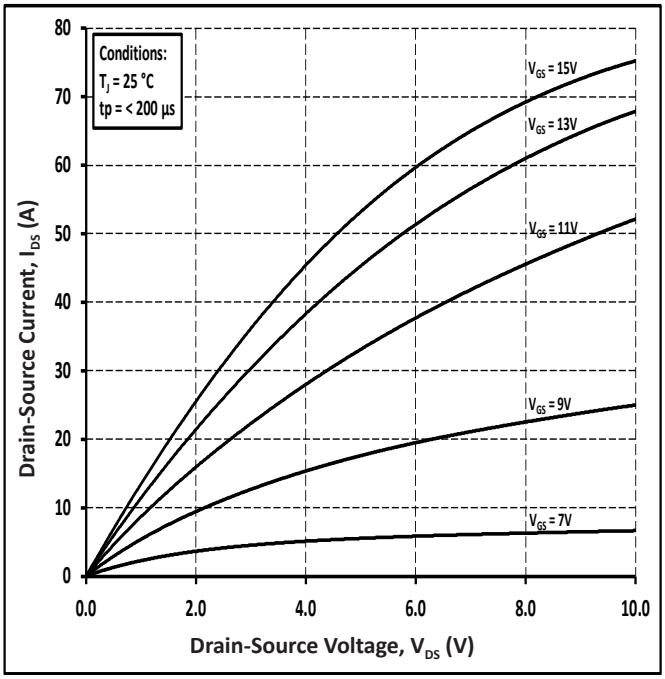



Figure 2. Output Characteristics $T_J$ = 25 °C

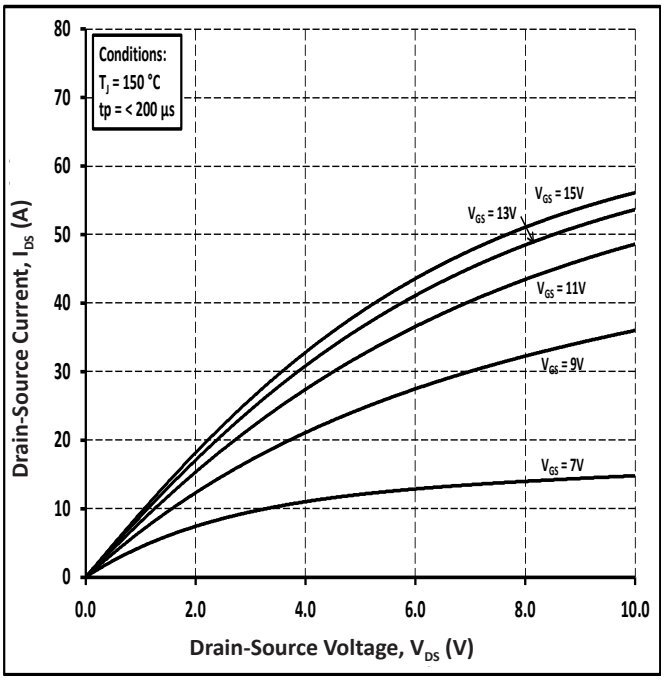



Figure 3. Output Characteristics $T_J$ = 150 °C

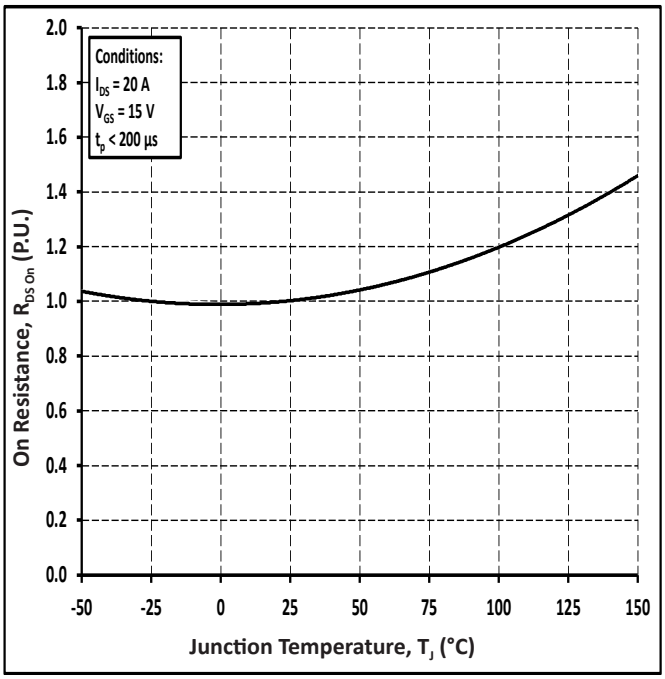



Figure 4. Normalized On-Resistance vs Temperature

## Typical Performance

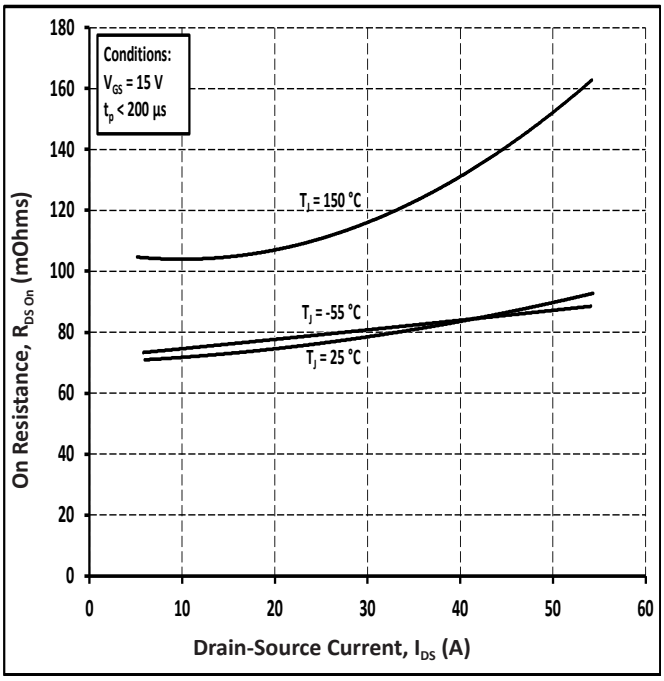



Figure 5. On-Resistance vs Drain Current for Various Temperatures

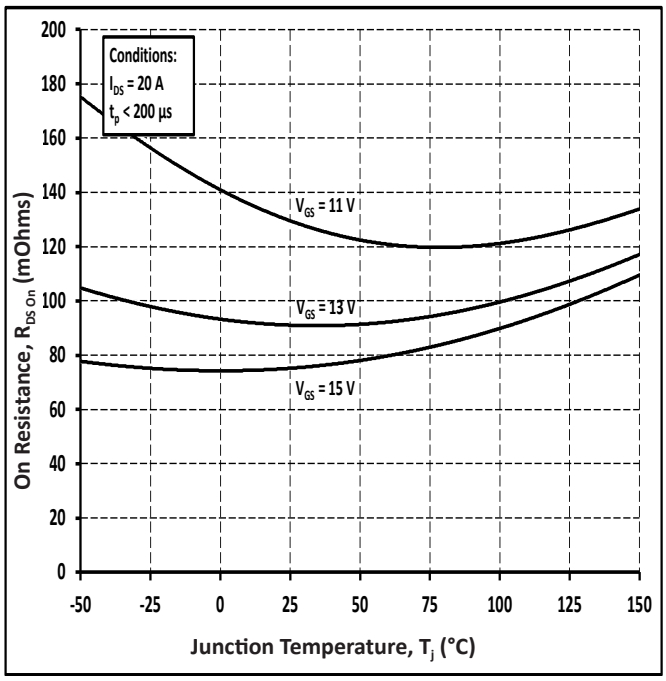



Figure 6. On-Resistance vs Temperature for Various Gate Voltage

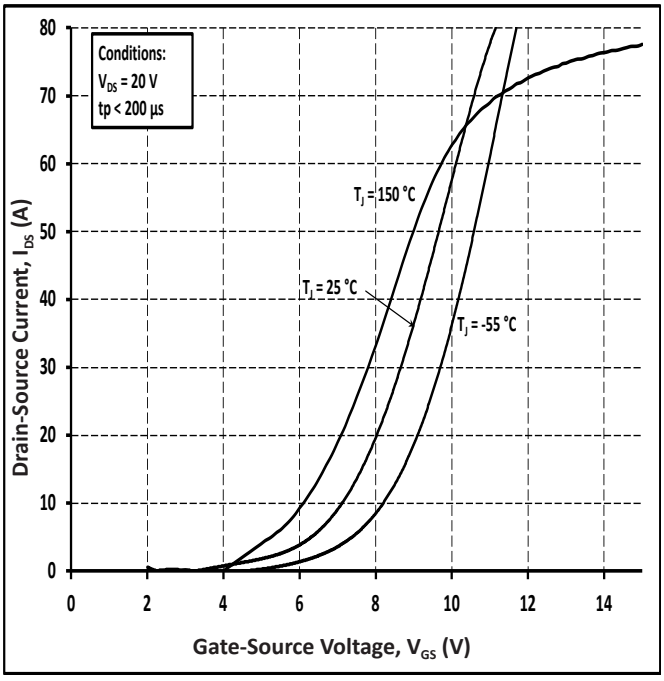



Figure 7. Transfer Characteristic for Various Junction Temperatures

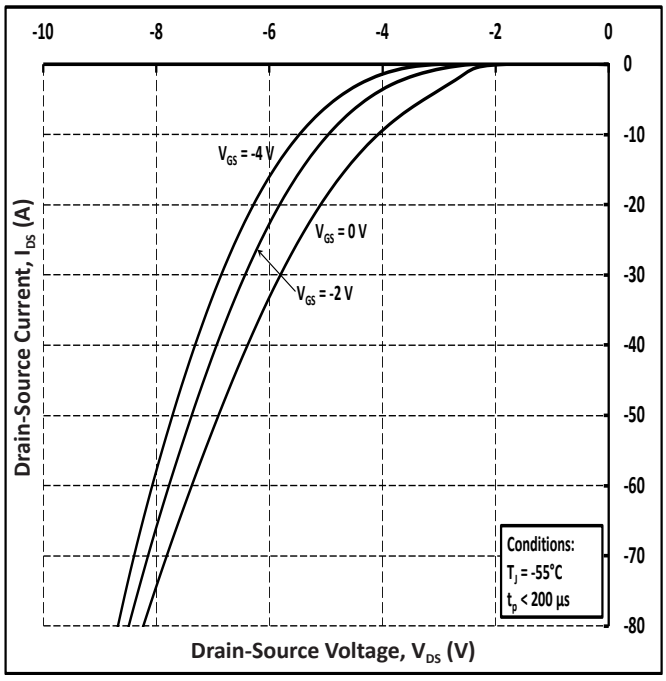



Figure 8. Body Diode Characteristic at -55 °C

## Typical Performance

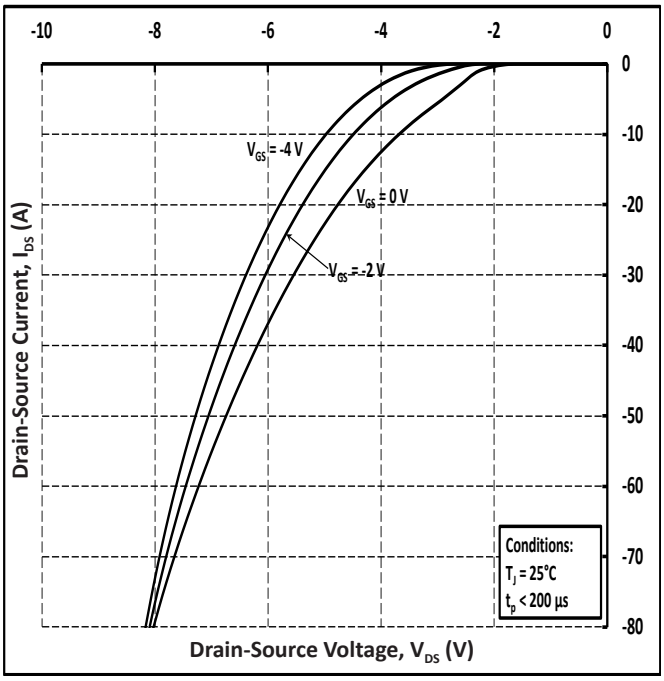



Figure 9. Body Diode Characteristic at 25 °C

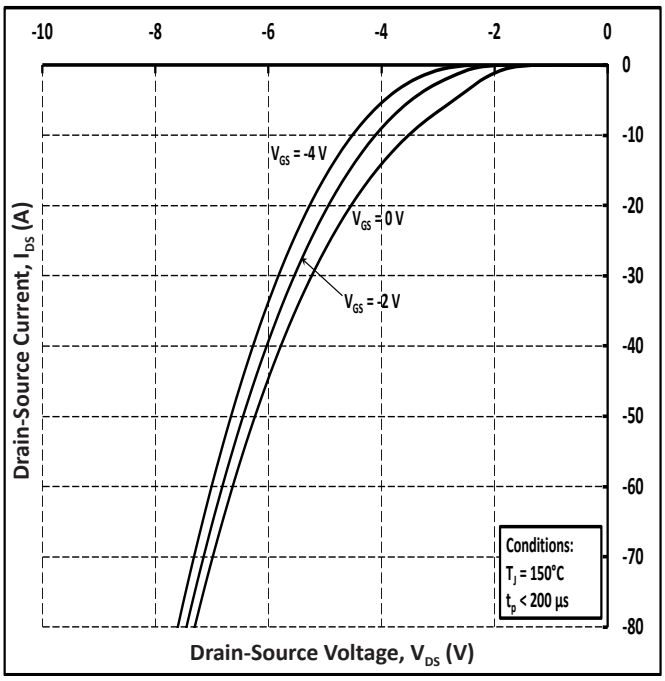



Figure 10. Body Diode Characteristic at 150 °C

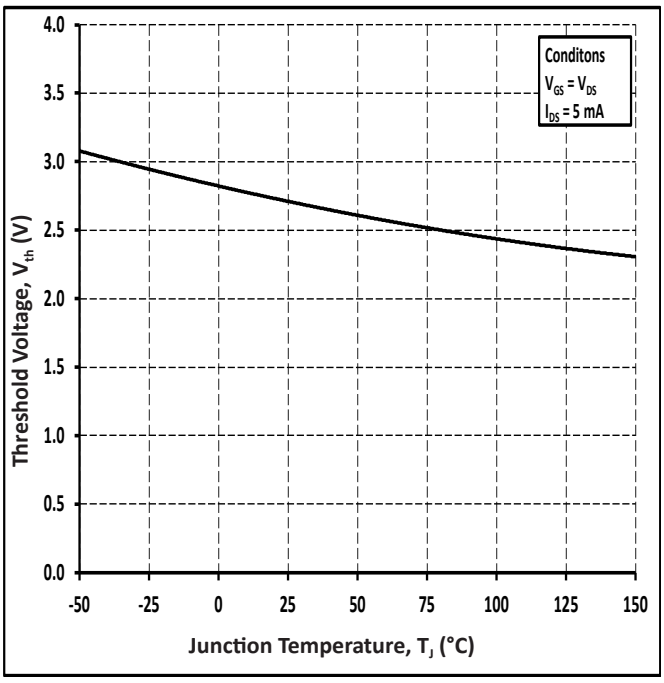



Figure 11. Threshold Voltage vs Temperature

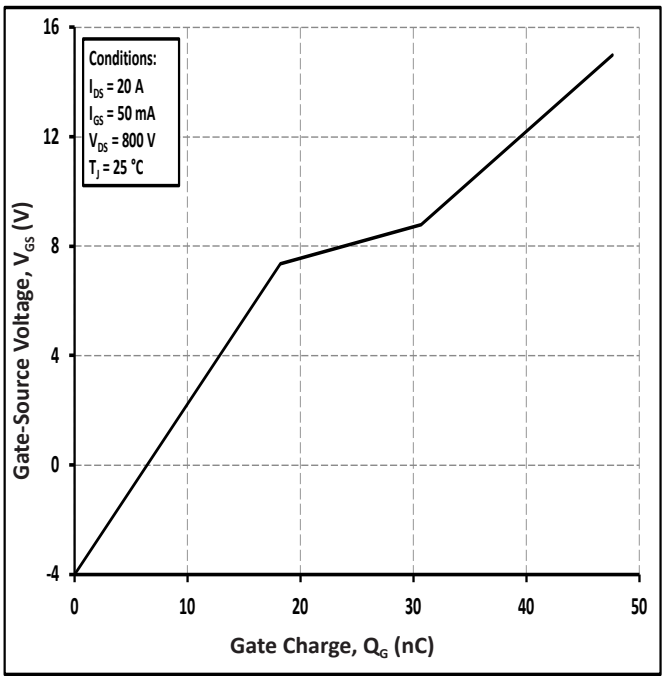



Figure 12. Gate Charge Characteristic

## Typical Performance

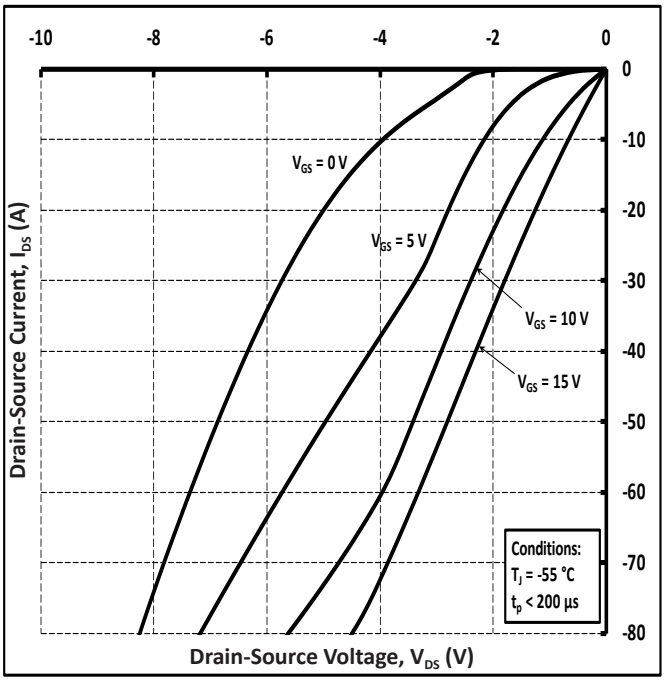



Figure 13. 3rd Quadrant Characteristic at -55 °C

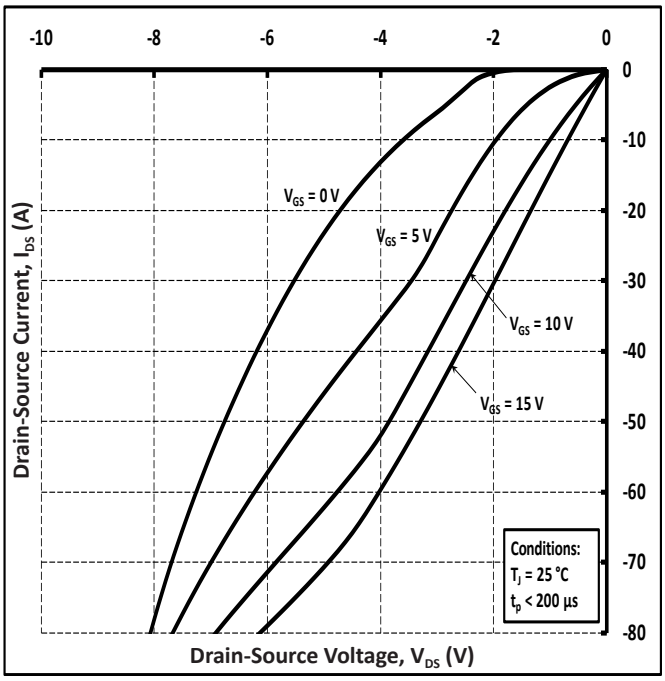



Figure 14. 3rd Quadrant Characteristic at 25 °C

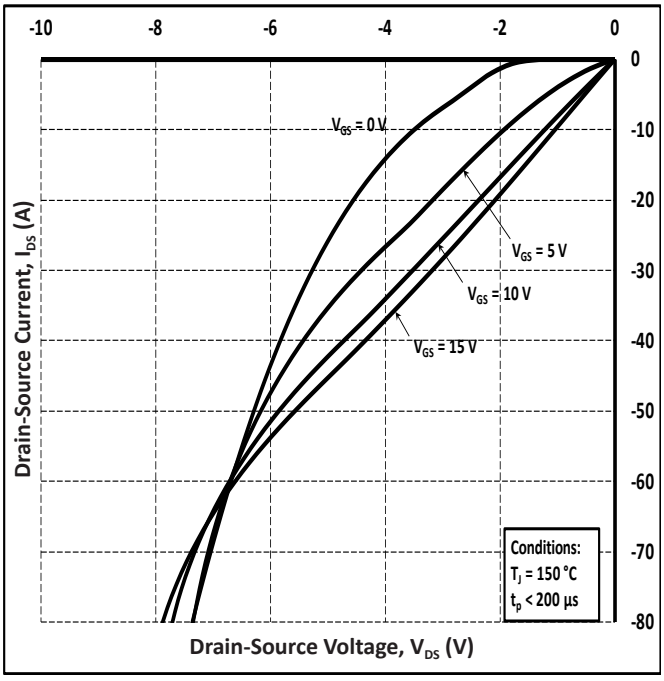



Figure 15. 3rd Quadrant Characteristic at 150 °C

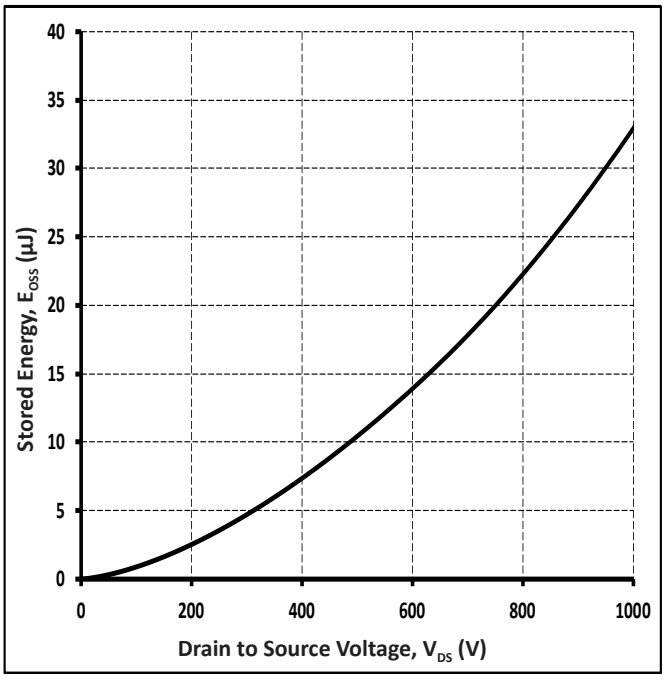



Figure 16. Output Capacitor Stored Energy

## Typical Performance

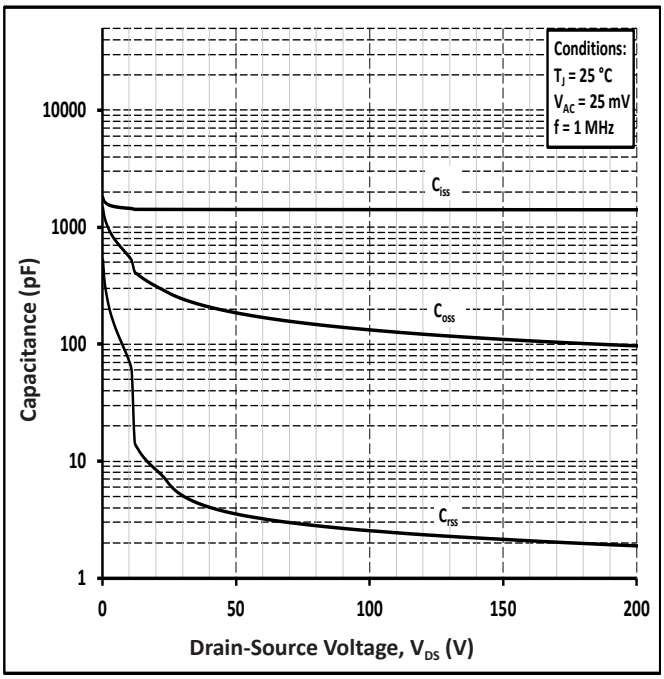



Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

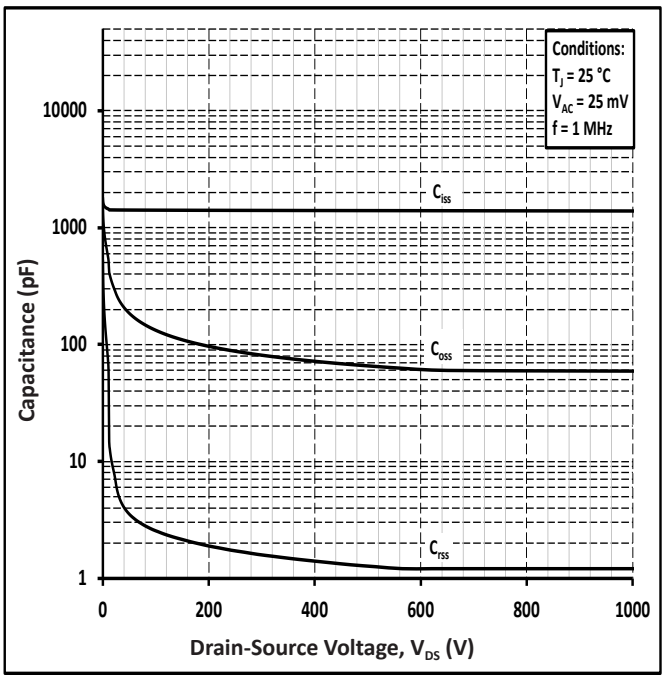



Figure 18. Capacitances vs Drain-Source Voltage (0-1000 V)

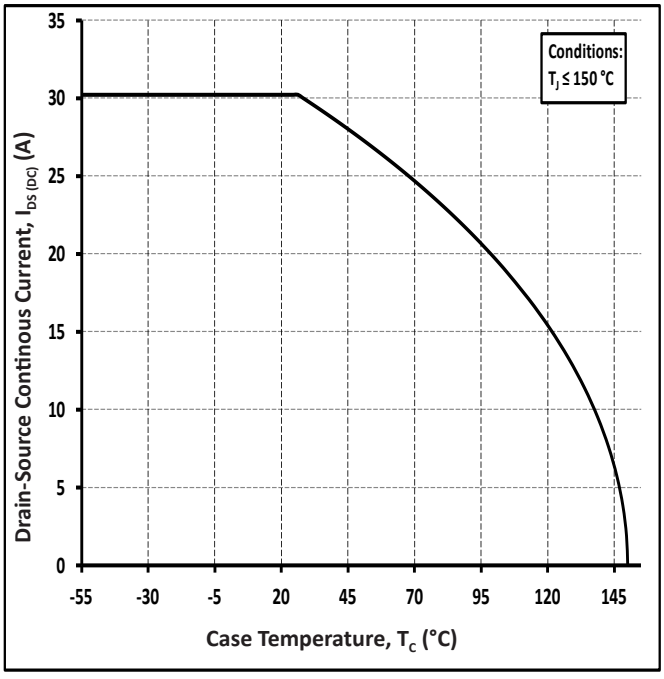



Figure 19. Continuous Drain Current Derating vs Case Temperature

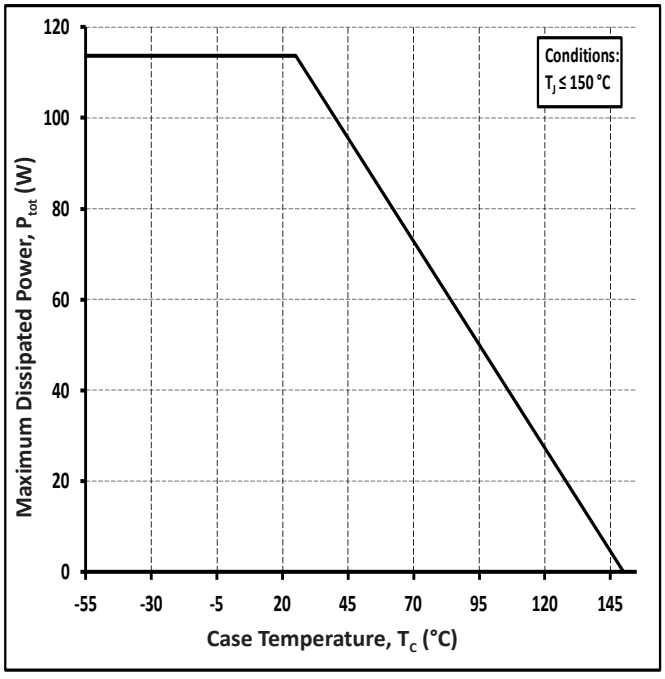



Figure 20. Maximum Power Dissipation Derating vs Case Temperature

## Typical Performance

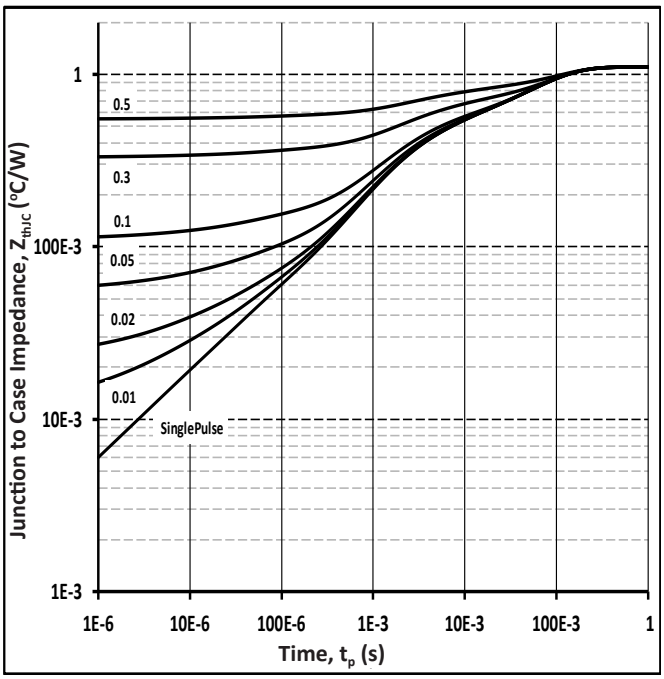



Figure 21. Transient Thermal Impedance (Junction - Case)

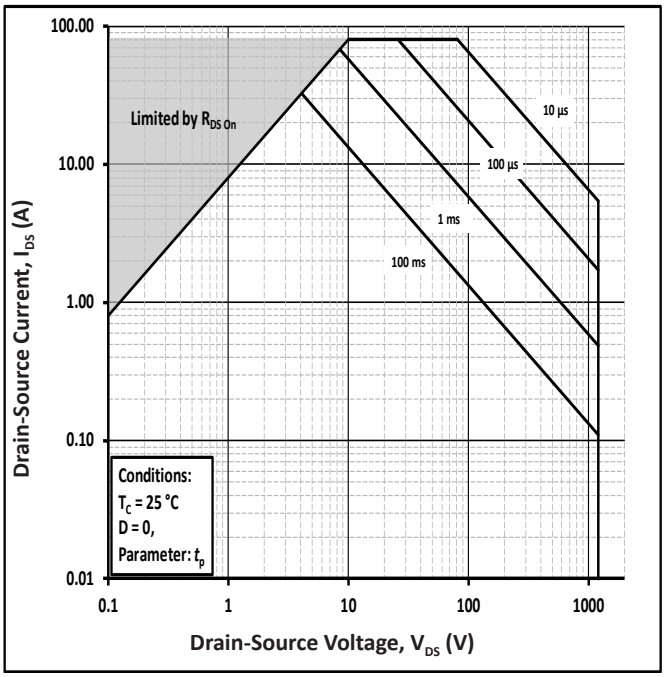



Figure 22. Safe Operating Area

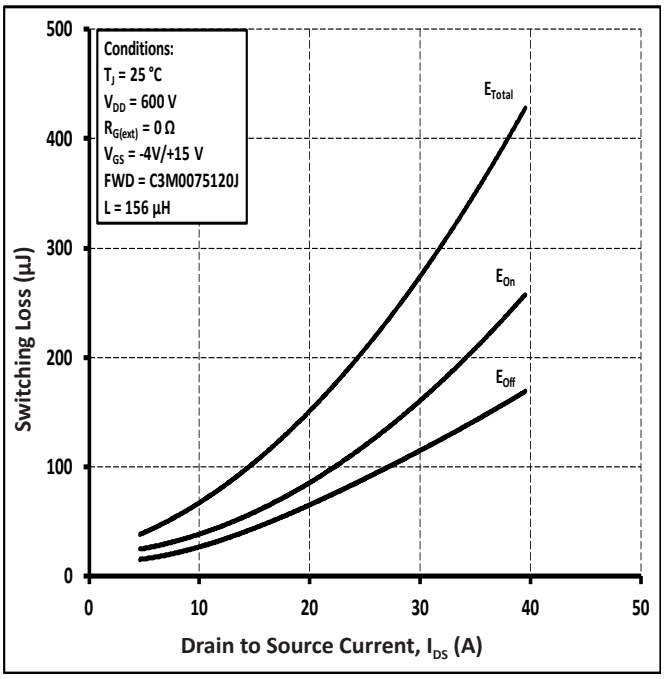



Figure 23. Clamped Inductive Switching Energy vs Drain Current ($V_{DD}$ = 600 V)

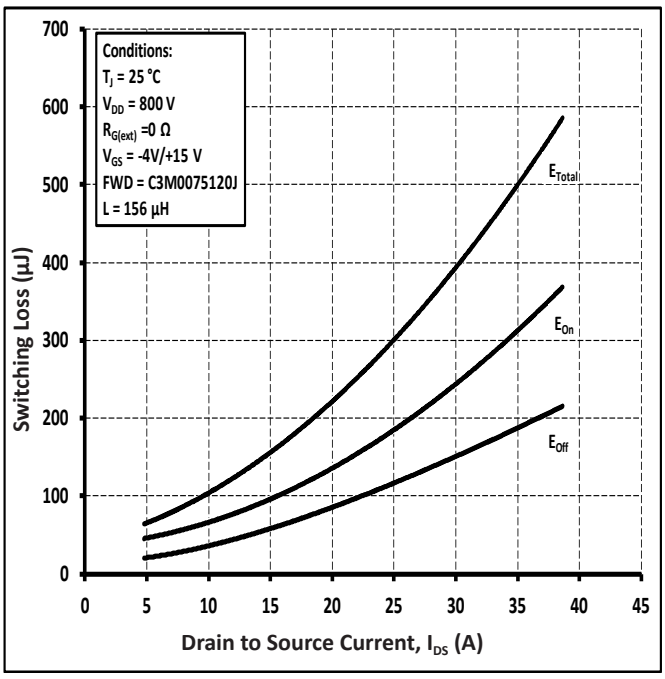



Figure 24. Clamped Inductive Switching Energy vs Drain Current ($V_{DD}$ = 800 V)

## Typical Performance

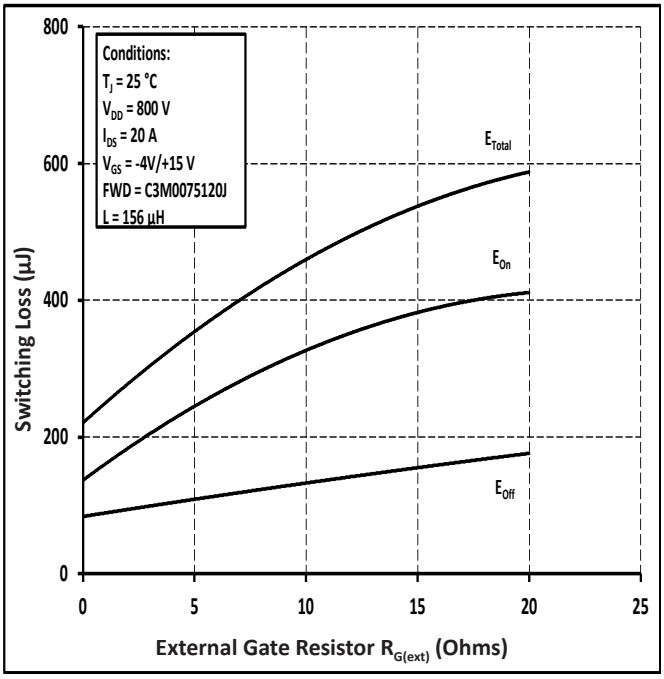



Figure 25. Clamped Inductive Switching Energy vs $R_{G(ext)}$

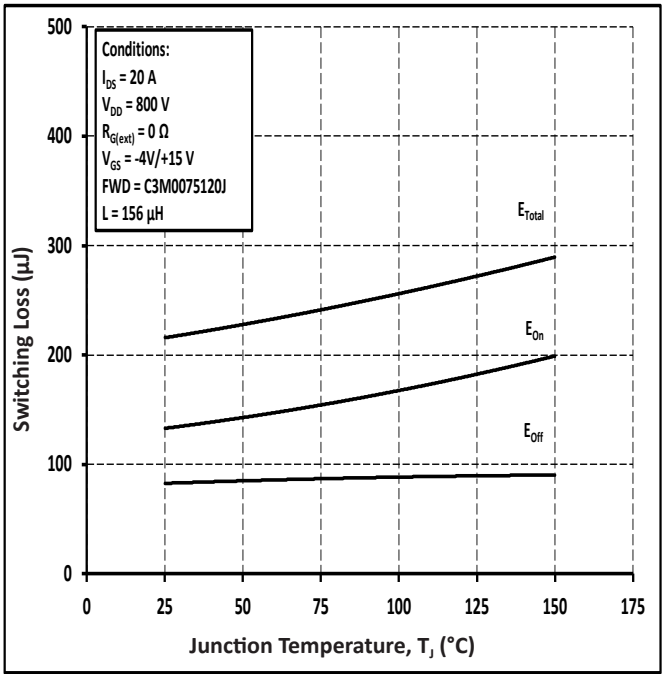



Figure 26. Clamped Inductive Switching Energy vs Temperature

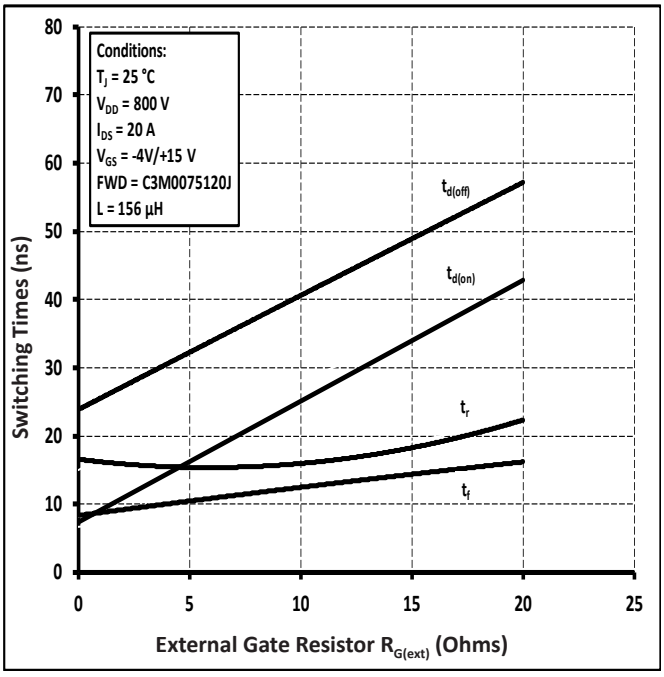



Figure 27. Switching Times vs $R_{G(ext)}$

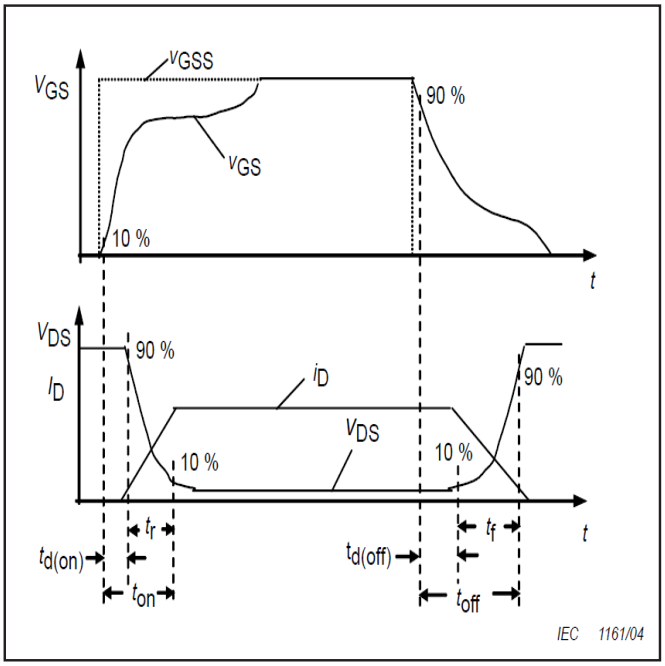



Figure 28. Switching Times Definition

## Test Circuit Schematic

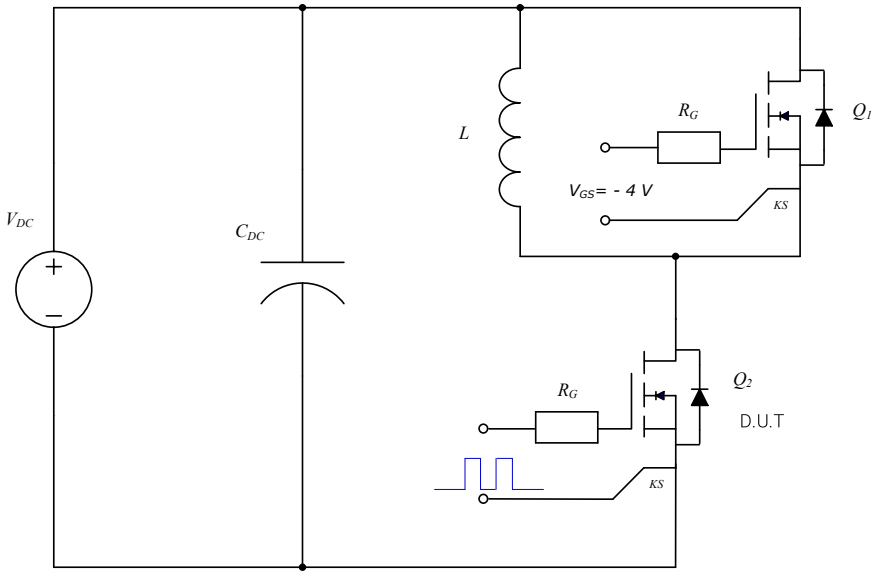
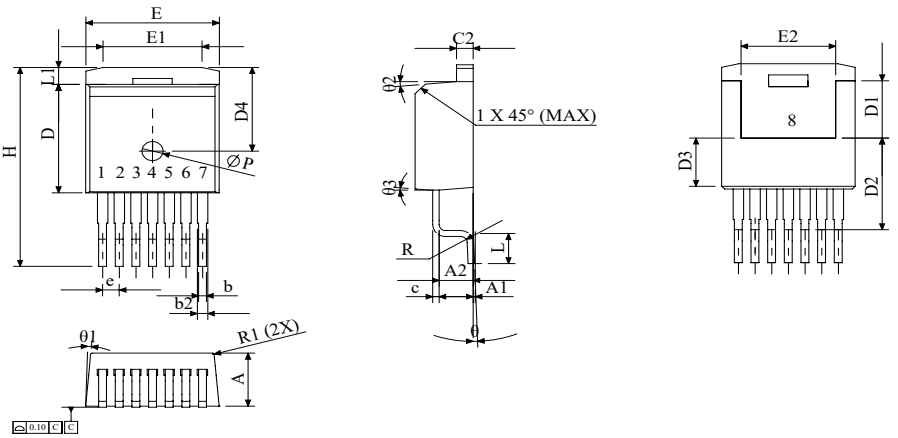



Figure 29. Clamped Inductive Switching Waveform Test Circuit

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET body diode as shown above.

## Package Dimensions

Package: TO-263-7L




| SYMBOL | MIN (mm) | MAX (mm) |
|---|---|---|
| A | 4.30 | 4.57 |
| A1 | 0.00 | 0.25 |
| b | 0.50 | 0.70 |
| b2 | 0.60 | 1.00 |
| c | 0.33 | 0.65 |
| C2 | 1.17 | 1.40 |
| D | 9.025 | 9.125 |
| D1 | 4.70 | 4.90 |
| D2 | 7.170 REF | |
| D3 | 4.000 REF | |
| D4 | 7.000 REF | |
| A2 | 2.595 REF | |
| E | 10.13 | 10.23 |
| E1 | 6.50 | 8.60 |
| E2 | 6.778 | 7.665 |
| e | 1.27 TYP | |
| H | 15.043 | 17.313 |
| L | 2.324 | 2.700 |
| L1 | 0.968 | 1.868 |
| R | 0.506 REF | |
| R1 | 0.500 REF | |
| θ | 0° | 8° |
| θ1 | 4.5° | 5.5° |
| θ2 | 4° | 6° |
| θ3 | 4° | 6° |

| | |
|---|---|
| 1 | GATE |
| 2 | KELVIN |
| 3 | SOURCE |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | DRAIN |

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

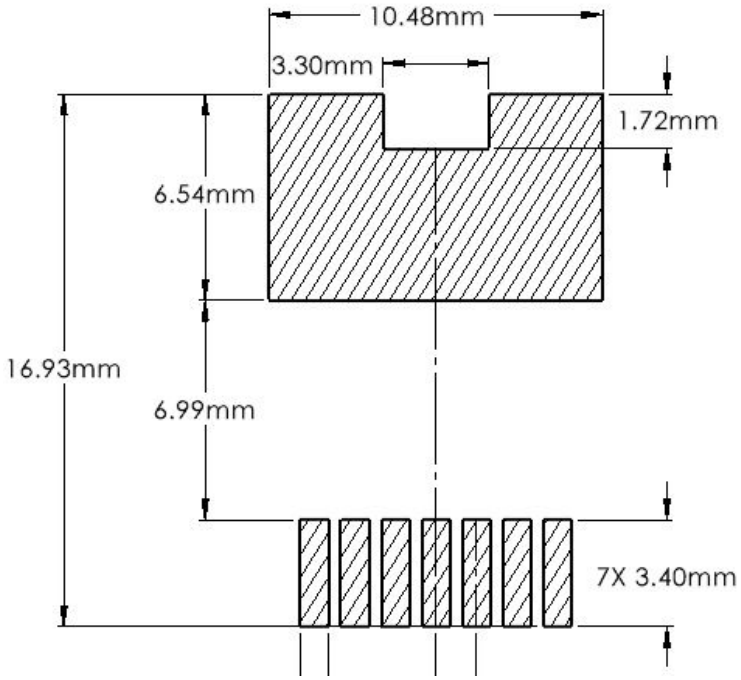
Wolfspeed

TITLE: PACKAGE OUTLINE DRAWING: TO 263-7L J

REVISION NO. 02 | A4

Date: 08/12/25 | PRD-05972 | SCALE:1:1 | SHEET 1 OF 1

## Recommended Solder Pad Layout




## Revision History

| Current Revision | Date of Release | Description of Changes |
|---|---|---|
| B | July-2019 | N/A |
| 3 | December-2023 | Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised |
| 4 | December - 2024 | Legal Disclaimer Updated |
| 5 | September - 2025 | Package drawing updated to correct dimension D1 |

## Related Links

- SiC MOSFET Isolated Gate Driver reference design
- SiC MOSFET Evaluation Board

## Notes & Disclaimer

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