

ESP32-S3-PICO-1 Series

Datasheet

2.4 GHz Wi-Fi + Bluetooth® LE SiP

Supporting IEEE 802.11 b/g/n (2.4 GHz Wi-Fi) and Bluetooth® 5 (LE)

Integrating all peripheral components in one single package

Including:

ESP32-S3-PICO-1-N8R2

ESP32-S3-PICO-1-N8R8



Preliminary 0.1
Espressif Systems
Copyright © 2022

Product Overview

ESP32-S3-PICO-1 is a System-in-Package (SiP) device that is based on ESP32-S3 with integrated 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). It integrates an up to 8 MB SPI flash and an up to 8 MB SPI PSRAM.

ESP32-S3-PICO-1 provides complete Wi-Fi and Bluetooth® functionalities, integrates all peripheral components seamlessly, including a crystal oscillator, filter capacitors, SPI flash/PSRAM, and RF matching links in a single package. Given no other peripheral components are involved, the welding and testing for extra peripheral components is not required. As such, ESP32-S3-PICO-1 reduces the complexity of supply chain and improves control efficiency.

With its ultra-small size, robust performance and low-energy consumption, ESP32-S3-PICO-1 is well suited for any space-limited or battery-operated applications, such as wearable electronics, medical equipment, sensors and other IoT products.

At the core of ESP32-S3-PICO-1 is the ESP32-S3 chip, which consists of high-performance dual-core microprocessor (Xtensa® 32-bit LX7), a low power coprocessor, a Wi-Fi baseband, a Bluetooth LE baseband, RF module, and numerous peripherals. For more details on ESP32-S3, please refer to [ESP32-S3 Series Datasheet](#).

Block Diagram

The block diagram of ESP32-S3-PICO-1 is shown below.

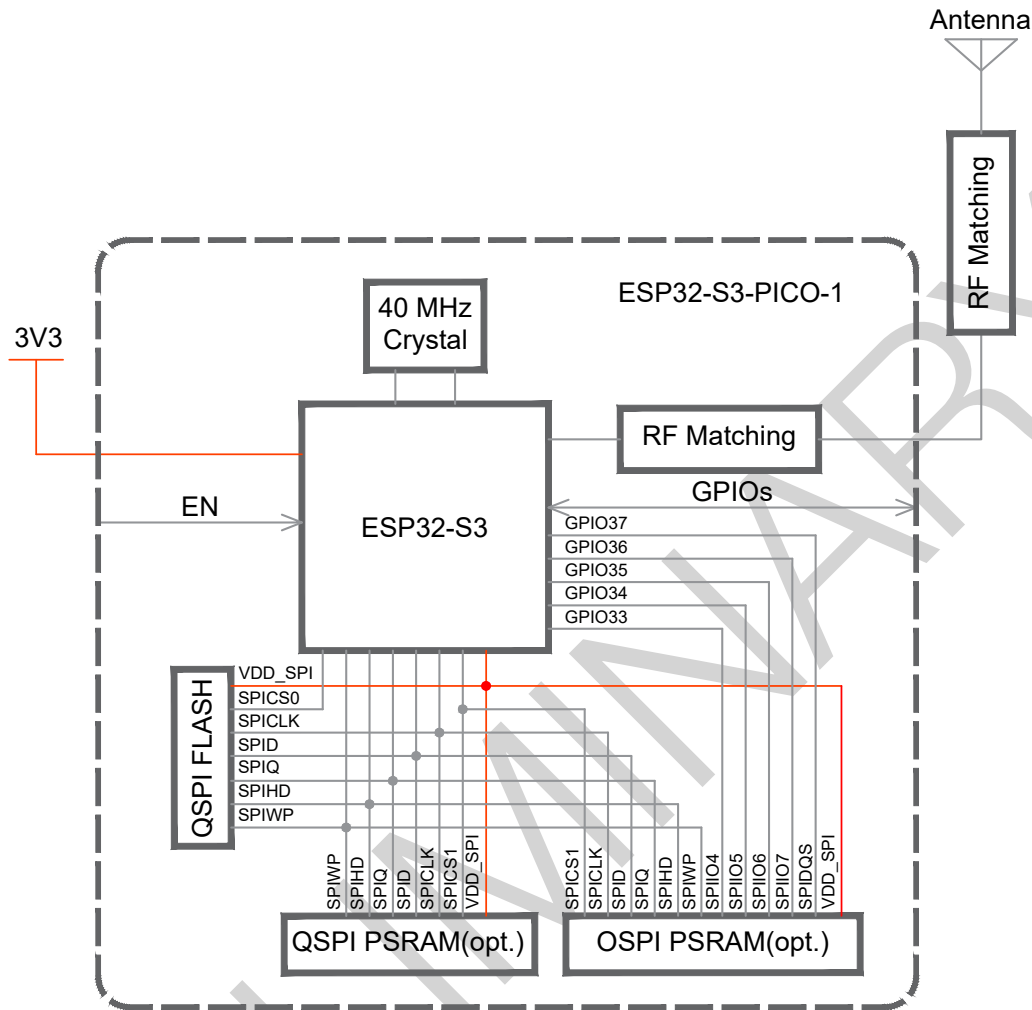


Figure 0-1. ESP32-S3-PICO-1 Block Diagram

Features

CPU and Memory

- ESP32-S3 SoC embedded, Xtensa® dual-core 32-bit LX7 microprocessor, up to 240 MHz
- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps

- A-MPDU and A-MSDU aggregation
- 0.4 μ s guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets

- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Peripherals

- GPIO, SPI, LCD interface, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, USB 1.1 OTG, USB Serial/JTAG controller, MCPWM, SDIO host, GDMA, TWAI® controller (compatible with ISO 11898-1), ADC, touch sensor, temperature sensor, timers and watchdogs

Integrated Components

- 40 MHz crystal oscillator
- Up to 8 MB Quad SPI flash
- Up to 8 MB PSRAM

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature:
 - ESP32-S3-PICO-1-N8R2: -40 ~ 85 °C
 - ESP32-S3-PICO-1-N8R8: -40 ~ 65 °C

Applications (A Nonexhaustive List)

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://www.espressif.com/documentation/esp32-s3-pico-1_datasheet_en.pdf



Contents

Product Overview

Block Diagram	2
Features	3
Applications	4

1 ESP32-S3-PICO-1 Series Comparison

1.1 ESP32-S3-PICO-1 Series Nomenclature	8
1.2 Comparison	8

2 Pin Definition

2.1 Pin Layout	9
2.2 Pin Description	9
2.3 Pin Name Description	10
2.4 Strapping Pins	13

3 Electrical Characteristics

3.1 Absolute Maximum Ratings	16
3.2 Recommended Operating Conditions	16
3.3 VDD_SPI Output Characteristics	16

4 Schematics

5 Peripheral Schematics

6 Packaging

7 Product Handling

7.1 Storage Conditions	21
7.2 Reflow Profile	21
7.3 Ultrasonic Vibration	21

8 Related Documentation and Resources

Revision History

List of Tables

1-1	ESP32-S3-PICO-1 Series Comparison	8
2-1	Pin Description	10
2-2	Pin Name Description	13
2-3	JTAG Signal Source Selection	14
2-4	Strapping Pins	14
2-5	The Default Value for VDD_SPI Voltage	15
2-6	Parameter Descriptions of Setup and Hold Times for the Strapping Pin	15
3-1	Absolute Maximum Ratings	16
3-2	Recommended Operating Conditions	16
3-3	VDD_SPI Output Characteristics	17

List of Figures

0-1	ESP32-S3-PICO-1 Block Diagram	3
1-1	ESP32-S3-PICO-1 Series Nomenclature	8
2-1	ESP32-S3-PICO-1 Pin Layout (Top View)	9
2-2	Setup and Hold Times for the Strapping Pin	15
4-1	ESP32-S3-PICO-1 Schematics	18
5-1	ESP32-S3-PICO-1 Peripheral Schematics	19
6-1	LGA56 (7x7 mm) Package	20
7-1	Reflow Profile	21

1 ESP32-S3-PICO-1 Series Comparison

1.1 ESP32-S3-PICO-1 Series Nomenclature

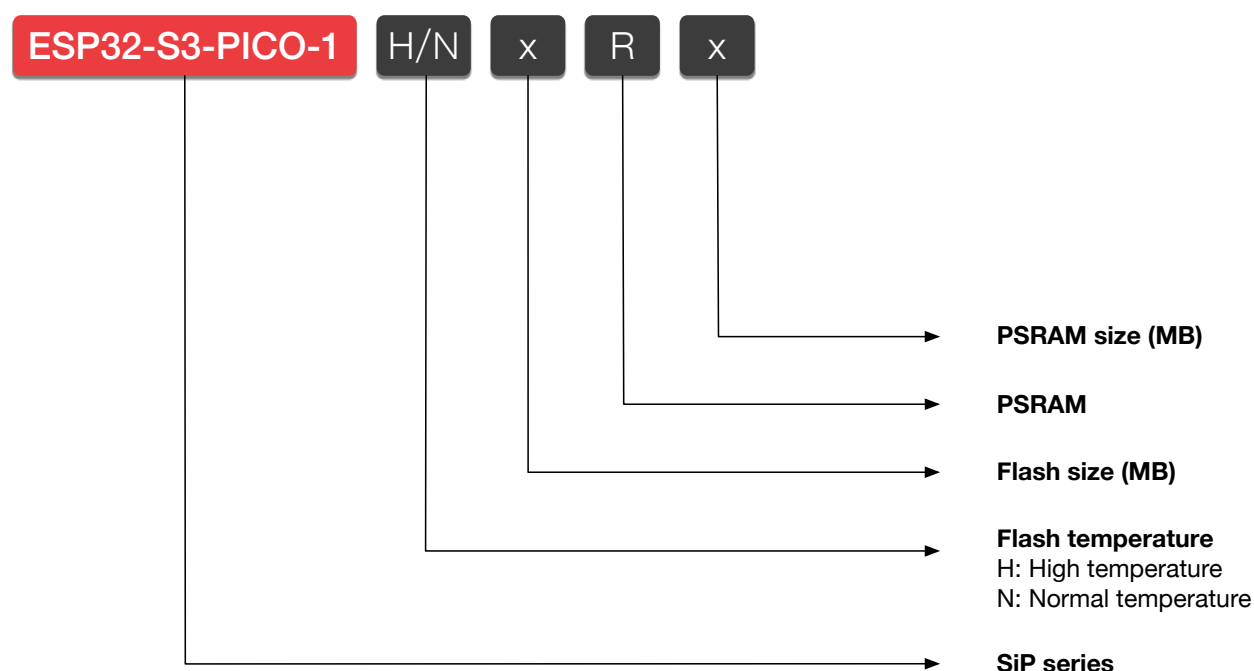


Figure 1-1. ESP32-S3-PICO-1 Series Nomenclature

1.2 Comparison

Table 1-1. ESP32-S3-PICO-1 Series Comparison

Ordering Code	In-package flash	In-package PSRAM	Ambient Temperature (°C) ²	SPI Voltage
ESP32-S3-PICO-1-N8R2	8 MB (Quad SPI)	2 MB (Quad SPI)	−40 ~ 85	3.3 V
ESP32-S3-PICO-1-N8R8	8 MB (Quad SPI)	8 MB (Octal SPI)	−40 ~ 65	3.3 V

2 Pin Definition

2.1 Pin Layout

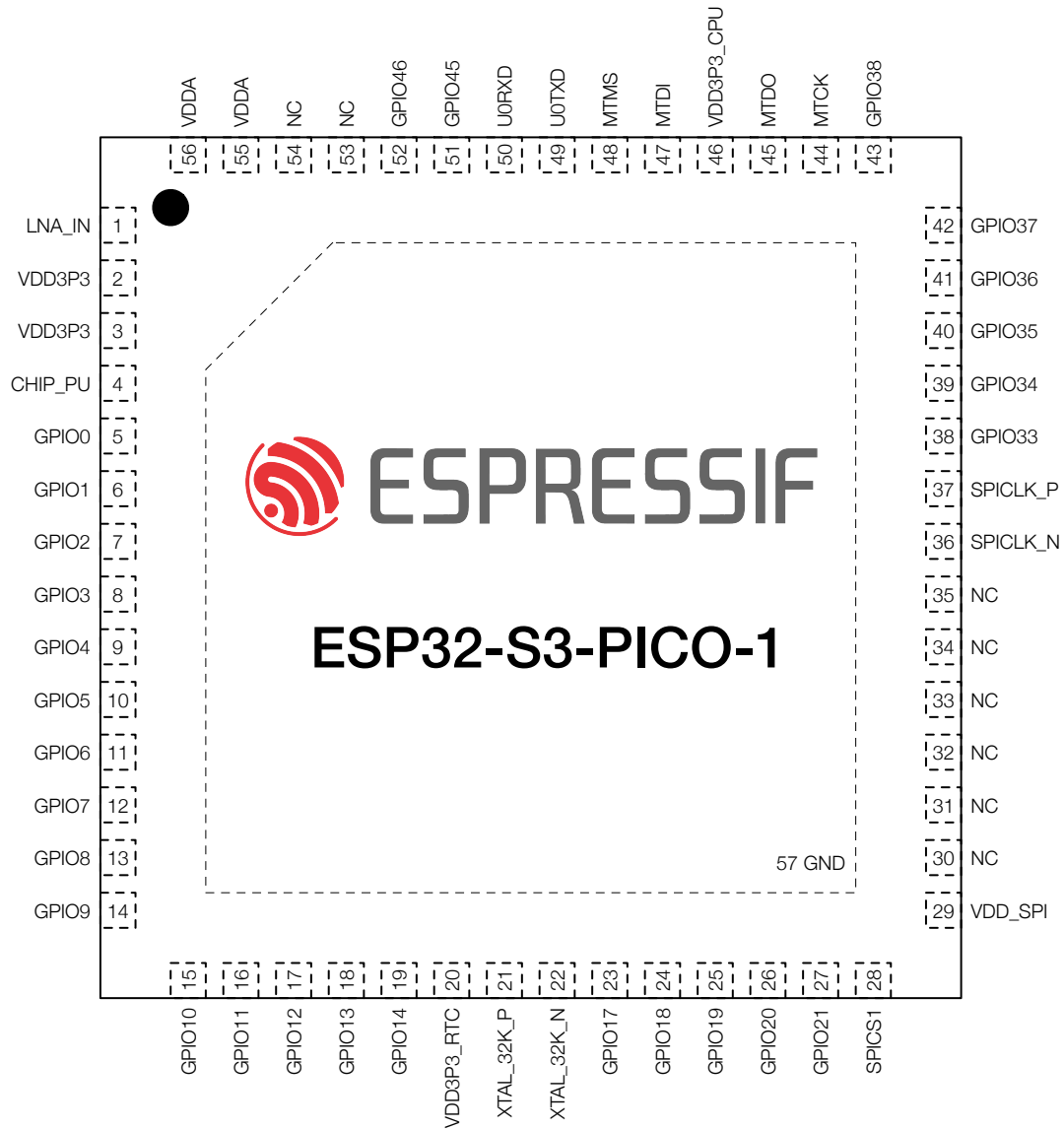


Figure 2-1. ESP32-S3-PICO-1 Pin Layout (Top View)

2.2 Pin Description

Table 2-1. Pin Description

Name	No.	Type ¹	Power Domain	Function ^{2, 5}
LNA_IN	1	I/O	—	Low Noise Amplifier (RF LNA) input and output signal
VDD3P3	2	P _A	—	Analog power supply
VDD3P3	3	P _A	—	Analog power supply
CHIP_PU	4	I	VDD3P3_RTC	High: on, enables ESP32-S3-PICO-1. Low: off, ESP32-S3-PICO-1 powers off. Note: Do not leave the CHIP_PU pin floating.
GPIO0	5	I/O/T	VDD3P3_RTC	RTC_GPIO0, GPIO0
GPIO1	6	I/O/T	VDD3P3_RTC	RTC_GPIO1, GPIO1 , TOUCH1, ADC1_CH0
GPIO2	7	I/O/T	VDD3P3_RTC	RTC_GPIO2, GPIO2 , TOUCH2, ADC1_CH1
GPIO3	8	I/O/T	VDD3P3_RTC	RTC_GPIO3, GPIO3 , TOUCH3, ADC1_CH2
GPIO4	9	I/O/T	VDD3P3_RTC	RTC_GPIO4, GPIO4 , TOUCH4, ADC1_CH3
GPIO5	10	I/O/T	VDD3P3_RTC	RTC_GPIO5, GPIO5 , TOUCH5, ADC1_CH4
GPIO6	11	I/O/T	VDD3P3_RTC	RTC_GPIO6, GPIO6 , TOUCH6, ADC1_CH5
GPIO7	12	I/O/T	VDD3P3_RTC	RTC_GPIO7, GPIO7 , TOUCH7, ADC1_CH6
GPIO8	13	I/O/T	VDD3P3_RTC	RTC_GPIO8, GPIO8 , TOUCH8, ADC1_CH7, SUBSPICS1
GPIO9	14	I/O/T	VDD3P3_RTC	RTC_GPIO9, GPIO9 , TOUCH9, ADC1_CH8, SUBSPIHD, FSPIHD
GPIO10	15	I/O/T	VDD3P3_RTC	RTC_GPIO10, GPIO10 , TOUCH10, ADC1_CH9, FSPIIO4, SUBSPICS0, FSPICS0
GPIO11	16	I/O/T	VDD3P3_RTC	RTC_GPIO11, GPIO11 , TOUCH11, ADC2_CH0, FSPIIO5, SUBSPID, FSPID
GPIO12	17	I/O/T	VDD3P3_RTC	RTC_GPIO12, GPIO12 , TOUCH12, ADC2_CH1, FSPIIO6, SUBSPICLK, FSPICLK
GPIO13	18	I/O/T	VDD3P3_RTC	RTC_GPIO13, GPIO13 , TOUCH13, ADC2_CH2, FSPIIO7, SUBSPIQ, FSPIQ
GPIO14	19	I/O/T	VDD3P3_RTC	RTC_GPIO14, GPIO14 , TOUCH14, ADC2_CH3, FSPIDQS, SUBSPIWP, FSPWP
VDD3P3_RTC	20	P _A	—	Analog power supply
XTAL_32K_P	21	I/O/T	VDD3P3_RTC	RTC_GPIO15, GPIO15 , U0RTS, ADC2_CH4, XTAL_32K_P
XTAL_32K_N	22	I/O/T	VDD3P3_RTC	RTC_GPIO16, GPIO16 , U0CTS, ADC2_CH5, XTAL_32K_N
GPIO17	23	I/O/T	VDD3P3_RTC	RTC_GPIO17, GPIO17 , U1TXD, ADC2_CH6

Name	No.	Type ¹	Power Domain	Function ^{2, 5}
GPIO18	24	I/O/T	VDD3P3_RTC	RTC_GPIO18, GPIO18 , U1RXD, ADC2_CH7, CLK_OUT3
GPIO19	25	I/O/T	VDD3P3_RTC	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
GPIO20	26	I/O/T	VDD3P3_RTC	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
GPIO21	27	I/O/T	VDD3P3_RTC	RTC_GPIO21, GPIO21
SPICS1 ⁴	28	I/O/T	VDD_SPI	SPICS1, GPIO26
VDD_SPI	29	P _D	—	Output power supply: VDD3P3_RTC
NC	30	—	—	NC
NC	31	—	—	NC
NC	32	—	—	NC
NC	33	—	—	NC
NC	34	—	—	NC
NC	35	—	—	NC
SPICLK_N	36	I/O/T	VDD_SPI	SPICLK_N_DIFF, GPIO48 , SUBSPICLK_N_DIFF
SPICLK_P	37	I/O/T	VDD_SPI	SPICLK_P_DIFF, GPIO47 , SUBSPICLK_P_DIFF
GPIO33 ^{3, 4}	38	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO4, GPIO33 , FSPIHD, SUBSPIHD
GPIO34 ^{3, 4}	39	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO5, GPIO34 , FSPICS0, SUBSPICS0
GPIO35 ^{3, 4}	40	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO6, GPIO35 , FSPID, SUBSPID
GPIO36 ^{3, 4}	41	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO7, GPIO36 , FSPICLK, SUBSPICLK
GPIO37 ^{3, 4}	42	I/O/T	VDD3P3_CPU / VDD_SPI	SPIDQS, GPIO37 , FSPIQ, SUBSPIQ
GPIO38	43	I/O/T	VDD3P3_CPU	GPIO38 , FSPIWP, SUBSPIWP
MTCK	44	I/O/T	VDD3P3_CPU	MTCK , GPIO39, CLK_OUT3, SUBSPICS1
MTDO	45	I/O/T	VDD3P3_CPU	MTDO , GPIO40, CLK_OUT2
VDD3P3_CPU	46	P _D	—	Input power supply for CPU IO
MTDI	47	I/O/T	VDD3P3_CPU	MTDI , GPIO41, CLK_OUT1
MTMS	48	I/O/T	VDD3P3_CPU	MTMS , GPIO42
U0TXD	49	I/O/T	VDD3P3_CPU	U0TXD , GPIO43, CLK_OUT1
U0RXD	50	I/O/T	VDD3P3_CPU	U0RXD , GPIO44, CLK_OUT2
GPIO45	51	I/O/T	VDD3P3_CPU	GPIO45
GPIO46	52	I/O/T	VDD3P3_CPU	GPIO46

Name	No.	Type ¹	Power Domain	Function ^{2, 5}
NC	53	—	—	NC
NC	54	—	—	NC
VDDA1	55	P _A	—	Analog power supply
VDDA2	56	P _A	—	Analog power supply
GND	57	G	—	Ground

¹ P: power pin; P_A: analog power pin; P_D: digital power pin; I: input; O: output; T: high impedance; NC: no component.

² Pin functions in bold font are the default pin functions in SPI Boot mode. For pins No.38 ~ 42, the default function is decided by eFuse bit.

³ Power supply for GPIO33, GPIO34, GPIO35, GPIO36 and GPIO37 is configurable to be either VDD3P3_CPU (default) or VDD_SPI.

⁴ For ESP32-S3-PICO-1-N8R2, SPICS1 is connected to the Quad SPI PSRAM and is not available for other uses. For ESP32-S3-PICO-1-N8R8, SPICS1 and GPIO33 ~ GPIO37 are connected to the Octal SPI PSRAM and are not available for other uses.

⁵ The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to [ESP32-S3 Technical Reference Manual](#).

2.3 Pin Name Description

The explanation of each pin name is briefly described below.

Table 2-2. Pin Name Description

Pin Name	Description
GPIOx	General-purpose input and output (x is GPIO number). GPIO pins can be assigned various functions, including digital and analog functions.
XTAL_32K_P/N	32 KHz external clock input/output (connecting to ESP32-S3-PICO-1's oscillator). P/N means differential clock positive/negative.
U0RXD/U0TXD	UART0 receive/transmit signals.
MTCK/MTDO/MTDI/MTMS	JTAG interface signals.
LNA_IN	Low-Noise Amplifier (RF LNA) input/output signals.
CHIP_PU	Power up pin.
GND	External ground connection.
VDDA	Power supply for analog domain.
VDD3P3_RTC	Power supply for RTC digital domain.
VDD3P3_CPU	Power supply for digital domain.
VDD_SPI	Power supply for SPI IOs.

2.4 Strapping Pins

ESP32-S3-PICO-1 has four strapping pins:

- GPIO0
- GPIO45
- GPIO46
- GPIO3

Software can read the values of corresponding bits from register "GPIO_STRAPPING".

During ESP32-S3-PICO-1's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until ESP32-S3-PICO-1 is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to ESP32-S3-PICO-1's internal weak pull-up/pull-down during ESP32-S3-PICO-1 reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

GPIO3 is floating by default. Its strapping value can be configured to determine the source of the JTAG signal inside the CPU, as shown in Table 2-4. In this case, the strapping value is controlled by the external circuit that cannot be in a high impedance state. Table 2-3 shows more configuration combinations of EFUSE_DIS_USB_JTAG, EFUSE_DIS_PAD_JTAG, and EFUSE_STRAP_JTAG_SEL that determine the JTAG signal source.

Table 2-3. JTAG Signal Source Selection

EFUSE_STRAP_JTAG_SEL	EFUSE_DIS_USB_JTAG	EFUSE_DIS_PAD_JTAG	JTAG Signal Source
1	0	0	Refer to Table 2-4
0	0	0	USB Serial/JTAG controller
don't care	0	1	USB Serial/JTAG controller
don't care	1	0	JTAG pins on SiP
don't care	1	1	N/A

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S3-PICO-1.

After reset, the strapping pins work as normal-function pins.

Refer to Table 2-4 for a detailed configuration of the strapping pins.

Table 2-4. Strapping Pins

VDD_SPI Voltage			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Bootling Mode ¹			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Don't care	0
Enabling/Disabling ROM Messages Print During Bootling ²			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See the 2nd note	See the 2nd note
JTAG Signal Selection			
Pin	Default	EFUSE_DIS_USB_JTAG = 0, EFUSE_DIS_PAD_JTAG = 0, EFUSE_STRAP_JTAG_SEL=1	
GPIO3	N/A	0: JTAG signal from JTAG pins on SiP 1: JTAG signal from USB Serial/JTAG controller	

Note:

1. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
2. By default, the ROM boot messages are printed over UART0 (U0TXD pin) and USB Serial/JTAG controller together. The ROM code printing can be disabled through configuration register and eFuse. For detailed information, please refer to Chapter [Chip Boot Control](#) in *ESP32-S3 Technical Reference Manual*.

VDD_SPI voltage is determined either by the strapping value of GPIO45 or by EFUSE_VDD_SPI_TIEH. When EFUSE_VDD_SPI_FORCE is 0, VDD_SPI voltage is determined by the strapping value of GPIO45; when EFUSE_VDD_SPI_FORCE is 1, VDD_SPI voltage is determined by EFUSE_VDD_SPI_TIEH. Please refer to the following table for default configurations:

Table 2-5. The Default Value for VDD_SPI Voltage

SiP Variant	EFUSE_VDD_SPI_FORCE	EFUSE_VDD_SPI_TIEH	VDD_SPI Voltage
ESP32-S3-PICO-1-N8R2	1	1	Force to 3.3 V
ESP32-S3-PICO-1-N8R8	1	1	Force to 3.3 V

Figure 2-2 shows the setup and hold times for the strapping pin before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 2-6.

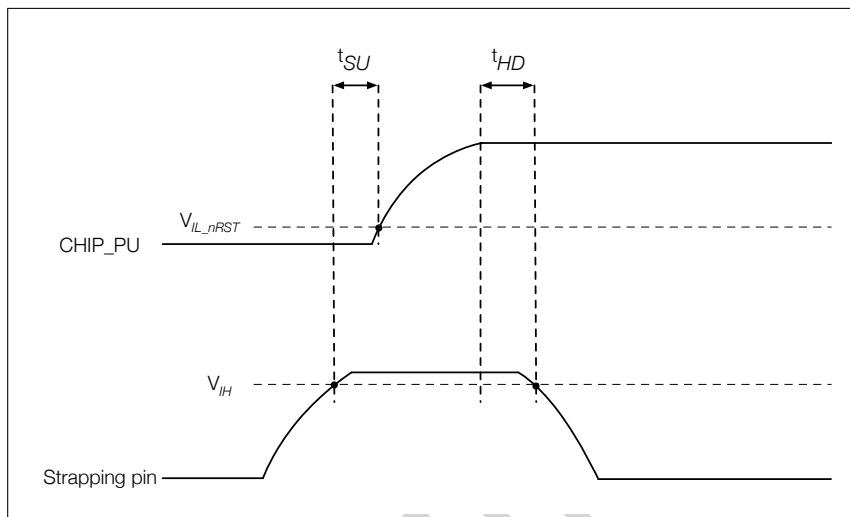


Figure 2-2. Setup and Hold Times for the Strapping Pin

Table 2-6. Parameter Descriptions of Setup and Hold Times for the Strapping Pin

Parameter	Description	Min (ms)
t_{SU}	Setup time before CHIP_PU goes from low to high	0
t_{HD}	Hold time after CHIP_PU goes high	3

Note:

The values presented in this section are **preliminary** and may change with the final release of this datasheet.

3.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device.

Table 3-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SPI	Voltage applied to power supply pins per power domain	-0.3	3.6	V
I_{output}^*	Cumulative IO output current	—	1500	mA
T_{STORE}	Storage temperature	-40	150	°C

* The ESP32-S3-PICO-1 series worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SPI) output high logic level to ground.

3.2 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA, VDD3P3 VDD3P3_RTC	Voltage applied to power supply pins per power domain	3.0	3.3	3.6	V
VDD_SPI (working as input power supply)	—	3.0	3.3	3.6	V
VDD3P3_CPU ^{1, 2}	Voltage applied to power supply pin	3.0	3.3	3.6	V
I_{VDD}^3	Current delivered by external power supply	0.5	—	—	A
T_A	Ambient temperature	-40	—	85	°C
				65	

¹ When writing to eFuses, VDD3P3_CPU should not exceed 3.3 V.

² When VDD_SPI is used to drive peripherals, VDD3P3_CPU should comply with the peripherals' specifications. For more information, please refer to Table 3-3.

³ If you use a single power supply, the recommended output current is 500 mA or more.

⁴ For ESP32-S3-PICO-1-N8R8, if the PSRAM ECC function is enabled, the maximum ambient temperature can be improved to 85 °C, while the usable size of PSRAM will be reduced by 1/16.

3.3 VDD_SPI Output Characteristics

Table 3-3. VDD_SPI Output Characteristics

Symbol	Parameter	Typ	Unit
R_{SPI}	On-resistance in 3.3 V mode	14	Ω

In real-life applications, when VDD_SPI works in 3.3 V output mode, VDD3P3_CPU may be affected by R_{SPI} . For example, when VDD3P3_CPU is used to drive a 3.3 V flash, it should comply with the following specifications:

$$VDD3P3_CPU > VDD_flash_min + I_flash_max * R_{SPI}$$

Among which, VDD_flash_min is the minimum operating voltage of the flash, and I_flash_max the maximum current.

The schematic diagram illustrates the internal circuitry of the ESP32-S3-PICO-1-N8R2 module. The central component is the ESP32-S3 chip (U1), which is connected to various external components. The power supply section includes VDDA and VDD3P3 pins, with decoupling capacitors C1 through C15. A 40MHz crystal (Y1) is connected to the XTAL pins. The chip is connected to a PSRAM (opt.) (U4) via SPI0, SPIQ, and SPIWP pins. The diagram also shows connections for the LNA_IN, CHIP_PU, and various GPIO pins. A pin mapping table is provided on the right side of the diagram.

ESP32-S3	ESP32-S3-PICO-1
LNA_IN	LNA_IN
VDD3P3	VDD3P3
VDD3P3	VDD3P3
CHIP_PU	CHIP_PU
GPIO0	GPIO0
GPIO1	GPIO1
GPIO2	GPIO2
GPIO3	GPIO3
GPIO4	GPIO4
GPIO5	GPIO5
GPIO6	GPIO6
GPIO7	GPIO7
GPIO8	GPIO8
GPIO9	GPIO9
GPIO10	GPIO10
GPIO11	GPIO11
GPIO12	GPIO12
GPIO13	GPIO13
GPIO14	GPIO14
VDD3P3_RTC	VDD3P3_RTC
XTAL_32K_P	XTAL_32K_P
XTAL_32K_N	XTAL_32K_N
GPIO17	GPIO17
GPIO18	GPIO18
GPIO19	GPIO19
GPIO20	GPIO20
GPIO21	GPIO21
SPI0	SPI0
SPIQ	SPIQ
SPIWP	SPIWP
SPIHD	SPIHD
VDD_SPI	VDD_SPI
SPIBD	NC
SPIWP	NC
SPICS0	NC
SPICLK	NC
SPIQ	NC
SPID	NC
SPICLK_N	SPICLK_N
SPICLK_P	SPICLK_P
GPIO33	GPIO33
GPIO34	GPIO34
GPIO35	GPIO35
GPIO36	GPIO36
GPIO37	GPIO37
GPIO38	GPIO38
MTCK	MTCK
MTDO	MTDO
VDD3P3_CPU	VDD3P3_CPU
MTDI	MTDI
U0TXD	U0TXD
U0RXD	U0RXD
GPIO45	GPIO45
GPIO46	GPIO46
XTAL_N	NC
XTAL_P	NC
VDDA	VDDA
VDDA	VDDA

Figure 4-1. ESP32-S3-PICO-1 Schematics

5 Peripheral Schematics

This is the typical application circuit of ESP32-S3-PICO-1 connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

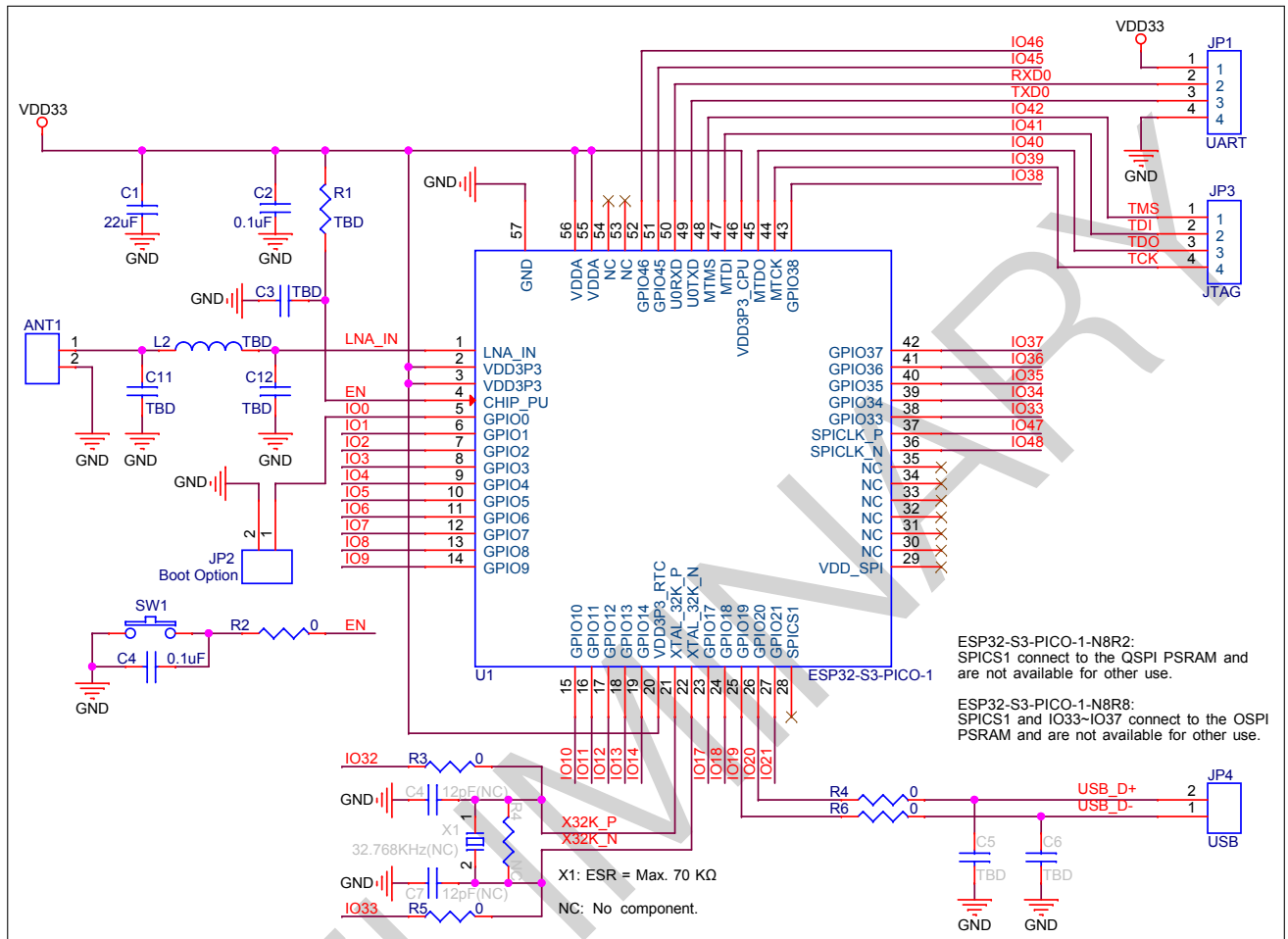


Figure 5-1. ESP32-S3-PICO-1 Peripheral Schematics

Note:

To ensure the power supply to during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually $R = 10\text{ k}\Omega$ and $C = 1\text{ }\mu\text{F}$. However, specific parameters should be adjusted based on the power-up timing and the power-up and reset sequence timing of the SiP. For ESP32-S3-PICO-1's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in [ESP32-S3 Series Datasheet](#).

6 Packaging

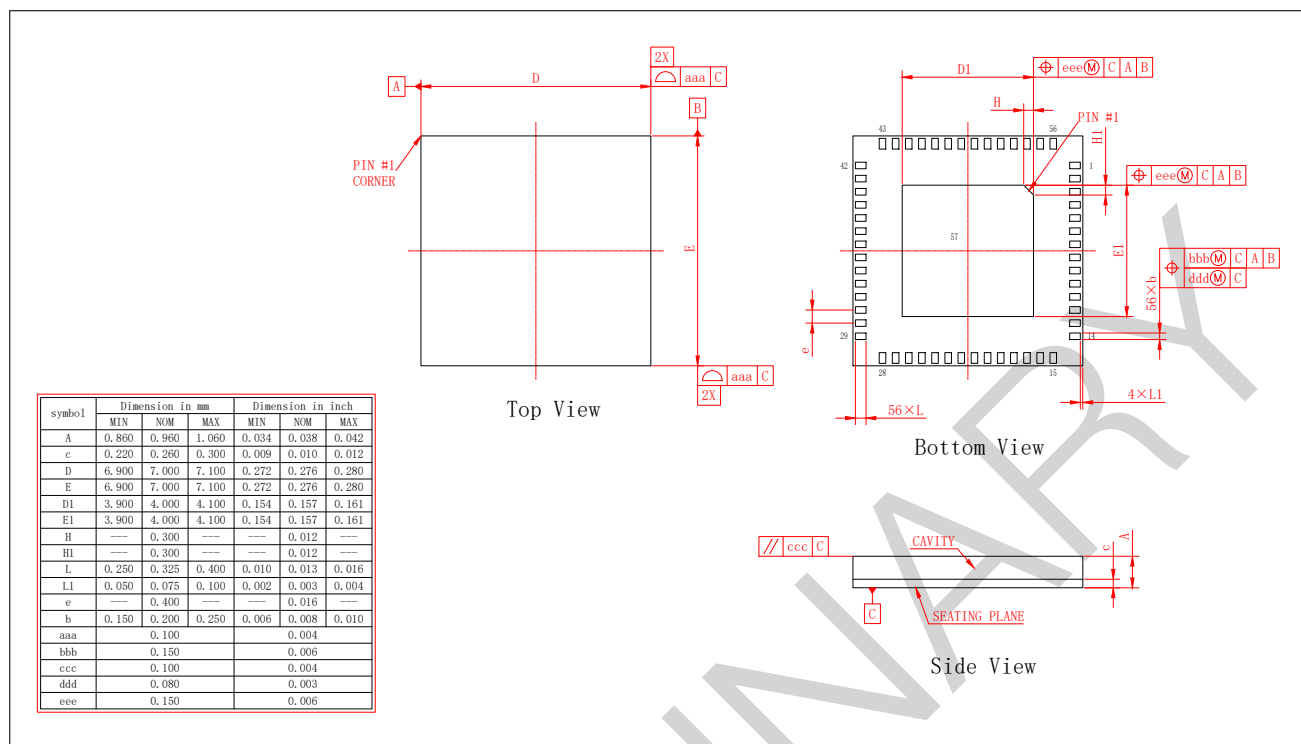


Figure 6-1. LGA56 (7x7 mm) Package

Note:

- The pins of the ESP32-S3-PICO-1 series are numbered in an anti-clockwise direction from Pin 1 in the top view.
- For information about tape, reel, and product marking, please refer to [Espressif Chip Packaging Information](#).

7 Product Handling

7.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of $< 40\text{ }^{\circ}\text{C}$ and $/90\%\text{RH}$. The SiP is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the SiP must be soldered within 168 hours with the factory conditions $25\pm 5\text{ }^{\circ}\text{C}$ and $/60\%\text{RH}$. If the above conditions are not met, the SiP needs to be baked.

7.2 Reflow Profile

Solder the SiP in a single reflow.

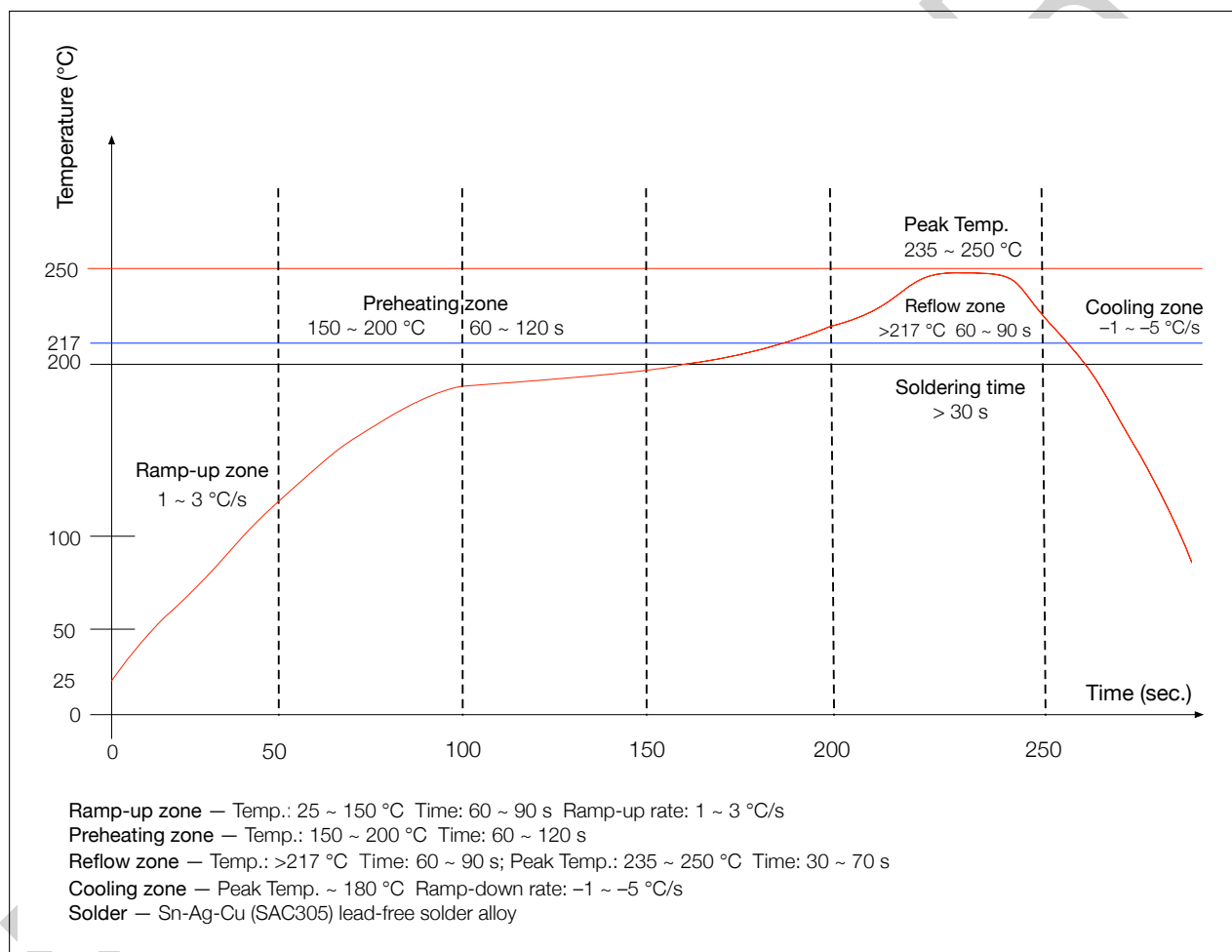


Figure 7-1. Reflow Profile

7.3 Ultrasonic Vibration

Avoid exposing Espressif SiPs to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-SiP crystal and lead to its malfunction or even failure. As a consequence, **the SiP may stop working or its performance may deteriorate.**

8 Related Documentation and Resources

Related Documentation

- [ESP32-S3 Technical Reference Manual](#) – Detailed information on how to use the ESP32-S3 memory and peripherals.
- [ESP32-S3 Hardware Design Guidelines](#) – Guidelines on how to integrate the ESP32-S3 into your hardware product.
- *Certificates*
<https://espressif.com/en/support/documents/certificates>
- *ESP32-S3 Product/Process Change Notifications (PCN)*
<https://espressif.com/en/support/documents/pcns?keys=ESP32-S3>
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
<https://espressif.com/en/support/documents/advisories?keys=ESP32-S3>
- *Documentation Updates and Update Notification Subscription*
<https://espressif.com/en/support/download/documents>

Developer Zone

- [ESP-IDF Programming Guide for ESP32-S3](#) – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
<https://github.com/espressif>
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
<https://esp32.com/>
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
<https://blog.espressif.com/>
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
<https://espressif.com/en/support/download/sdks-demos>

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
<https://espressif.com/en/products/socs?id=ESP32-S3>
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
<https://espressif.com/en/products/modules?id=ESP32-S3>
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
<https://espressif.com/en/products/devkits?id=ESP32-S3>
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
<https://products.espressif.com/#/product-selector?language=en>

Contact Us

- See the tabs *Sales Questions*, *Technical Enquiries*, *Circuit Schematic & PCB Design Review*, *Get Samples* (Online stores), *Become Our Supplier*, *Comments & Suggestions*.
<https://espressif.com/en/contact-us/sales-questions>

Revision History

Date	Version	Release notes
2022-09-23	v0.1	Preliminary

PRELIMINARY



www.espressif.com

Disclaimer and Copyright Notice

Information in this document, including URL references, is subject to change without notice.

ALL THIRD PARTY'S INFORMATION IN THIS DOCUMENT IS PROVIDED AS IS WITH NO WARRANTIES TO ITS AUTHENTICITY AND ACCURACY.

NO WARRANTY IS PROVIDED TO THIS DOCUMENT FOR ITS MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, NOR DOES ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE.

All liability, including liability for infringement of any proprietary rights, relating to use of information in this document is disclaimed. No licenses express or implied, by estoppel or otherwise, to any intellectual property rights are granted herein.

The Wi-Fi Alliance Member logo is a trademark of the Wi-Fi Alliance. The Bluetooth logo is a registered trademark of Bluetooth SIG.

All trade names, trademarks and registered trademarks mentioned in this document are property of their respective owners, and are hereby acknowledged.

Copyright © 2022 Espressif Systems (Shanghai) Co., Ltd. All rights reserved.