24AA02E48/24AA025E48/ 24AA02E64/24AA025E64

2-Kbit I²C Serial EEPROMs with EUI-48™ or EUI-64™ Node Identity

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges	Cascadable	Page Size	Node Address
24AA02E48	1.7V-5.5V	400 kHz(1)	I, E	No	8-Bytes	EUI-48
24AA025E48	1.7V-5.5V	400 kHz(1)	I, E	Yes	16-Bytes	EUI-48
24AA02E64	1.7V-5.5V	400 kHz(1)	I, E	No	8-Bytes	EUI-64
24AA025E64	1.7V-5.5V	400 kHz(1)	I, E	Yes	16-Bytes	EUI-64

Note 1: 100 kHz for VCC <2.5V

Features

- Pre-Programmed Globally Unique, 48-bit or 64-bit Node Address
- Compatible with EUI-48 and EUI-64
- Single Supply with Operation Down to 1.7V
- Low-Power CMOS Technology:
  - Read current: 1 mA, maximum
  - Standby current: – 1 µA, maximum (I-Temp.)
    – 5 µA, maximum (E-Temp.)
- Two-Wire Serial Interface, I²C Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- Page Write Buffer:
  - 8-byte page (24AA02E48/24AA02E64)
  - 16-byte page (24AA025E48/24AA025E64)
- High Reliability:
  - More than one million erase/write cycles
  - Data retention >200 years
  - ESD protection >4,000V
- Factory Programming Available
- RoHS Compliant
- Available for Extended Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- Automotive AEC-Q100 Qualified

Packages

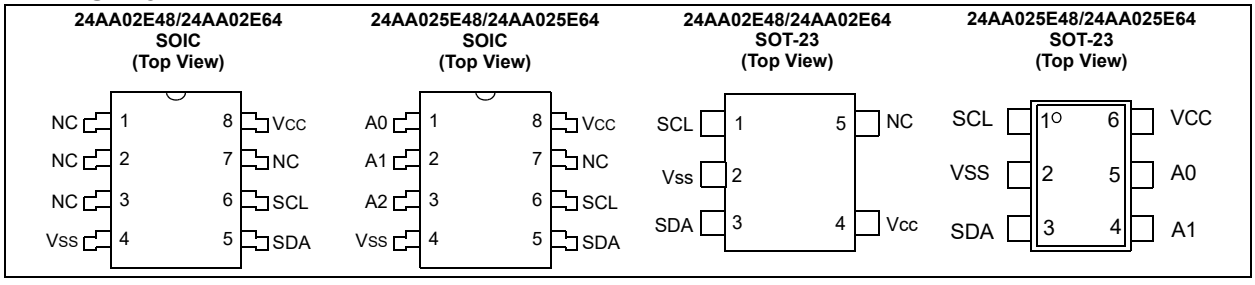
- 8-Lead SOIC, 5-Lead SOT-23 (24AA02E48 and 24AA02E64) and 6-Lead SOT-23 (24AA025E48 and 24AA025E64)

Description

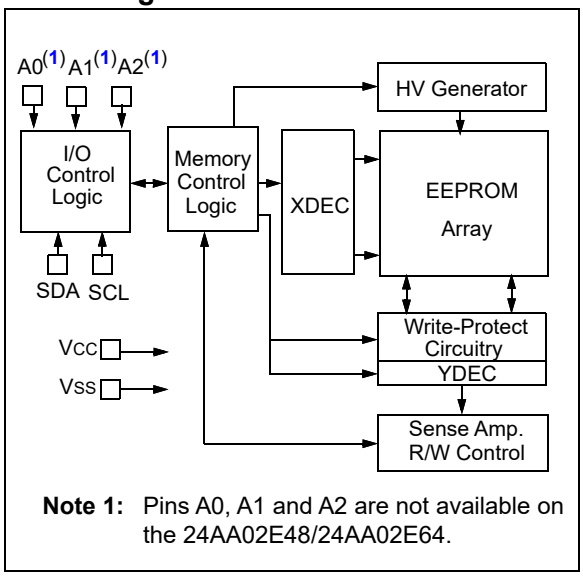
The Microchip Technology Inc. 24AA02XEXX(1) is a 2-Kbit Electrically Erasable PROM (EEPROM). The device is organized as two blocks of 128 x 8-bit memory with a two-wire serial interface. Low-voltage design permits operation down to 1.7V, with maximum standby currents of only 1 µA for I-temp. and 5 µA for E-temp., as well as a maximum active current of 1 mA. The 24AA02XEXX also has a page write capability for up to eight bytes of data (16 bytes on the 24AA025E48/24AA025E64).

Note 1: 24AA02XEXX is used in this document as a generic part number for the 24AA02E48/ 24AA02E64/24AA025E48/24AA025E64 devices.

Package Types



Block Diagram



Note 1: Pins A0, A1 and A2 are not available on the 24AA02E48/24AA02E64.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C, VCC = +1.7V to +5.5V Extended (E): TA = -40°C to +125°C, VCC = +1.7V to +5.5V			
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	0.7 VCC	—	V	
D2	VIL	Low-Level Input Voltage	—	0.3 VCC	V	
D3	VHYS	Hysteresis of Schmitt Trigger Inputs	0.05 VCC	—	V	Note 1
D4	VOL	Low-Level Output Voltage	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D5	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin Capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V (Note 1) TA = +25°C, FCLK = 1 MHz
D8	ICCWRITE	Operating Current	—	3	mA	VCC = 5.5V, SCL = 400 kHz
D9	ICCREAD		—	1	mA	
D10	ICCS	Standby Current	—	1	µA	Industrial (I) SDA = SCL = VCC
			—	5	µA	Extended (E) SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V Extended (E): T_A = -40°C to +125°C, V_{CC} = +1.7V to +5.5V			
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock Frequency	—	400	kHz	2.5V ≤ V_{CC} ≤ 5.5V
			—	100	kHz	1.7V ≤ V_{CC} < 2.5V
2	T_{HIGH}	Clock High Time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
			4000	—	ns	1.7V ≤ V_{CC} < 2.5V
3	T_{LOW}	Clock Low Time	1300	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
			4700	—	ns	1.7V ≤ V_{CC} < 2.5V
4	T_R	SDA and SCL Rise Time	—	300	ns	2.5V ≤ V_{CC} ≤ 5.5V (**Note 1**)
			—	1000	ns	1.7V ≤ V_{CC} < 2.5V (**Note 1**)
5	T_F	SDA and SCL Fall Time	—	300	ns	**Note 1**
6	$T_{HD:STA}$	Start Condition Hold Time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
			4000	—	ns	1.7V ≤ V_{CC} < 2.5V
7	$T_{SU:STA}$	Start Condition Setup Time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
			4700	—	ns	1.7V ≤ V_{CC} < 2.5V
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	ns	**Note 2**
9	$T_{SU:DAT}$	Data Input Setup Time	100	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
			250	—	ns	1.7V ≤ V_{CC} < 2.5V
10	$T_{SU:STO}$	Stop Condition Setup Time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
			4000	—	ns	1.7V ≤ V_{CC} < 2.5V
11	T_{AA}	Output Valid from Clock	—	900	ns	2.5V ≤ V_{CC} ≤ 5.5V (**Note 2**)
			—	3500	ns	1.7V ≤ V_{CC} < 2.5V (**Note 2**)
12	T_{BUF}	Bus Free Time: Bus time must be free before a new transmission can start	1300	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
			4700	—	ns	1.7V ≤ V_{CC} < 2.5V
13	T_{OF}	Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	—	250	ns	2.5V ≤ V_{CC} ≤ 5.5V
			—	250	ns	1.7V ≤ V_{CC} < 2.5V
14	T_{SP}	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	**Notes 1** and **3**
15	T_{WC}	Write Cycle Time (byte or page)	—	5	ms	
16		Endurance	1,000,000	—	cycles	+25°C, 5.5V, Page Mode (**Note 4**)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization.

FIGURE 1-1: BUS TIMING DATA

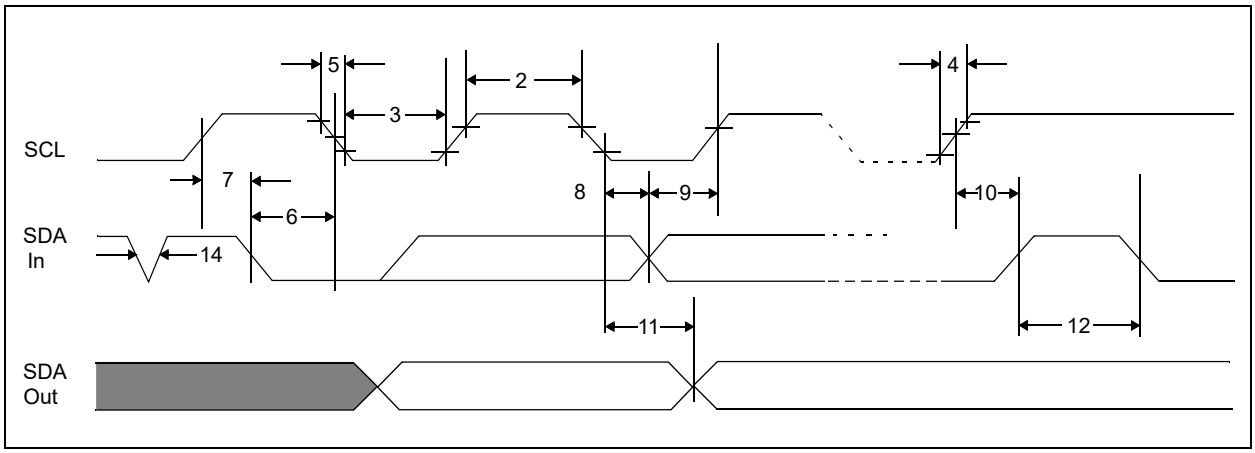
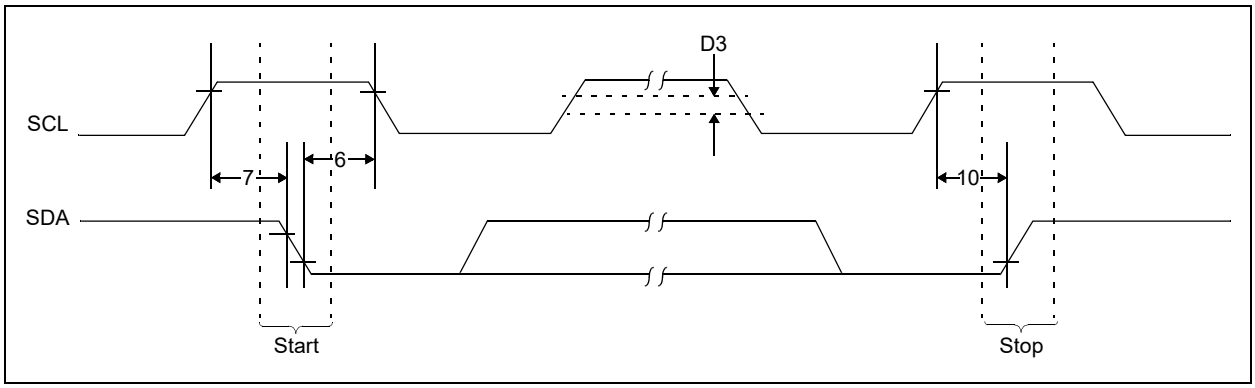


FIGURE 1-2: BUS TIMING START/STOP



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	SOIC	5-Pin SOT-23	6-Pin SOT-23	Description
A0	1	—	5	Chip Address Input(1)
A1	2	—	4	Chip Address Input(1)
A2	3	—	—	Chip Address Input(1)
VSS	4	2	2	Ground
SDA	5	3	3	Serial Address/Data I/O
SCL	6	1	1	Serial Clock
NC	7	5	—	Not Connected
VCC	8	4	6	+1.7V to 5.5V Power Supply

Note 1: Chip address inputs A0, A1 and A2 are not connected on the 24AA02E48/24AA02E64.

2.1 Chip Address Inputs (A0, A1, A2)

The A0, A1 and A2 pins are not used by the 24AA02E48/24AA02E64. They may be left floating or tied to either VSS or VCC.

For the 24AA025E48/24AA025E64, the levels on the A0, A1 and A2 inputs are compared with the corresponding bits in the client address. The chip is selected if the compare is true. For the 6-lead SOT-23 package, pin A2 is not connected and its corresponding bit in the client address should always be set to '0'.

Up to eight 24AA025E48/24AA025E64 devices (four for the SOT-23 package) may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VSS or VCC.

2.2 Serial Address/Data Input/Output (SDA)

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

2.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

3.0 FUNCTIONAL DESCRIPTION

The 24AA02XEXX supports a bidirectional, two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24AA02XEXX works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the host device and is, theoretically, unlimited (although only the last sixteen will be stored when doing a write operation). When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) principle.

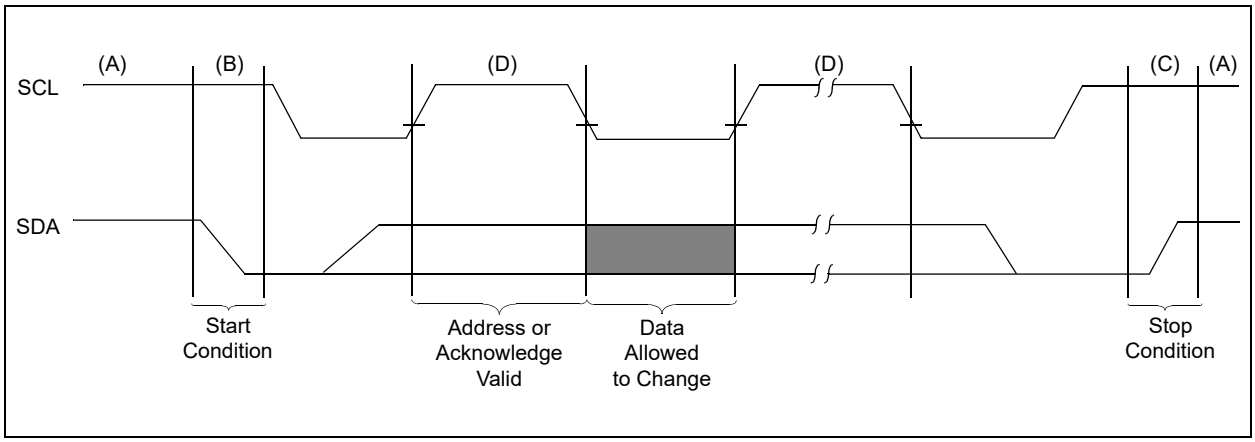
4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24AA02XEXX does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24AA02XEXX) will leave the data line high to enable the host to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The control byte consists of a four-bit control code. For the 24AA02XEXX, this is set as '1010' binary for read and write operations. For the 24AA02E48/24AA02E64, the next three bits of the control byte are "don't cares."

For the 24AA025E48/24AA025E64, the next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24AA025E48/24AA025E64 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

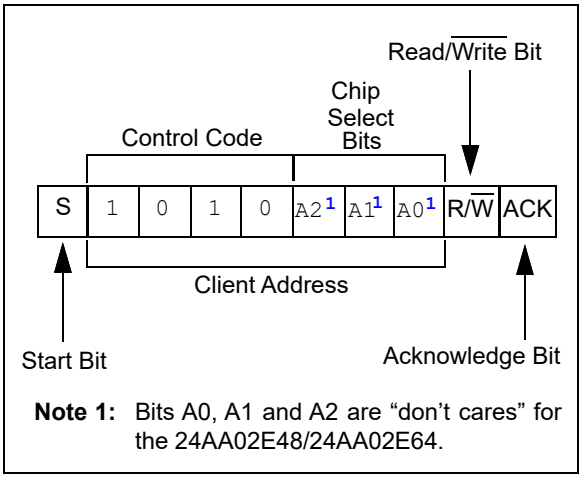
For the 6-pin SOT-23 package, the A2 address pin is not available. During device addressing, the A2 Chip Select bit should be set to '0'.

The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. The next byte received defines the address of the first data byte (Figure 5-2).

Following the Start condition, the 24AA02XEXX monitors the SDA bus, checking the device type identifier being transmitted and, upon a '1010' code, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA02XEXX will select a read or write operation.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	Chip Address	1
Write	1010	Chip Address	0

FIGURE 5-1: CONTROL BYTE ALLOCATION



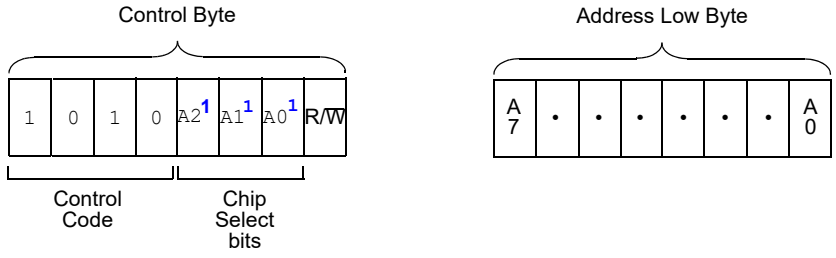
Note 1: Bits A0, A1 and A2 are "don't cares" for the 24AA02E48/24AA02E64.

5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24AA025E48/24AA025E64 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8; A1 as address bit A9; and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

For the SOT-23 package, up to four 24AA025E48/24AA025E64 devices can be added for up to 8K bits of address space. In this case, software can use A0 of the control byte as address bit A8 and A1 as address bit A9. It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



Note 1: Bits A0, A1 and A2 are "don't cares" for the 24AA02E48/24AA02E64.

6.0 WRITE OPERATION

6.1 Byte Write

Following the Start condition from the host, the device code (four bits), the chip address (three bits) and the R/$\overline{W}$ bit which is a logic-low, is placed onto the bus by the host transmitter. This indicates to the addressed client receiver that a byte with a word address will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the word address and will be written into the Address Pointer of the 24AA02XEXX. After receiving another Acknowledge signal from the 24AA02XEXX, the host device will transmit the data word to be written into the addressed memory location. The 24AA02XEXX acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24AA02XEXX will not generate Acknowledge signals (Figure 6-1).

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA02XEXX in the same way as in a byte write. However, instead of generating a Stop condition, the host transmits up to eight data bytes to the 24AA02XEXX, which are temporarily stored in the on-chip page buffer and will be written into memory once the host has transmitted a Stop condition. Upon receipt of each word, the three lower-order Address Pointer bits (four for the 24AA025E48/24AA025E64) are internally incremented by one.

The higher-order five bits (four for the 24AA025E48/24AA025E64) of the word address remain constant. If the host should transmit more than eight words (16 for the 24AA025E48/24AA025E64) prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 6-2).

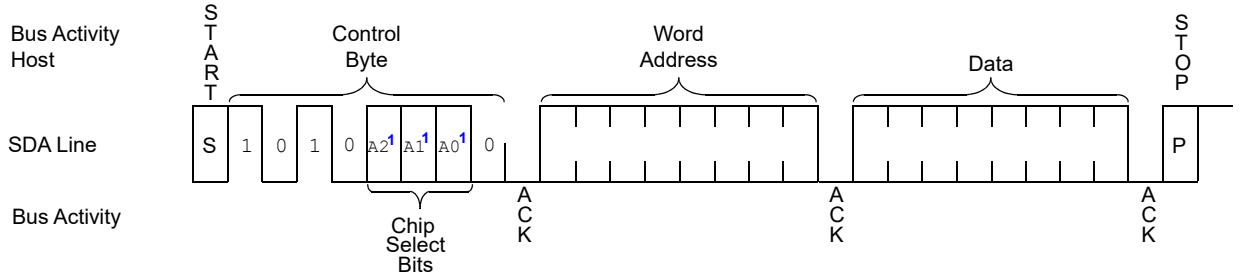
Note:	Page write operations are limited to writing bytes within a single physical page **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The upper half of the array (80h-FFh) is permanently write-protected. Write operations to this address range are inhibited. Read operations are not affected.

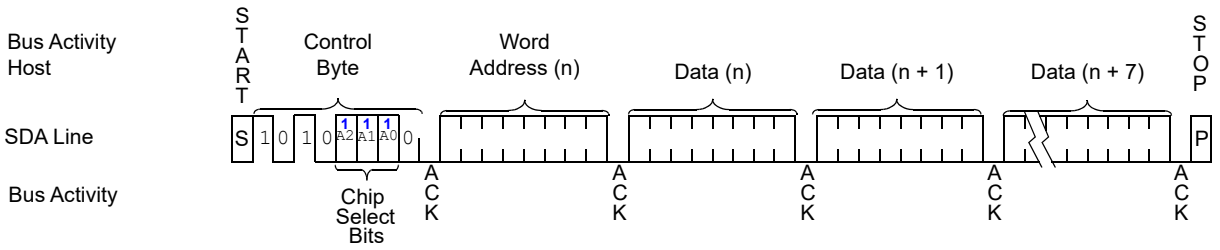
The remaining half of the array (00h-7Fh) can be written to and read from normally.

FIGURE 6-1: BYTE WRITE



Note 1: Bits A0, A1 and A2 are "don't cares" for the 24AA02E48/24AA02E64.

FIGURE 6-2: PAGE WRITE

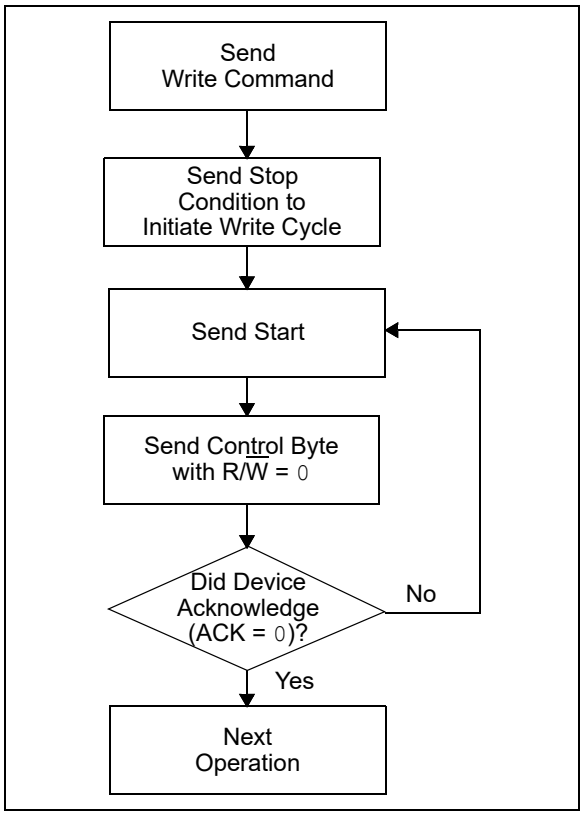


Note 1: Bits A0, A1 and A2 are “don’t cares” for the 24AA02E48/24AA02E64.

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the host, the device initiates the internally-timed write cycle and ACK polling can then be initiated immediately. This involves the host sending a Start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the host can then proceed with the next read or write command. See Figure 7-1 for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the client address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24AA02XEXX contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address 'n', the next current address read operation would access data from address n + 1. Upon receipt of the client address with R/$\overline{W}$ bit set to '1', the 24AA02XEXX issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but generate a Stop condition and the 24AA02XEXX discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24AA02XEXX as part of a write operation. Once the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24AA02XEXX will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer, but generate a Stop condition and the 24AA02XEXX will discontinue transmission (Figure 8-2).

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24AA02XEXX transmits the first data byte, the host issues an Acknowledge as opposed to a Stop condition in a random read. This directs the 24AA02XEXX to transmit the next sequentially addressed 8-bit word (Figure 8-3).

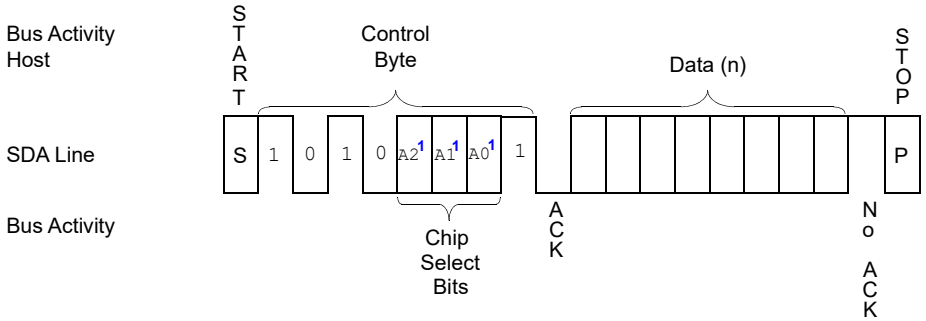
To provide sequential reads, the 24AA02XEXX contains an internal Address Pointer that is incremented by one upon completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24AA02XEXX employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5V at nominal conditions.

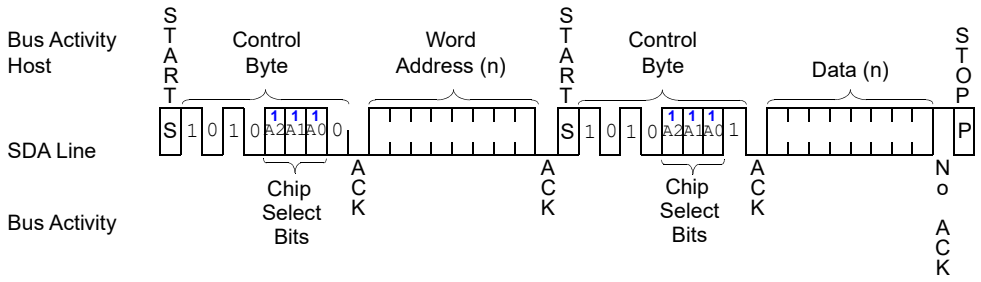
The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

FIGURE 8-1: CURRENT ADDRESS READ



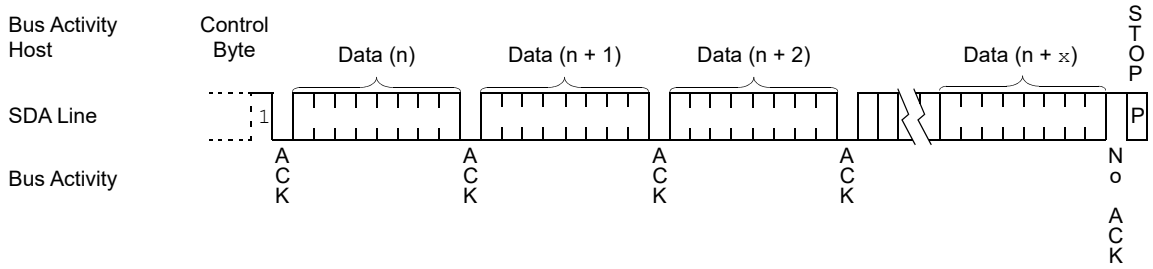
Note 1: Bits A0, A1 and A2 are "don't cares" for the 24AA02E48/24AA02E64.

FIGURE 8-2: RANDOM READ



Note 1: Bits A0, A1 and A2 are “don’t cares” for the 24AA02E48/24AA02E64.

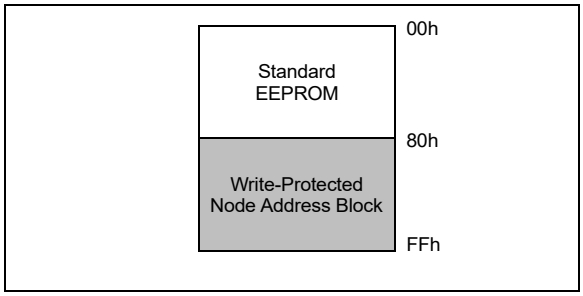
FIGURE 8-3: SEQUENTIAL READ



9.0 PRE-PROGRAMMED EUI-48 OR EUI-64 NODE ADDRESS

The 24AA02XEXX is programmed at the factory with a globally unique node address stored in the upper half of the array and permanently write-protected. The remaining 1,024 bits are available for application use.

FIGURE 9-1: MEMORY ORGANIZATION



9.1 EUI-48 Node Address (24AAXXXE48)

The 6-byte EUI-48 node address value of the 24AAXXXE48 is stored in array locations 0xFA through 0xFF, as shown in Figure 9-2. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining three bytes are the Extension Identifier and are generated by Microchip to ensure a globally unique, 48-bit value.

9.1.1 ORGANIZATIONALLY UNIQUE IDENTIFIERS (OUIs)

Each OUI provides roughly 16M (2^{24}) addresses. Once the address pool for an OUI is exhausted, Microchip will acquire a new OUI from IEEE to use for programming this model. For more information on past and current OUIs see *"Organizationally Unique Identifiers For Preprogrammed EUI-48 and EUI-64 Address Devices"* Technical Brief (DS90003187).

Note:	The OUI will change as addresses are exhausted. Customers are not guaranteed to receive a specific OUI and should design their application to accept new OUIs as they are introduced.

9.1.2 EUI-64 SUPPORT USING THE 24AAXXXE48

The pre-programmed EUI-48 node address of the 24AAXXXE48 can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by the application software inserting 0xFFFE between the OUI and the Extension Identifier, as shown below.

Note:	As an alternative, the 24AAXXXE64 features an EUI-64 node address that can be used in EUI-64 applications directly without the need for encapsulation, thereby simplifying system software. See **Section 9.2 "EUI-64 Node Address (24AAXXXE64)"** for details.

FIGURE 9-2: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (24AAXXXE48)

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
Array Address	FAh					FFh

Corresponding EUI-48 Node Address: 00-04-A3-12-34-56

Corresponding EUI-64 Node Address After Encapsulation (1): 00-04-A3-FF-FE-12-34-56

Note 1: Encapsulation is performed by the application software.

9.2 EUI-64 Node Address (24AAXXXE64)

The 8-byte EUI-64 node address value of the 24AAXXXE64 is stored in array locations 0xF8 through 0xFF, as shown in Figure 9-3. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining five bytes are the Extension Identifier and are generated by Microchip to ensure a globally unique, 64-bit value.

Note:	In conformance with IEEE guidelines, Microchip will not use the values 0xFFFE and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values are specifically reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

FIGURE 9-3: EUI-64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (24AAXXXE64)

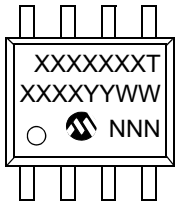
Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	90h
Array Address	F8h							FFh

Corresponding EUI-64 Node Address: 00-04-A3-12-34-56-78-90

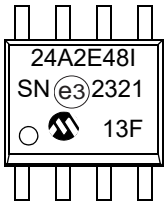
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

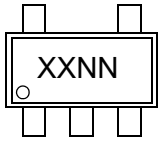
8-Lead SOIC (3.90 mm)



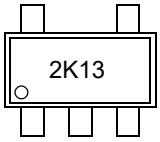
Example



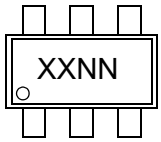
5-Lead SOT-23 (**1-Line Marking**)



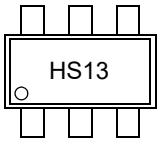
Example



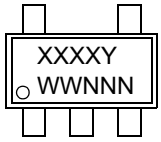
6-Lead SOT-23 (**1-Line Marking**)



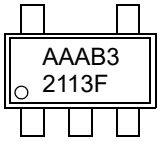
Example



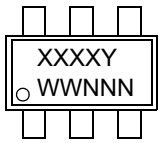
5-Lead SOT-23 (**2-Line Marking**)



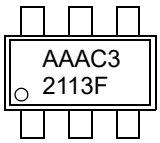
Example



6-Lead SOT-23 (**2-Line Marking**)



Example



Part Number	1st Line Marking Code			
	SOIC		SOT-23	
	I-Temp.	E-Temp.	I-Temp.	E-Temp.
24AA02E48	24A2E48I	24A2E48E	2KNN(1)	AABLY(2)
24AA025E48	4A25E48I	4A25E48E	HSNN(1)	AABMY(2)
24AA02E64	24A2E64I	24A2E64E	AAABY(2)	AABNY(2)
24AA025E64	4A25E64I	4A25E64E	AAACY(2)	AABPY(2)

Note 1: These parts use the 1-line SOT-23 marking format

2: These parts use the 2-line SOT-23 marking format

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS-compliant JEDEC® designator for Matte Tin (Sn)

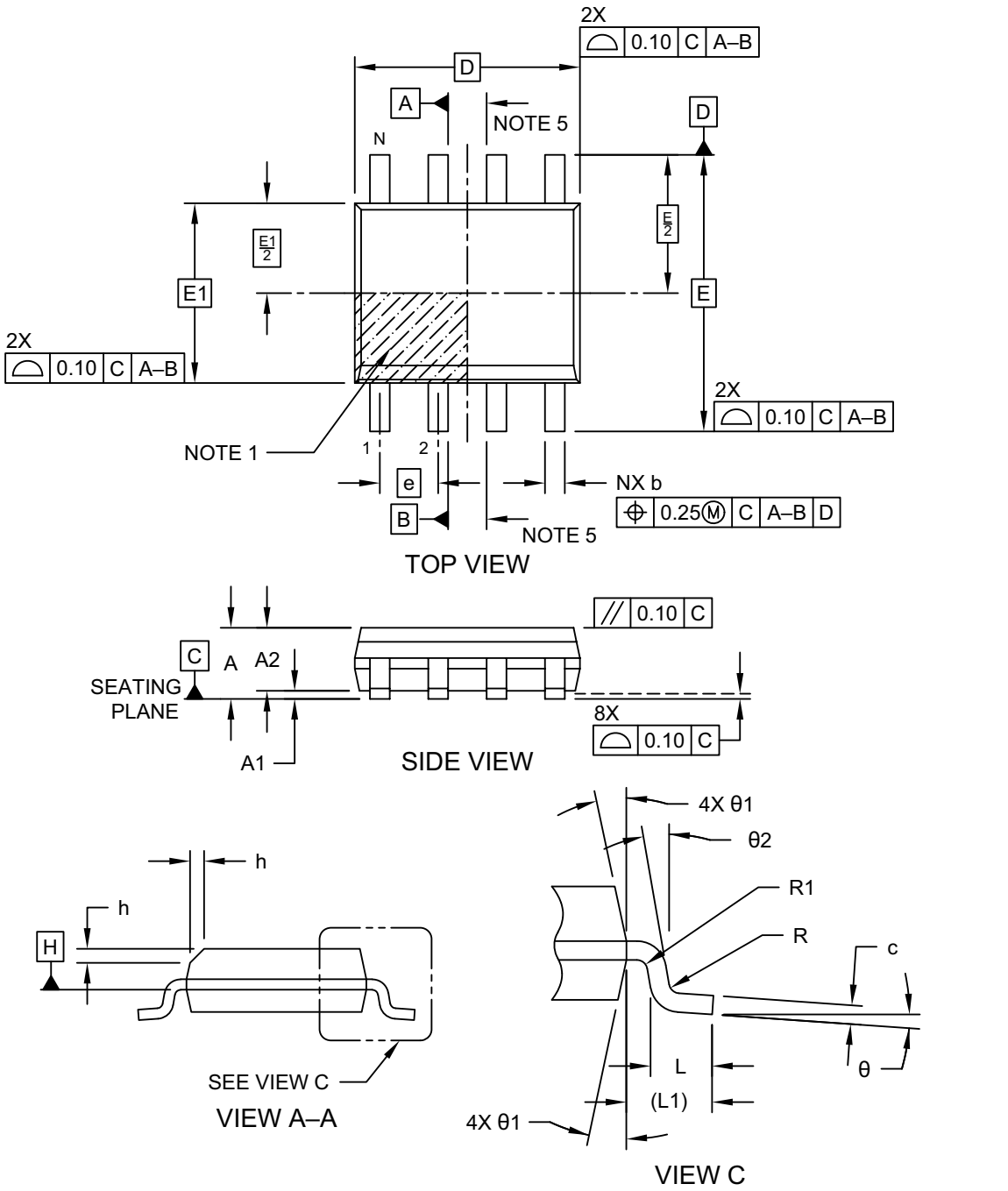
Note: Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

Note: For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

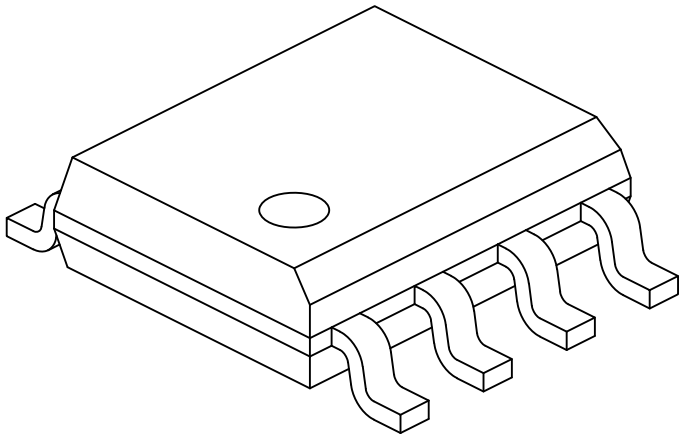
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

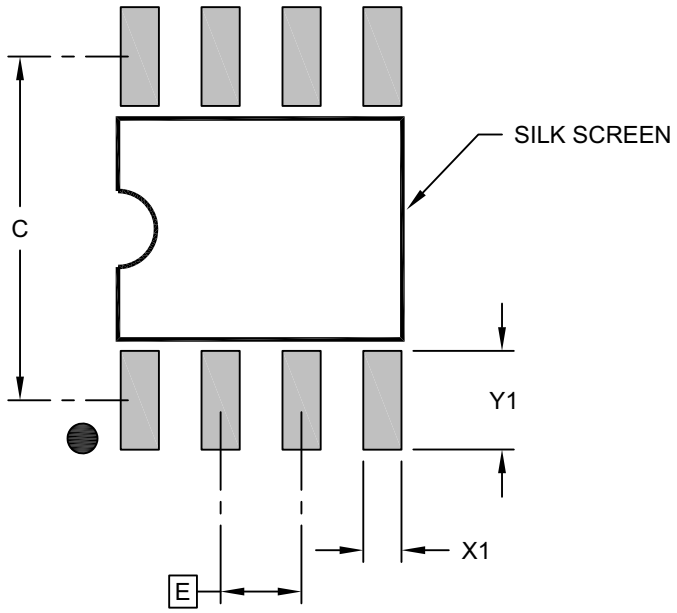
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

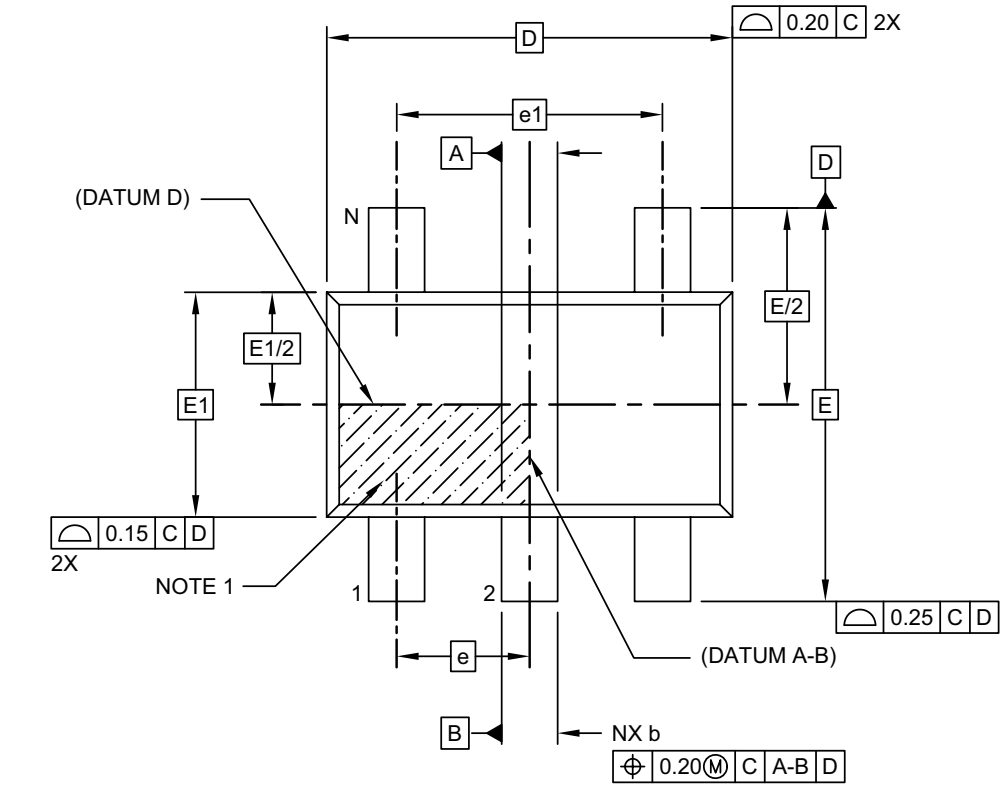
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

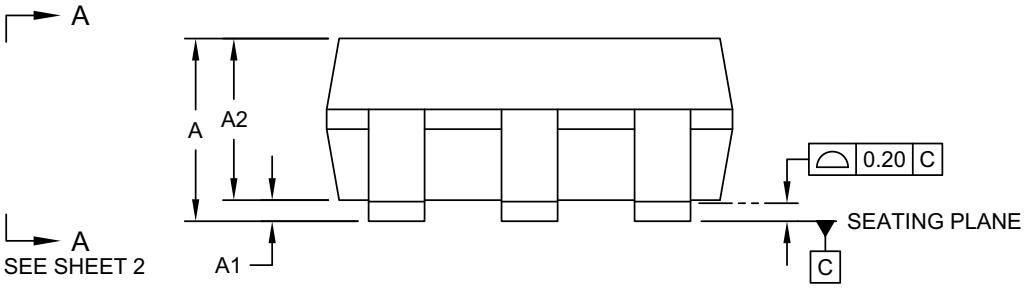
Microchip Technology Drawing C04-2057-SN Rev K

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

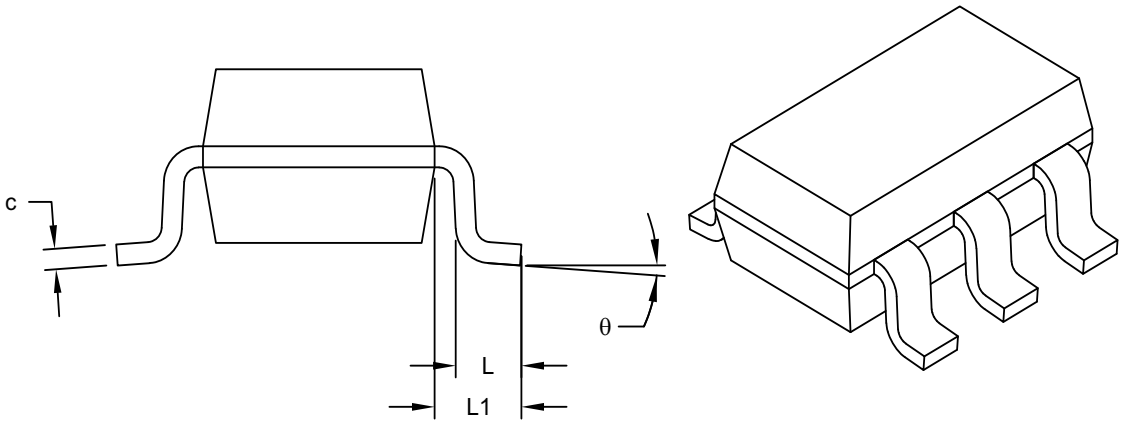


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

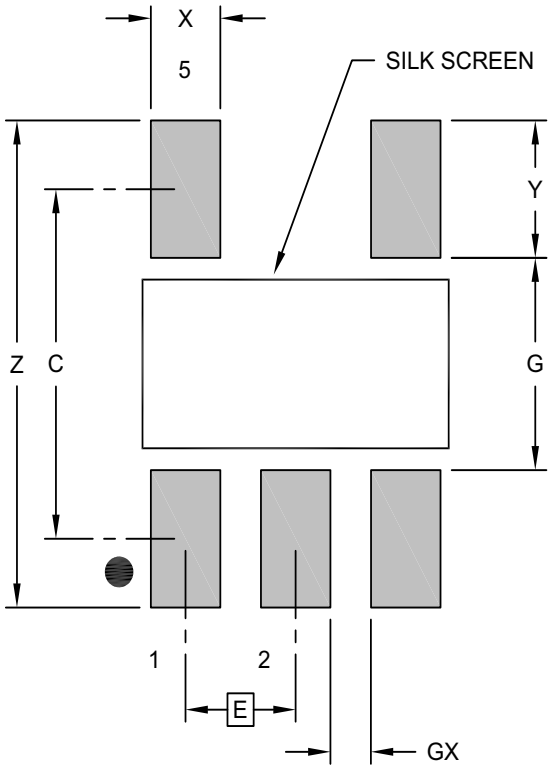
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

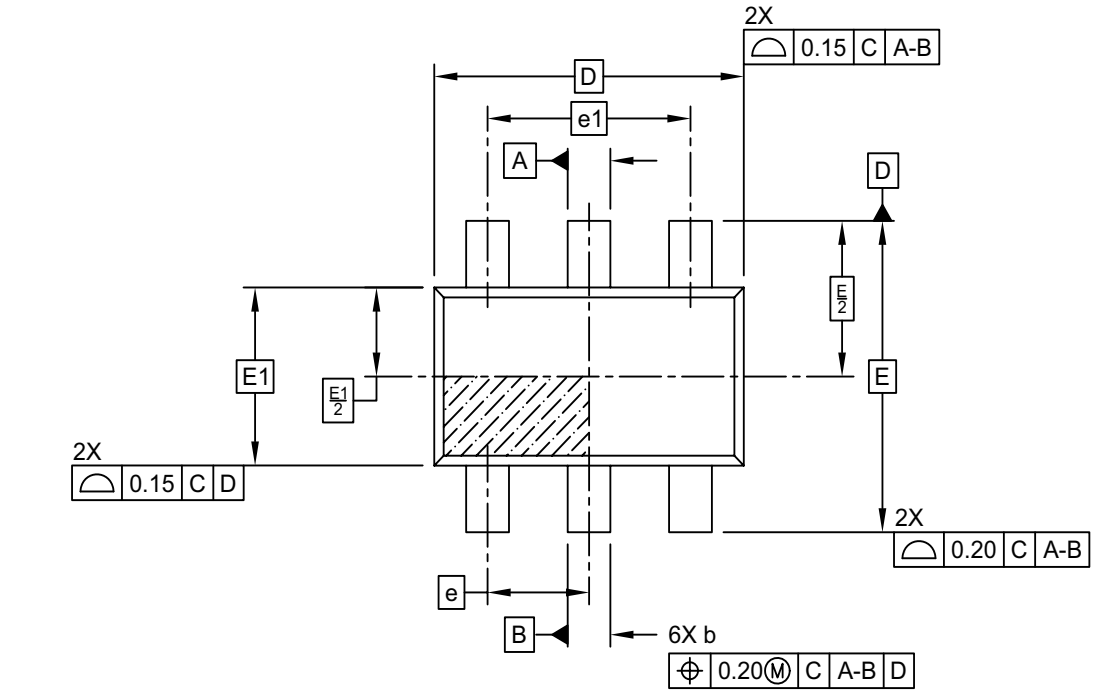
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

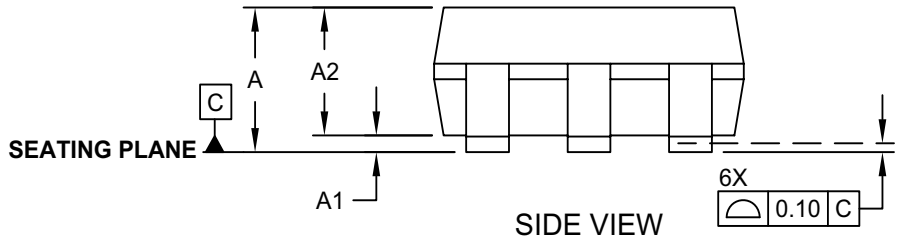
Microchip Technology Drawing No. C04-2091-OT Rev H

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

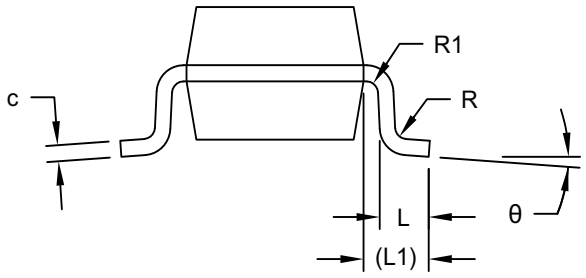
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

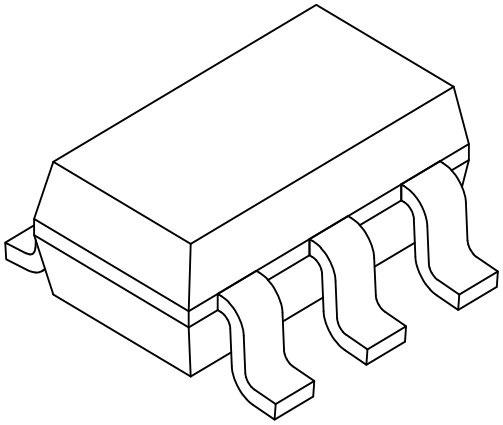


END VIEW

Microchip Technology Drawing C04-028-OT Rev E Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

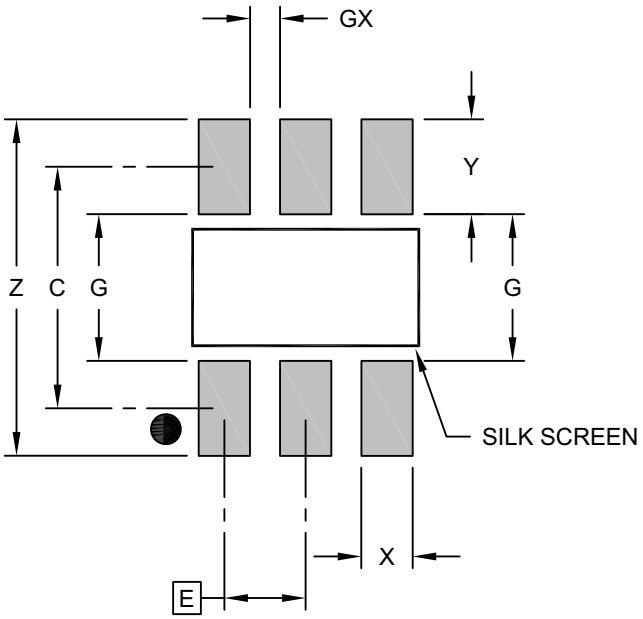
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028-OT Rev E Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028-OT Rev E

APPENDIX A: REVISION HISTORY

Revision K (08/23)

Added automotive product offering; Updated SOT-23 package drawings.

Revision J (09/2022)

Updated SOIC and SOT-23 package drawings; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively; Replaced “Automotive (E):” designation with “Extended (E):” designation; Reformatted some sections for better readability.

Revision H (02/18)

Added detailed description of OUIs.

Revision G (08/16)

Added new OUI (54-10-EC) to list.

Revision F (10/14)

Added E-temp. option to part numbers.

Revision E (04/13)

Added 24AA02E64 and 24AA025E64 part numbers.

Revision D (05/10)

Added 24AA025E48 part number and 6-lead SOT-23 package.

Revision C (03/10)

Added new sections 2.0 through 9.0.

Revision B (01/09)

Removed preliminary status.

Revision A (12/08)

Initial release of this document.

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- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, the latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups and a Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, the latest Microchip press releases, a listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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Users of Microchip products can receive assistance through several channels:

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- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: https://www.microchip.com/support

PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	24AA02E48	= 1.7V, 2-Kbit I^2C Serial EEPROM with EUI-48™ Node Identity
	24AA025E48	= 1.7V, 2-Kbit I^2C Serial EEPROM with EUI-48™ Node Identity and Address Pins
	24AA02E64	= 1.7V, 2-Kbit I^2C Serial EEPROM with EUI-64™ Node Identity
	24AA025E64	= 1.7V, 2-Kbit I^2C Serial EEPROM with EUI-64™ Node Identity and Address Pins
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel(1)
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package:	SN	= Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC)
	OT	= Plastic Small Outline Transistor (SOT-23) (Tape and Reel only)

Examples:

a) 24AA02E48-I/SN: 2-Kbit, 8-byte page, Serial EEPROM with EUI-48 Node Identity, 1.7V, Industrial Temperature, SOIC package.

b) 24AA02E48T-I/OT: 2-Kbit, 8-byte page, Serial EEPROM with EUI-48 Node Identity, 1.7V, Tape and Reel, Industrial Temperature, 5-lead, SOT-23 package.

c) 24AA025E48-I/SN: 2-Kbit, 16-byte page, Serial EEPROM with EUI-48 Node Identity, 1.7V, Cascadable, Industrial Temperature, SOIC package.

d) 24AA02E64-I/SN: 2-Kbit, 8-byte page, Serial EEPROM with EUI-64 Node Identity, 1.7V, Industrial Temperature, SOIC package.

e) 24AA02E64T-I/OT: 2-Kbit, 8-byte page, Serial EEPROM with EUI-64 Node Identity, 1.7V, Tape and Reel, Industrial Temperature, 5-lead, SOT-23 package.

f) 24AA025E64-I/SN: 2-Kbit, 16-byte page, Serial EEPROM with EUI-64 Node Identity, 1.7V, Cascadable, Industrial Temperature, SOIC package.

g) 24AA025E48T-E/SN: 2-Kbit, 16-byte page, Serial EEPROM with EUI-48 Node Identity, 1.7V, Cascadable, Tape and Reel, Extended Temperature, SOIC package.

h) 24AA02E48-E/SN: 2-Kbit, 8-byte page, Serial EEPROM with EUI-48 Node Identity, 1.7V, Extended Temperature, SOIC package.

i) 24AA025E48T-E/OT: 2-Kbit, 16-byte page, Serial EEPROM with EUI-48 Node Identity, 1.7V, Cascadable, Tape and Reel, Extended Temperature, 6-lead, SOT-23 package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX	XXX(2,3)
Device	Tape and Reel Option	Temperature Range	Package	Variant

Device:	24AA02E48	=	1.7V, 2-Kbit I^2C Serial EEPROM with EUI-48™ Node Identity
Tape and Reel Option:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel(1)
Temperature Range:	I	=	-40°C to +85°C (AEC-Q100 Grade 3)
	E	=	-40°C to +125°C (AEC-Q100 Grade 1)
Package:	SN	=	Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC)
	OT	=	Plastic Small Outline Transistor (SOT-23) (Tape and Reel only)
Variant:	16KVAO	=	Standard Automotive, 16K Process (2)
	16KVXX	=	Customer-Specific Automotive, 16K Process(3)

Examples:

a) 24AA02E48T-E/SN16KVAO: 2-Kbit, 8-byte page, Serial EEPROM with EUI-48 Node Identity, 1.7V Automotive Grade 1, SOIC package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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