9-CHANNEL LIGHT EFFECT LED DRIVER

October 2018

GENERAL DESCRIPTION

IS31FL3199 is a 9-channel light effect LED driver which features two-dimensional auto breathing mode and an audio modulated display mode. It has One Shot Programming mode and PWM Control mode for RGB lighting effects. The maximum output current can be adjusted in 8 levels (5mA~40mA).

In PWM Control mode, the PWM duty cycle of each output can be independently programmed and controlled in 256 steps to simplify color mixing. In One Shot Programming mode, the timing characteristics for output current - current rising, holding, falling and off time, can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single color breathing without requiring any additional interface activity, thus saving valuable system resources.

The IS31FL3199 includes an audio modulated display mode, wherein the brightness of LED can be modulated by audio signal. There is a cascade pin for the synchronization of two chips.

IS31FL3199 is available in QFN-20 (3mm × 3mm). It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- 2.7V to 5.5V supply voltage
- I2C interface, automatic address increment function
- Three groups RGB, single color LED breathing system-free pre-established pattern
- 9 independently controlled automatic and semiautomatic breathing system-free pre-established pattern
- 9 independently controlled outputs of 256 PWM steps
- 8 levels programmable output current
- Audio mode with AGC function
- Cascade for the synchronization of chips
- Over-temperature protection
- QFN-20 (3mm × 3mm) package

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

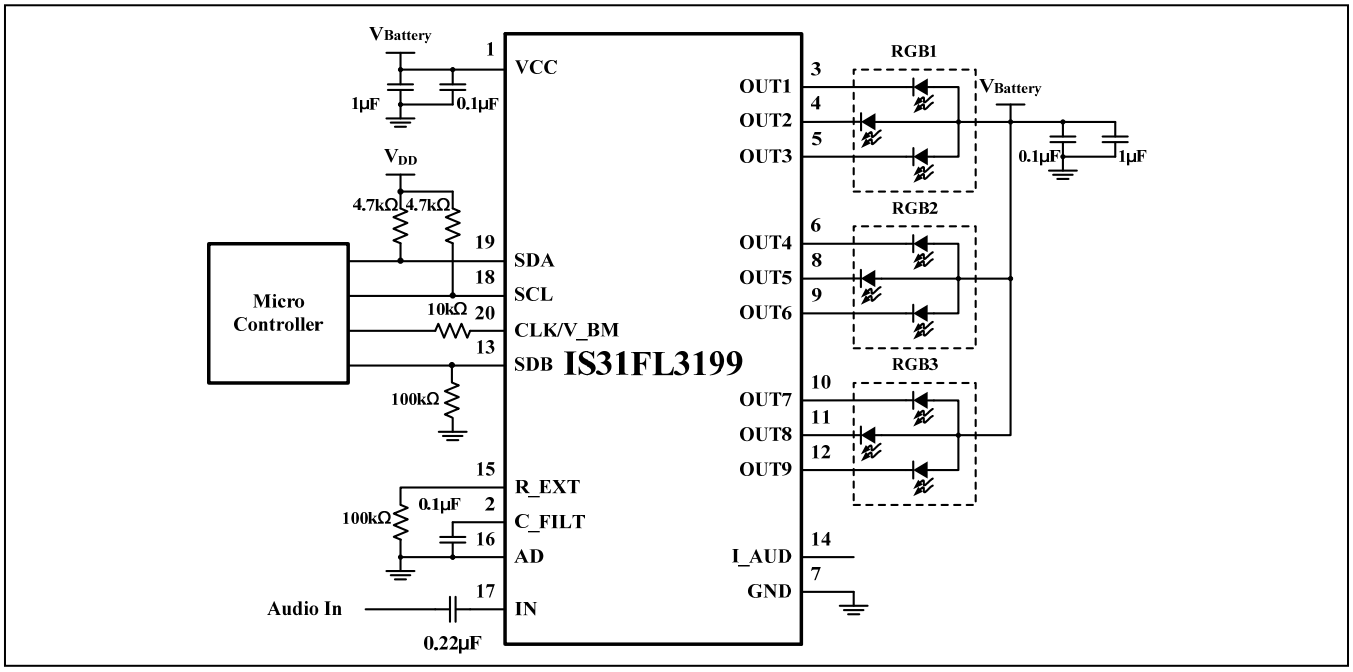


Figure 1 Typical Application Circuit

Note 1: IC should be placed far away from the antenna in order to prevent the EMI.

Note 2: The VIH of I2C bus (VDD as above) should be smaller than VCC. And if VIH is lower than 3.0V, it is recommended add a level shift circuit to avoid extra shutdown current.

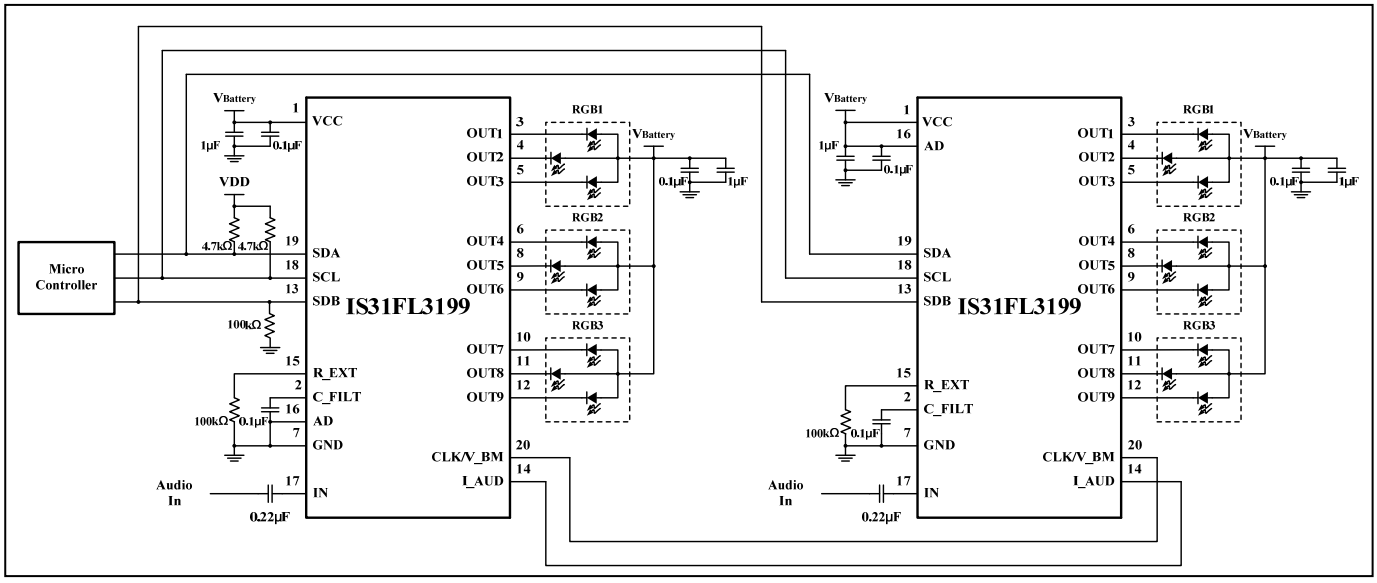
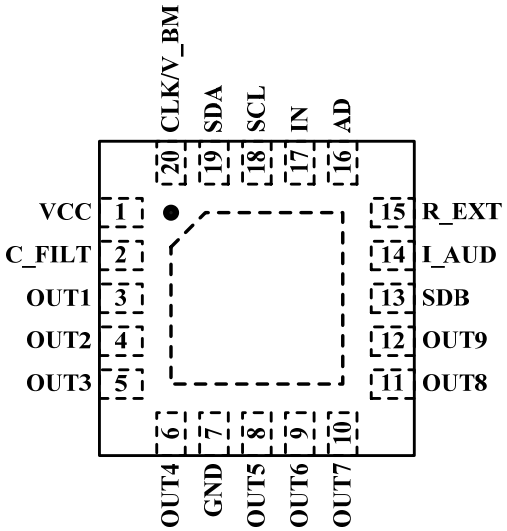


Figure 2 Typical Application Circuit (Cascade Mode)

Note 3: One system should contain only one clock master, all slave parts should be configured as slave mode before the master is configured as master mode. Work as master mode or slave mode specified by Configuration Register-2 (CM bit, register 04h). Master part output master clock, and all the other parts which work as slave input this master clock.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	

PIN DESCRIPTION

No.	Pin	Description
1	VCC	Power supply.
2	C_FILT	Filter capacitor for audio control.
3~6	OUT1~OUT4	Current source outputs.
7	GND	Ground.
8~12	OUT5~OUT9	Current source outputs.
13	SDB	Shutdown the chip when pulled to low.
14	I_AUD	Audio current input or output for cascade.
15	R_EXT	Input terminal used to connect an external resistor. The value must be about 100kΩ.
16	AD	I2C address setting.
17	IN	Audio input.
18	SCL	I2C serial clock.
19	SDA	I2C serial data.
20	CLK/V_BM	CLK input or output for cascade. When breathing mark function enable, this pin is V_BM pin.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3199-QFLS2-TR	QFN-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any OUTx pins	-0.3V ~ V_{CC}+0.3V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
GND terminal current	400mA
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, $T_A = T_J$	-40°C ~ +85°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	58.1°C/W
ESD (HBM) ESD (CDM)	±2kV ±1kV

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = -40°C ~ +85°C, unless otherwise noted. Typical value are T_A = 25°C, V_{CC} = 5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	$V_{SDB} = V_{CC}$		3		mA
I_{SD}	Shutdown current	V_{SDB} = 0V		1		μA
		$V_{SDB} = V_{CC}$, software shutdown		2		
I_{OUT}	Output current	PWM Control Mode, V_{DS} = 0.4V PWM Register(07h~0Fh) = 0xFF		20 (Note 5)		mA
		Audio Mode, Gain = 12dB $V_{IN} = 0.8V_{P-P,}$ 1kHz square wave		18 (Note 5)		
V_{HR}	Current sink headroom voltage	I_{OUT} = 20mA		400		mV
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V	1.4			V
I_{IL}	Logic "0" input current	SSD= "0", V_{INPUT}= 0V		5 (Note 6)		nA
I_{IH}	Logic "1" input current	SSD= "0", V_{INPUT}= V_{CC}		5 (Note 6)		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 6)

Symbol	Parameter	Condition	Standard Mode			Fast Mode			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-Clock frequency				100			400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		4.7			1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		4.0			0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		4.7			0.6			μs
$t_{SU, STO}$	STOP condition setup time		4.0			0.6			μs
$t_{HD, DAT}$	Data hold time (Note 7)		0		3.45	0		0.9	μs
$t_{SU, DAT}$	Data setup time (Note 8)		250			100			ns
t_{LOW}	SCL clock low period		4.7			1.3			μs
t_{HIGH}	SCL clock high period		4.0			0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving (Note 9)				1000		$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals, receiving (Note 9)				300		$20+0.1C_b$	300	ns

Note 5: The average current of each channel is I_{OUT}.

Note 6: Guaranteed by design.

Note 7: The minimum $t_{HD, DAT}$ measured start from V_{IL}(max) of SCL signal. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. V_{IL}(max)

Note 8: A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU,DAT} \geq 250ns$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU,DAT}$ = 1000 + 250 = 1250ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

Note 9: C_b= total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3199 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3199 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Since IS31FL3199 only supports write operations, A0 must always be "0". The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write Only):

Bit	A7:A3	A2:A1	A0
Value	11001	AD	0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3199.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3199's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3199 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3199, the register address byte is sent, most significant bit first. IS31FL3199 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3199 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3199, load the address of the data register that the first data byte is intended for. During the IS31FL3199 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3199 will be placed in the new address, and so on (Figure 6).

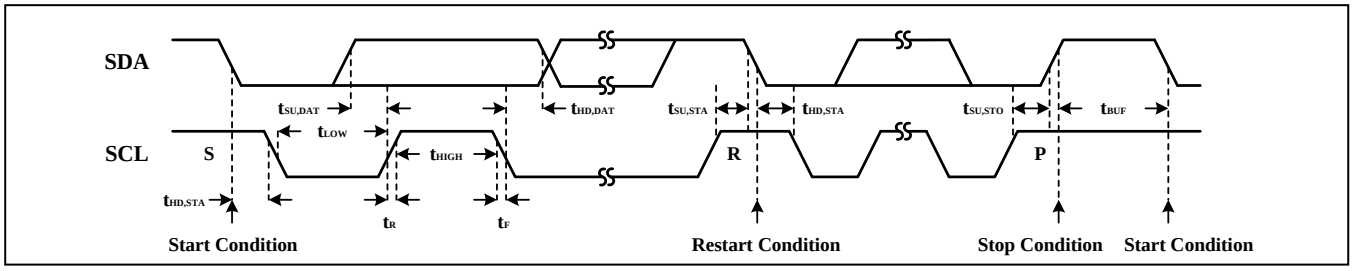


Figure 3 Interface Timing

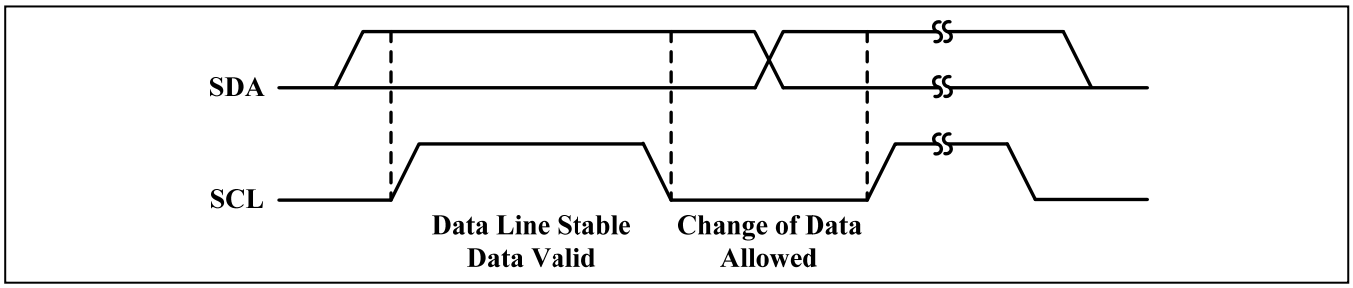


Figure 4 Bit Transfer

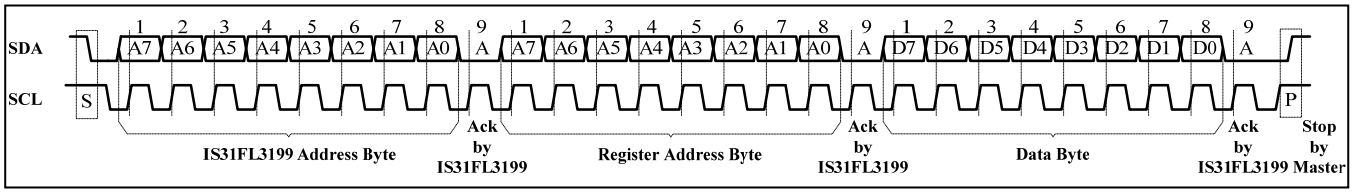


Figure 5 Writing to IS31FL3199(Typical)

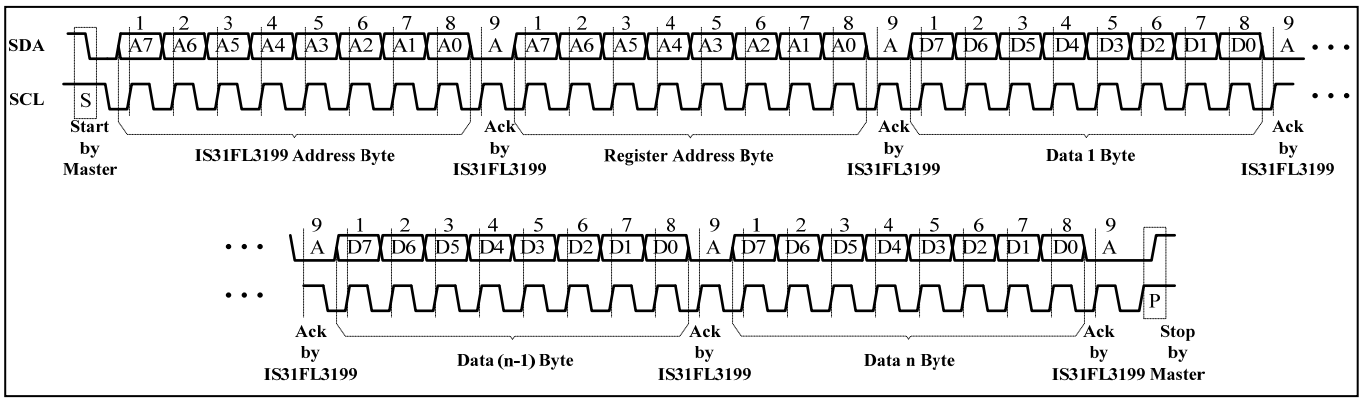


Figure 6 Writing to IS31FL3199(Automatic Address Increment)

REGISTERS DEFINITIONS

Table 2 Register Function

Address	Name	Function	Table	Default
00h	Shutdown Register	Set software shutdown mode	3	0000 0000
01h	LED Control Register 1	OUT1~ OUT6 enable bit	4	0111 0111
02h	LED Control Register 2	OUT7~ OUT9 enable bit	5	0000 0111
03h	Configuration Register 1	Set operation mode	6	0000 0000
04h	Configuration Register 2	Set output current and audio input gain	7	
05h	Ramping Mode Register	Set the ramping function mode	8	
06h	Breathing Mark Register	Set the breathing mark function	9	
07h ~ 0Fh	PWM Register	9 channels PWM duty cycle data registers	10	
10h	Data Update Register	Load PWM Registers and LED Control Registers' data	-	xxxx xxxx
11h ~ 19h	T0 Register	Set the T0 time	11	0000 0000
1Ah ~ 1Ch	T1~T3 Register	Set the T1~T3 time	12	
1Dh ~ 25h	T4 Register	Set the T4 time	13	
26h	Time Update Register	Load time registers' data	-	xxxx xxxx
FFh	Reset Register	Reset all registers to default value	-	

Table 3 00h Shutdown Register

Bit	D7:D1	D0
Name	-	SSD
Default	0000 000	0

The Shutdown Register sets software shutdown mode of IS31FL3199.

SSD Software Shutdown Enable
0 Software shutdown mode
1 Normal operation

Table 4 01h LED Control Register 1(OUT1~OUT6)

Bit	D7	D6:D4	D3	D2:D0
Name	-	OUT6:OUT4	-	OUT3:OUT1
Default	0	111	0	111

Table 5 02h LED Control Register 2(OUT7~OUT9)

Bit	D7:D3	D2:D0
Name	-	OUT9:OUT7
Default	0000 0	111

The LED Control Registers store the on or off state of each channel LED.

OUTx LED State
0 LED off
1 LED on

Table 6 03h Configuration Register 1

Bit	D7	D6:D4	D3	D2	D1	D0
Name	-	RGB3:1	-	AE	AGCE	AGCM
Default	0	000	0	0	0	0

The Configuration Register 1 sets operation mode.

RGBx RGB Mode Selection
0 PWM Control Mode
1 One Shot Programming Mode

AE Audio Modulate Enable
0 Disable
1 Enable

AGCE AGC Function Enable
0 Enable
1 Disable

AGCM AGC Mode Selection
0 Mode1 (Fast Modulation)
1 Mode2 (Slow Modulation)

Table 7 04h Configuration Register 2

Bit	D7	D6:D4	D3	D2:D0
Name	CM	CS	-	AGS
Default	0	000	0	000

The Configuration Register 2 stores the intensity control settings for all of the LEDs and the control mode.

CM Control Mode
0 Master
1 Slave

CS Current Setting
000 20mA
001 15mA
010 10mA
011 5mA
100 40mA
101 35mA
110 30mA
111 25mA

AGS Audio Gain Selection
000 Gain= 0dB
001 Gain= 3dB
010 Gain= 6dB
011 Gain= 9dB
100 Gain= 12dB
101 Gain= 15dB
110 Gain= 18dB
111 Gain= 21dB

Table 8 05h Ramping Mode Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	RM(RGB3:1)	-	HT(RGB3:1)
Default	0	000	0	000

The Ramping Mode Register sets the ramping function.

RM Ramping Mode Enable
0 Disable
1 Enable

HT Hold Time Selection
0 Breathing Hold on T2
1 Breathing Hold on T4

Table 9 06h Breathing Mark Register

Bit	D7:D5	D4	D3:D0
Name	-	BME	CSS
Default	000	0	0000

The Breathing Mark Register sets the breathing mark function (Detail information refers to Page 11).

BME	Breathing Mark Enable
0	Disable
1	Enable

CSS	Channel Selection
0000	OUT1
0001	OUT2
0010	OUT3
0011	OUT4
0100	OUT5
0101	OUT6
0110	OUT7
0111	OUT8
1000	OUT9
Others	Not available

Table 10 07h~0Fh PWM Register(OUT1~OUT9)

Bit	D7:D0
Name	PWM
Default	0000 0000

The PWM Registers can modulate RGB light with 256 different items.

The value of PWM Registers decide the average output current of OUT1~OUT9. The average output current may be computed using the Formula (1):

$$I_{OUT} = \frac{I_{MAX}}{256} \cdot \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (1)$$

Where “n” indicates the bit location in the respective PWM register.

For example: D7:D0 = 10110101,

$$I_{OUT} = I_{MAX} (2^0+2^2+2^4+2^5+2^7)/256$$

I_{MAX} is set by Configuration Register2 (04h).

10h Data Update Register

The data sent to the PWM Registers and the LED Control Registers will be stored in temporary registers. A write operation of “0000 0000” data to the Data Update Register is required to update the registers (01h~02h, 07h~0Fh).

Table 11 11h~19h T0 Register (OUT1~OUT9)

Bit	D7:D6	D5:D4	D3:D0
Name	-	B	A
Default	00	00	0000

The T0 Registers set the T0 time in One Shot Programming Mode.

$T0 = \tau \times A \times 2^B$

A = 0~15, B = 0~3 and τ = 260ms (Typ.)

For example, the max T0 is $260ms \times 15 \times 2^3 = 31.2s$

Table 12 1Ah~1Ch T1~T3 Register (RGB1~RGB3)

Bit	D7	D6:D4	D3	D2:D0
Name	DT	B	-	A
Default	0	000	0	000

The T1~T3 Registers set the T1~T3 time in One Shot Programming Mode.

DT	Double Time
0	T3 =T1
1	T3 = 2T1

If A = 0~4, $T1 = T3 = \tau \times 2^A$, τ = 260ms (Typ.)

If A = 5~6, the breathing function disable.

If A = 7, T1= T3 = 0.1ms

If B = 1~7, $T2 = \tau \times 2^{B-1}$, τ = 260ms (Typ.)

If B = 0, T2 = 0s.

For example, the max T1&T3 is $260ms \times 2^4 = 4.16s$

The max T2 is $260ms \times 2^6 = 16.64s$

Table 13 1Dh~25h T4 Register (OUT1~OUT9)

Bit	D7:D6	D5:D4	D3:D0
Name	-	B	A
Default	00	00	0000

The T4 Registers set the T4 time in One Shot Programming Mode.

$T4 = \tau \times A \times 2^B$

A = 0~15, B = 0~3 and τ = 260ms (Typ.)

For example, the max T4 is $260ms \times 15 \times 2^3 = 31.2s$

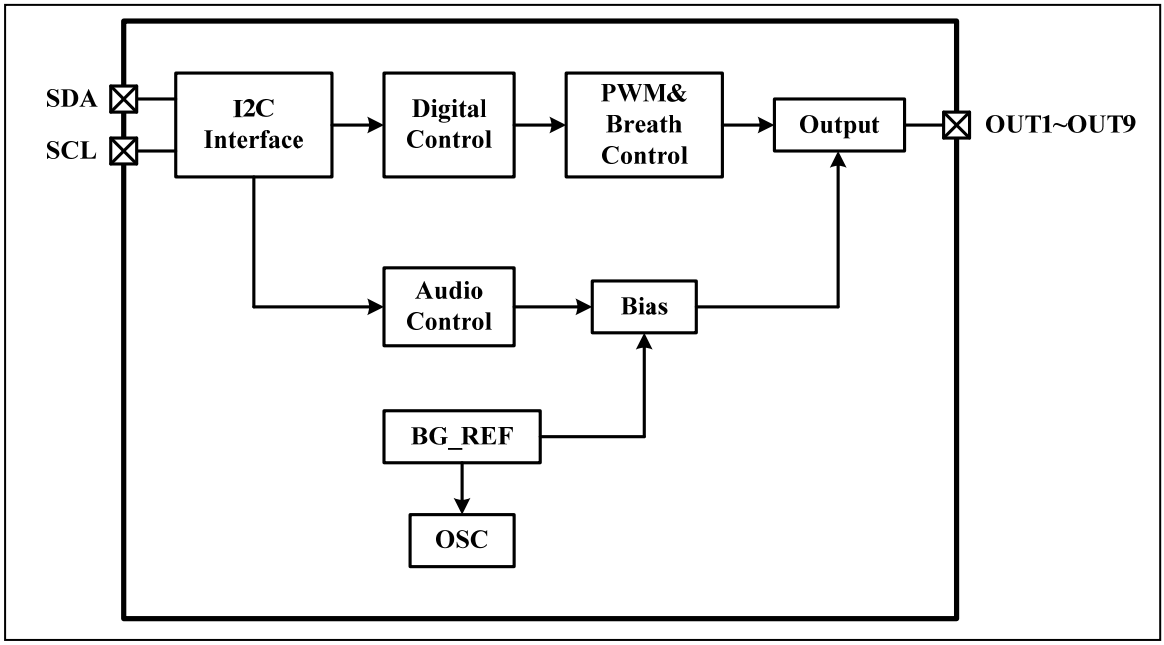
26h Time Update Register

The data sent to the time registers (11h~25h) will be stored in temporary registers. A write operation of “0000 0000” data to the Time Update Register is required to update the registers (11h~25h).

FFh Reset Register

Once user writes “0000 0000” data to the Reset Register, IS31FL3199 will reset all registers to default value. On initial power-up, the IS31FL3199 registers are reset to their default values for a blank display.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION

GENERAL DESCRIPTION

IS31FL3199 is a 9-channel LED driver with two-dimensional auto breathing and PWM Control mode. It can drive nine LEDs or three groups RGB.

POWER ON SEQUENCE

IS31FL3199 provides a power-on reset feature that is controlled by V_{BAT} (voltage at pin1) supply voltage. When the V_{BAT} exceeds 2.0V (POR_H, Typ.), the internal circuit starts to work. The reset signal will be generated to perform a power-on reset (POR_H) operation, which will reset all control circuits and configuration registers until the internal power voltage become stable.

Before SDB pull high, the I2C operation is allowed. The SDB rising edge will reset the I2C bus.

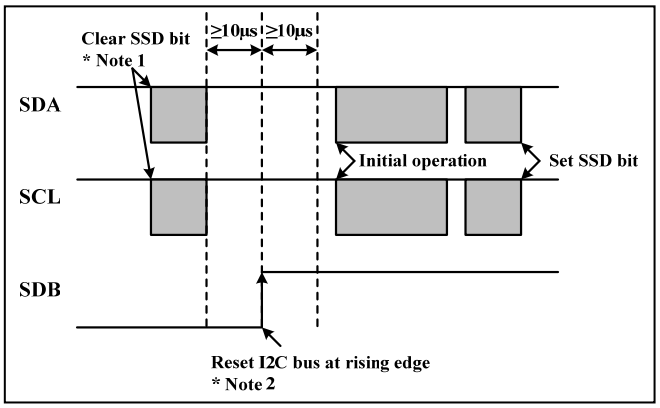


Figure 7 SDB Pin Sequence

Note 1: I2C operation is allowed when SDB is low.

Note 2: There should be no I2C operation 10μs before and after SDB rinsing edge.

In some case, like a mouse, when plug-out and quickly plug-in back the USB power, the LED will flash for a very short time. The reason is the power is not lower than the POR_L voltage point 1.92V (Typ.), and the device still stores the previous setting data, if user pull-up the SDB high when power up, following with the initial operation, the LED will be ON between SDB rising edge and PWM initial effective, to avoid this, as above figure, a writing to 00h is recommended to shutdown the chip before pull-high the SDB pin.

PWM CONTROL

By setting the RGBx bits of the Configuration Register1 (03h) to “0”, the IS31FL3199 will operate in PWM Control mode. The PWM Registers (07h~0Fh) can modulate LED brightness of 9 channels with 256 steps. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

RGB BREATHING CONTROL WITH AUTO COLOR CHANGING

By setting the RGBx bits of the Configuration Register1 (03h) to “1”, the IS31FL3199 will operate in One Shot Programming mode. In this mode each group RGB can be modulated breathing cycle independently by T0~T4. The full cycle is T1 to T4 (Figure 8). Setting different T0~T4 can achieve RGB breathing with auto color changing. The maximum intensity of each RGB can be adjusted independently by the PWM Registers (07h~0Fh).

Note, if IS31FL3199 operates in the One Shot Programming mode and then enters into the shutdown mode, an 8-bit data write operation to the Time Update Register is required to restart the LED breathing effect after the IC is re-enabled.

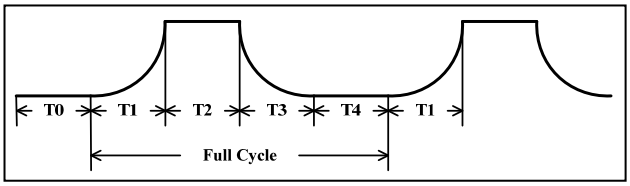


Figure 8 Breathing Timing

RGB AUTO BREATHING CONTROL WITH COLOR SETTING

IS31FL3199 can pre-establish pattern achieving mixing color breathing. There are three groups RGB. Each RGB consists of three channels. Every channel has an 8-bit PWM data register. The color can be set by the PWM data register. For example, there are three PWM data: 20h, 80h, C8h, so the three data will determine a kind of color.

After setting the color, T0~T4 time register will be set to control the LED breathing panel. And T0~T4 time should be same for one RGB or the pre-established color will change.

SEMIAUTOMATIC BREATHING

By setting the RGBx bits of the Configuration Register1 (03h) to “1” and the RM bit of the Ramping Mode Register (05h) to “1”, the ramping function is enabled. HT is the time select bit. When HT bit is set to “0”, T2 will be held forever, and the LED will remain at the programmed maximum intensity. When HT bit is set to “1”, T3 will continue and T4 will be held, causing the LED to complete one breathing cycle and then remain off.

AUDIO MODULATE DISPLAY MODE WITH AGC FUNCTION

In audio modulate display mode the output current can be modulated by the audio input signal. An AGC automatically adjusts the audio input gain to improve the dynamic range of the LED current modulation, thus improving the visual effect. When the input signal is

large such that the amplifier output begins to clip, the gain goes down. If the input signal is small, the gain increases, adjusting the output to provide a good dynamic response to the input signal.

The AGC can be disabled and the audio gain can be set by programming Configuration Register 1 (03h).

BREATHING MARK FUNCTION

By setting the BME bit of the Breathing Mark Register (06h) to "1", the breathing mark function is enabled. The CLK/V_BM pin is used as V_BM. If the BME bit sets to "0", the breathing mark function disabled. The CLK/V_BM pin is used as CLK. V_BM is an output pin. The breathing mark function is useful as a signal to notify the MCU when to update the color data. At the end of time period T1, V_BM will induce a falling edge and hold logic low, so the new data can be sent by MCU at this time. At the end of T3, V_BM will induce a rising edge and the MCU can send an update command to update all data simultaneously (Figure 9). The marking channel (OUT1~OUT9) is selected by the CSS bits of the Breathing Mark Register (06h).

When IS31FL3199 operates as slave, the breathing mark function is unavailable.

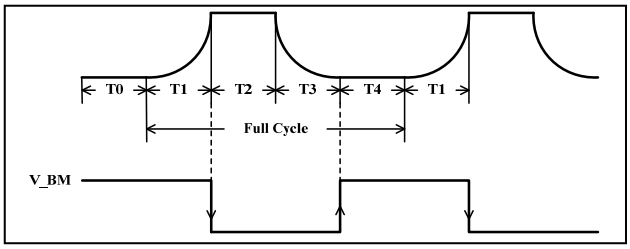


Figure 9 V_BM Signal

CASCADE FOR SYNCHRONIZATION OF CHIPS

Operating in the cascade mode can make two chips synchronize. By setting the CM bit of Configuration Register 2 (04h) to "0", IS31FL3199 operates as a master. There are two pins (CLK, I_AUD) for synchronization of chips. CLK pin can synchronize the breathing and I_AUD pin can synchronize the audio current.

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data and can be accessed via the I2C bus interface. The only difference between Software and Hardware shutdown mode is the current consumption.

Software Shutdown

By setting SSD bit of the Shutdown Register (00h) to "0", the IS31FL3199 will operate in software shutdown mode, wherein it consumes only 2μA (Typ.) current. When the IS31FL3199 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein it consumes only 1μA (Typ.) current. When the IS31FL3199 is in hardware shutdown mode, all current sources are switched off.

Register Access During Shutdown

All registers are accessible (read or write) while the IS31FL3199 is in either Software or Hardware shutdown. SDB turn on time is about 200μs, do not send I2C commands during a rising edge of the SDB pin as data will be corrupted. Data transfers during SDB falling edge, low or high steady state are permitted.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

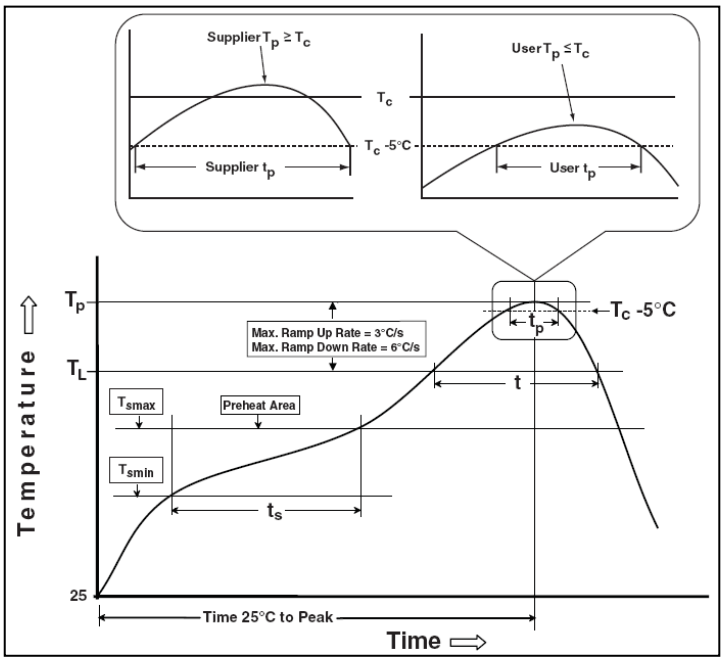


Figure 10 Classification Profile

PACKAGE INFORMATION

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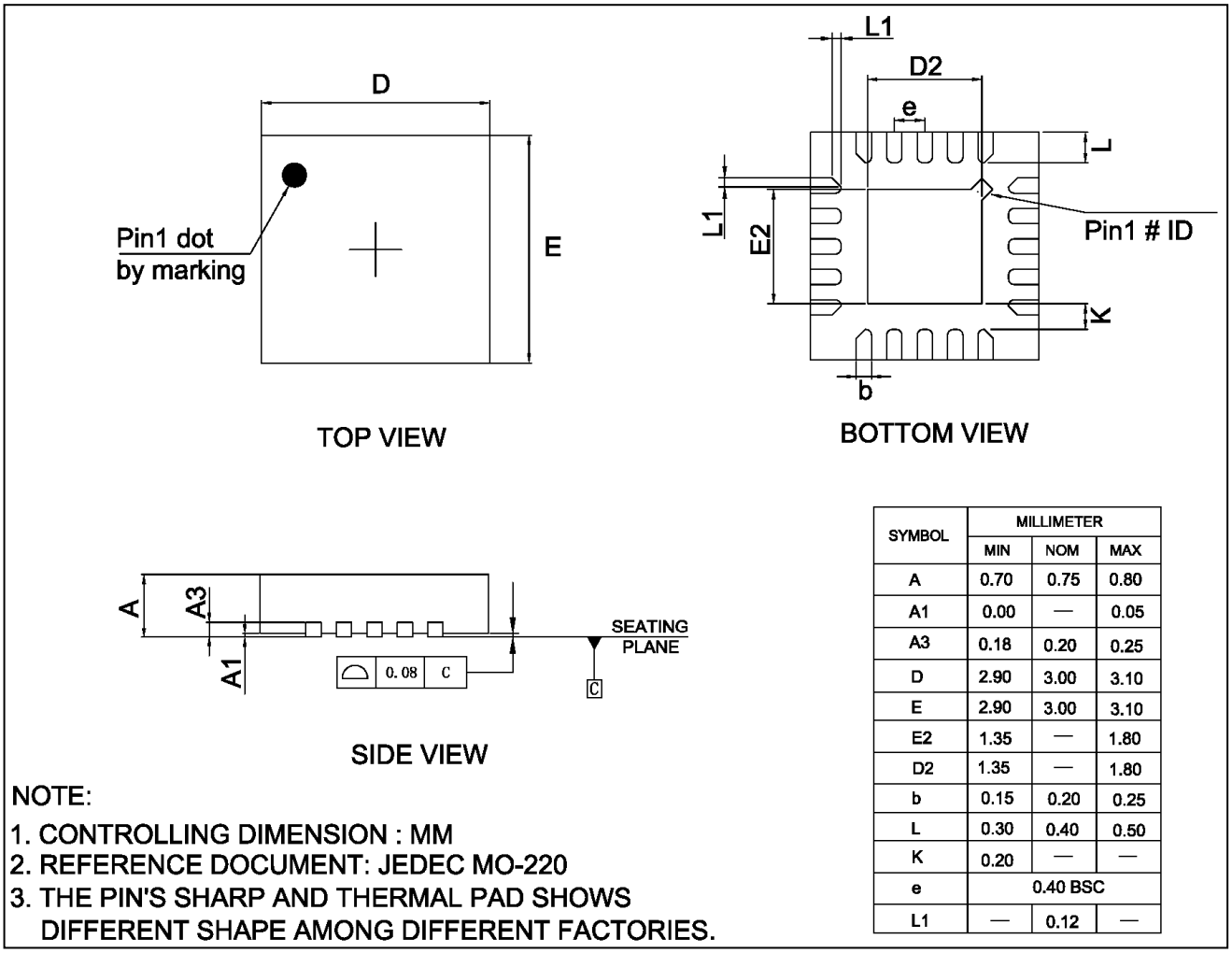

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E2	1.35	—	1.80
D2	1.35	—	1.80
b	0.15	0.20	0.25
L	0.30	0.40	0.50
K	0.20	—	—
e	0.40 BSC		
L1	—	0.12	—

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

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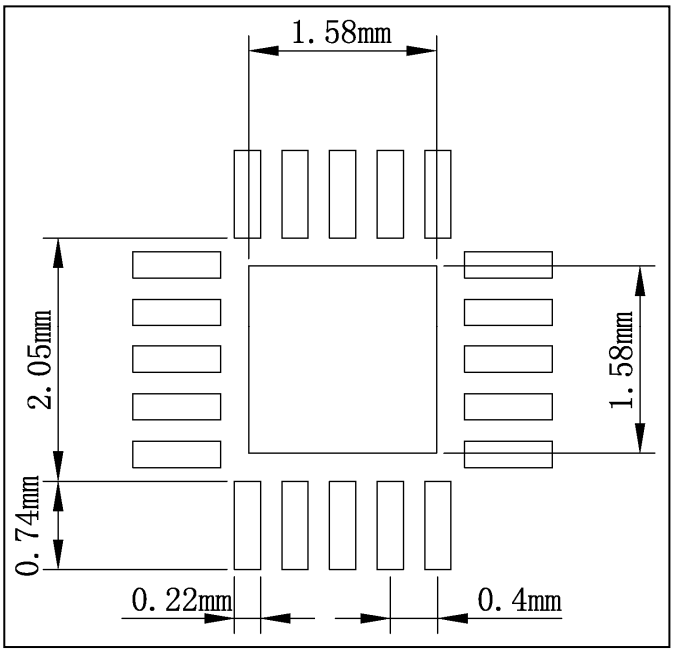

Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.12.26
B	Add ESD(HBM/CDM) value	2013.12.25
C	1. Update θ_{JA} value 2. Update IIH/IIL test condition 3. VIH, VIL condition revise to V_{CC}= 2.7V~5.5V 4. Add STANDARD MODE in DIGITAL INPUT SWITCHING CHARACTERISTICS 5. Add function block diagram 6. Add POWER ON SEQUENCE section in APPLICATION INFORMATION 7. Update POD 8. Add land pattern	2018.10.15

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