

TINSHARP

TG320240A-03

Specification For Approval

Customer Approval: _____ Date: _____

Prepared: _____ Check: _____ Approval: _____

Date: _____ Date: _____ Date: _____

Description

REV.	DESCREPTION	DATE
V00	First issue.	Jul-11-2006
V01	Update PIN Description.	Apr-25-2007
V02	Updata IC.	Dec-04-2007

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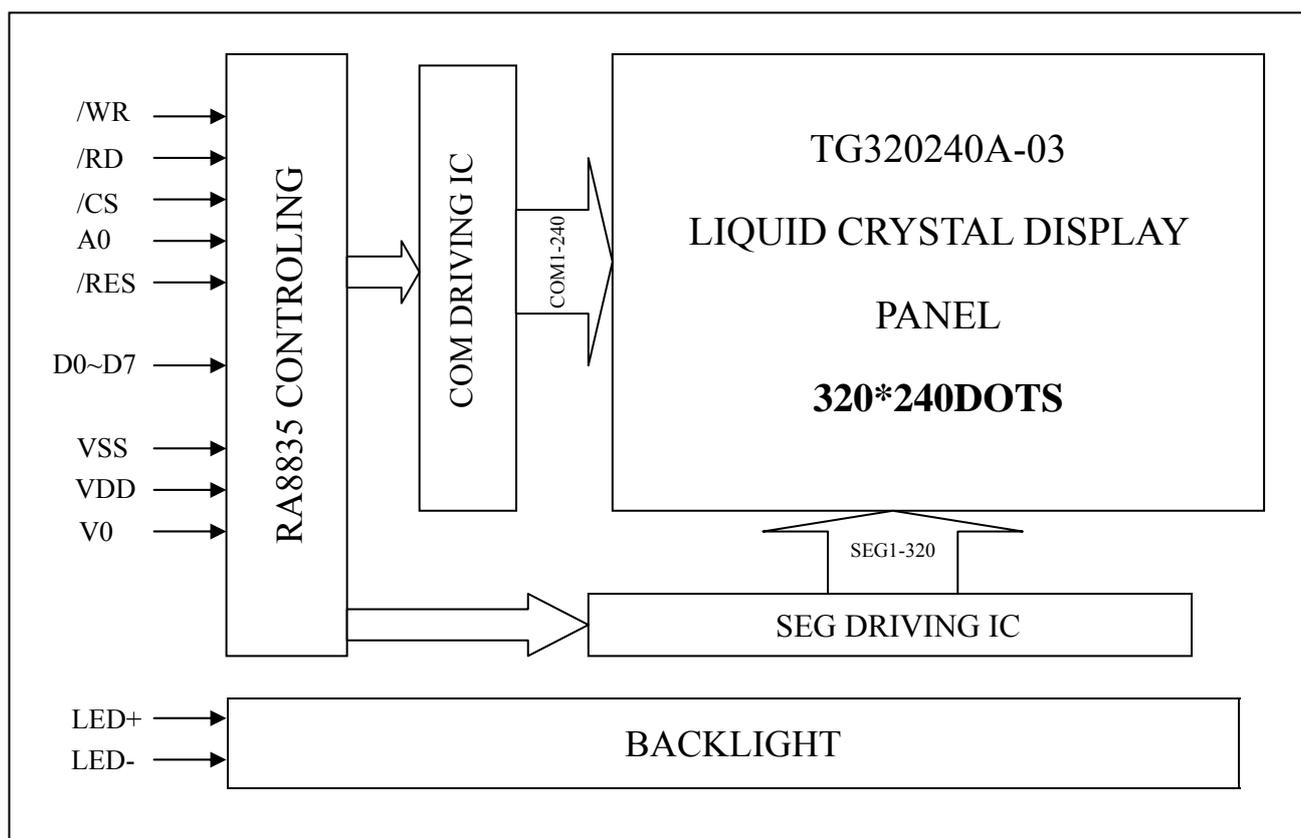
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1 . SPECIFICATIONS

1.1 FEATURES

Item	Contents	Unit
LCD TYPE	FSTN/Transflective/Positive/B-W	--
LCD duty	1/240	--
LCD bias	1/16	--
Module size(W x H x T)	139.0 X 100.0X 11.0	mm
Viewing area(W x H)	104.0 X 79.5	mm
Number of dots	320 X 240	dots
Dots size(W x H)	0.28 X 0.28	mm
Dots pitch(W x H)	0.30 X 0.30	mm

1.2. BLOCK DIAGRAM



1.4. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Absolute Voltage Range	V _{DD}	-0.3 to 7.0	V
Input Logic Voltage Range	V _{in}	-0.3 to V _{DD} +0.3	V
Power Dissipation	P _D	--	mW
Operating Temperature Range	T _{opg}	-10 to 60	°C
Storage Temperature Range	T _{stg}	-20 to 70	°C
Soldering Temperature(6 seconds)	T _{solder}	280+/-10	°C

Notes:

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heats stress the package.
2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines. (See section 6.2.)
3. All supply voltages are referenced to V_{SS} = 0V.

1.5.RA8835 CHARACTERISTIC

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = -15 to 65°C

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ.	Max.	
Supply Voltage	V _{DD}		4.5	5.0	5.5	V
Input Leakage Current	I _{LI}		--	0.5	20	uA
Output Leakage Current	I _{LO}		--	1.0	20	uA
Operating Supply Current	I _{OPR}		--	20	30	mA
Quiescent Supply Current	I _Q		--	5	50	uA
Oscillator Frequency	F _{osc}		1.0	--	10	MHz
External Frequency	F _{cl}		1.0	--	10	MHz
Oscillator Feedback Resistor	R _f		0.5	1.0	3.0	Mohm
High-Level Input Voltage	V _{IHC}		0.8V _{DD}	--	V _{DD}	V
Low-Level Input Voltage	V _{ILC}		V _{SS}	--	0.2V _{DD}	V
High-Level Output Voltage	V _{OHC}		V _{DD} -0.4	--	--	V
Low-Level Output Voltage	V _{OLC}		--	--	V _{SS} +0.4	V
Rising-edge threshold Voltage	V _{T+}		0.5V _{DD}	0.7V _{DD}	0.8V _{DD}	V
Falling-edge threshold Voltage	V _{T-}		0.2V _{DD}	0.3V _{DD}	0.5V _{DD}	V

Notes:

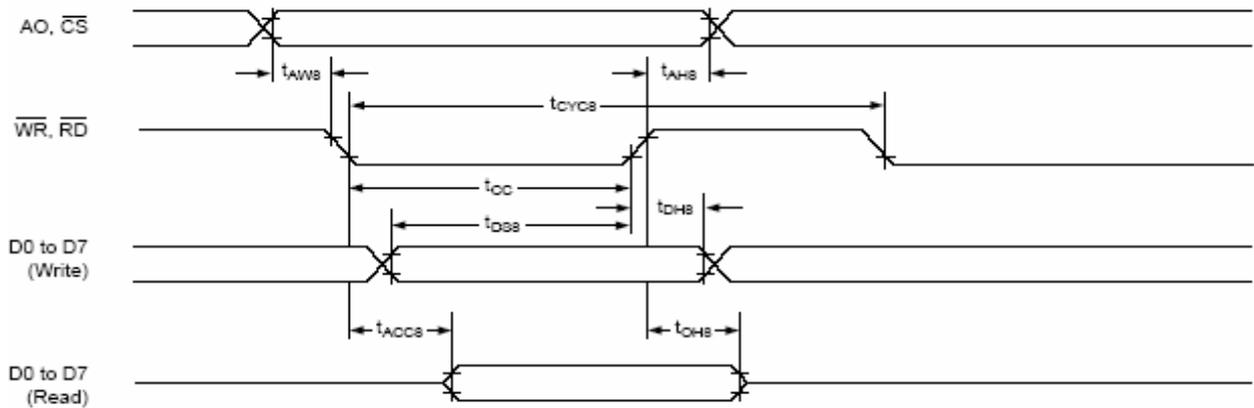
1. D0 to D7, A0, CS, RD, WR, VD0 to VD7, VA0 to VA15, VRD, VWR and VCE are TTL-level inputs.
2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.
3. RES is a Schmitt-trigger input. The pulse width on RES must be at least 200 ms. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. f_{osc} = 10 MHz, no load (no display memory), internal character generator, 256 ´ 200 pixel display. The operating

supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.

5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
6. Because the oscillator circuit input bias current is in the order of μA , design the printed circuit board so as to reduce leakage currents.

1.6 RA8835 TIMING DIAGRAMS

1.6.1. 8080 family interface timing



$T_a = -10$ to 65°C

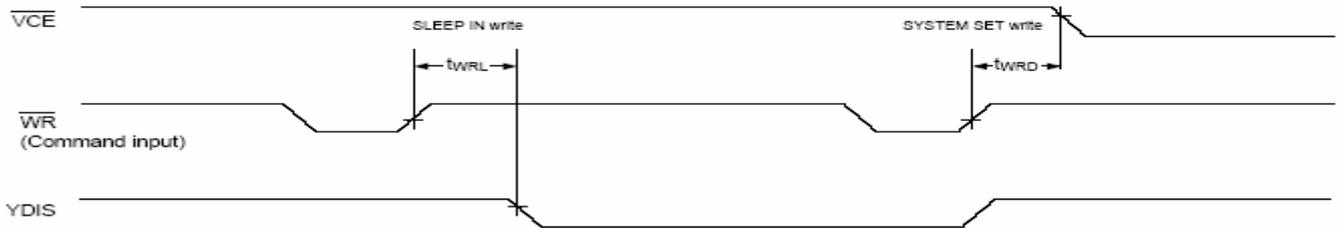
Signal	Symbol	Parameter	Range		Unit	Condition
			Min.	Max.		
A0,/CS	TAH8	Address hold time	50	--	ns	CL=100pF
	TAW8	Address set up time	10	--	ns	
/WR,/RD	tCYC8	System cycle time	Reference note		ns	
	tCC	Strobe pulse width	160		ns	
DB0 to DB7	TDS8	Data set up time	160		ns	
	TDH8	Data hold time	15		ns	
	TACC8	/RD access time		80	ns	
	TOH8	Output disable time	30	50	ns	

Note: For memory control and system control commands:

$$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$$

For all other commands:

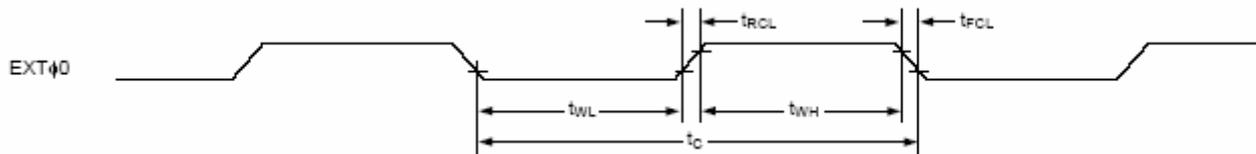
$$t_{CYC8} = 4t_C + t_{CC} + 30$$

1.6.2. SLEEP IN command timing


Ta = -10 to 65°C

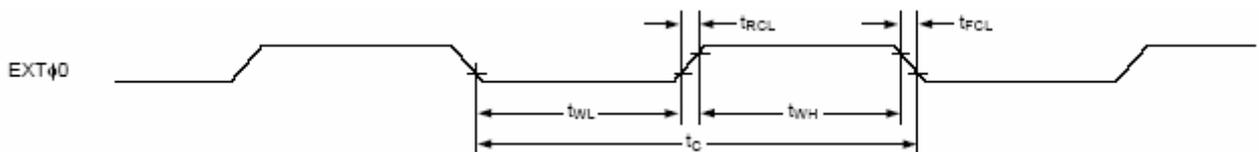
Signal	Symbol	Parameter	VDD=4.5 to 5.5V		Unit	Condition
			Min.	Max.		
/WR	TWRD	/VCE falling-edge delay time	25	--	ns	CL=100pF
	TWRL	YDIS falling-edge delay time	25	--	ns	

Notes:
 $T_{WRD} = 18t_c + t_{OSS} + 40$ (Toss is the time delay from the sleep state until stable operation)

 $T_{WRL} = 36t_c \times [TC/R] \times [1/f] + 70$
External oscillator signal timing


Ta = -10 to 65°C

Signal	Symbol	Parameter	VDD=4.5V to 5.5V		Unit
			Min.	Max.	
EXT	TRCL	External clock rise time	--	20	ns
	TFCL	External clock falling time	--	20	ns
	TWH	External clock high-level pulse width			
	TWL	External clock Low-level pulse width			
	TC	External clock period	130	--	ns

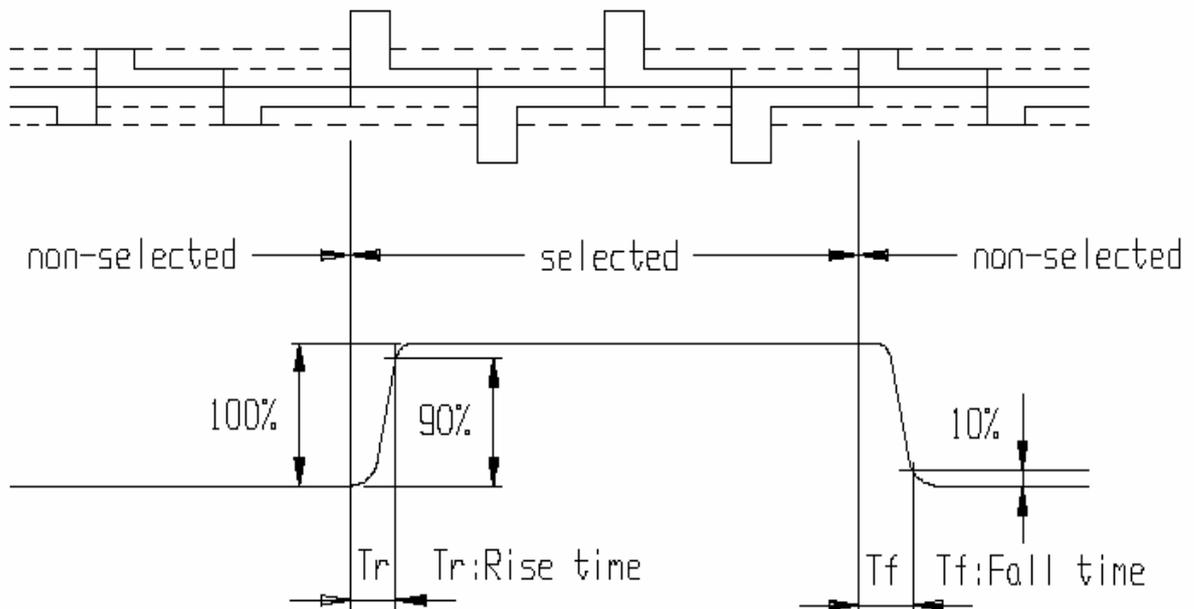
Notes:
 $1. (T_c - T_{RCL} - T_{FCL}) \times 475/1000 < T_{WH}, T_W$
 $2. (T_c - T_{RCL} - T_{FCL}) \times 525/1000 > T_{WH}, T_W$
External oscillator signal timing


Signal	Symbol	Parameter	VDD = 4.5 to 5.5v		Unit	condition
			Min.	Max.		
	Tr	Rise time	10	30	ns	CL=100pF
	Tf	Fall time	10	30	ns	
XSCL	Tcx	Shift clock cycle time	4Tc	--	ns	
	Twx	XSCL clock pulse width	2Tc-80	--	ns	
SD0 to XD3	T _{DH}	X data hold time	2Tc-80	--	ns	
	T _{DS}	X data setup time	2Tc-80	--	ns	
Lp	T _{LS}	Latch data setup time	2Tc-75	--	ns	
	T _{WL}	Lp pulse width	4Tc-75	--	ns	
	T _{LD}	Lp delay time from XSCL	4Tc-80	--	ns	
WF	T _{DF}	Permitted WF delay	10	60	ns	
YD	T _{DHY}	Y data hold time	2Tc-30	--	ns	

1.7 ELECTRO-OPTICAL CHARACTERISTIC

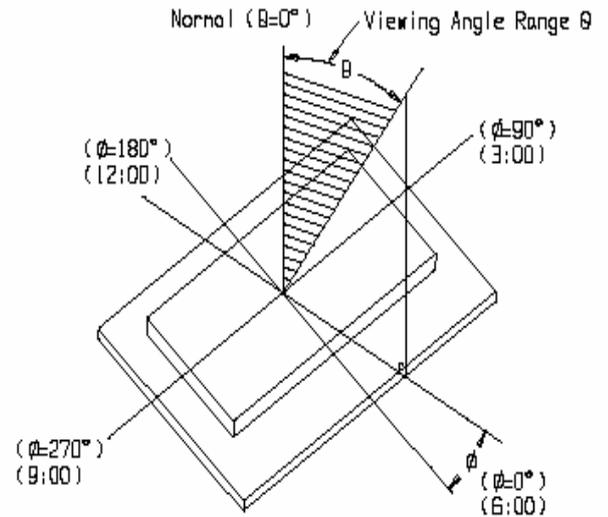
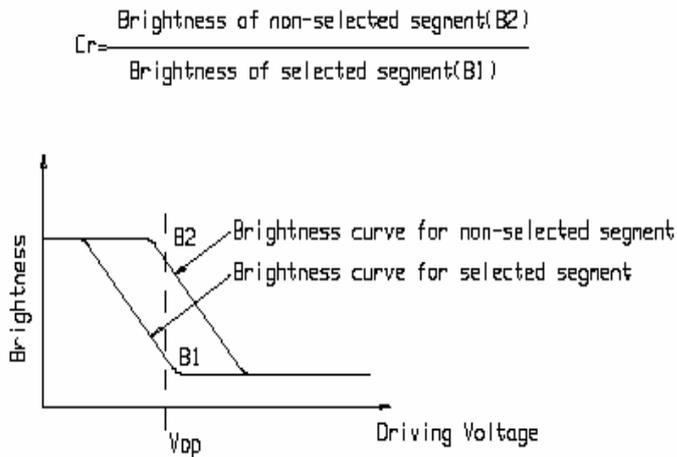
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Contrast ratio	K	$\theta=0, \Phi=0$	-	2	-		2
Response time(rise)	Tr	25°C		-	-	ms	1
Response time(fall)	Tf			-	-		1
Viewing angle	Φ	25°C		-		deg.	3
	θ			-			3

Note1: Definition of response time.



Note2: Definition of contrast ratio 'Cr' .

Note3: Definition of viewing angle range 'θ'.



1.8 LED BACKLIGHT CHARACTERISTIC

1.8.1 ABSOLUTE MAXIMUM RATINGS($T_a=25^\circ\text{C}$)

Item	Symbol	Conditions	Rating	Unit
Absolute maximum forward current	I_{fm}		180	mA
Peak forward current	I_{fp}	I_{mac} 脉冲, 1/10 占空比 I_{msec} plus 10% Duty Cycle	540	mA
Reverse voltage	V_r		5	V
Power dissipation	P_d		630	mW
Operating Temperature Range	T_{OPr}		-20~+70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}		-30~+80	$^\circ\text{C}$

1.8.2 ELECTRICAL –OPTICAL CHARACTERISTICS($T_a=25^\circ\text{C}$)

Color	Wavelength $\lambda_p(\text{nm})$	Min.Forward Voltage(V)	Typ.Forward Voltage(V)	Max.Forward Voltage(V)	Forward Current (mA)
WHITE	white	3.0	3.2	3.4	135

2. MODULE STRUCTURE

2.1 PIN DESCRIPTION

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground
2	VDD	+5V	Power for logic operating.
3	V0	--	Adjust LCD contrast.
4	/WR	H/L	This is active LOW for data writing. The signals on the data bus are latched at the rising edge of the /WR signal.
5	/RD	H/L	This is active LOW for data read.
6	/CS	H/L	This is the chip select signal, When CS is set "L,"the chip is active
7	A0	H/L	A0 = "L": Indicates that D0 to D7 are display data. A0 = "H": Indicates that D0 to D7 are control data.
8	/RES	H/L	When /RES is set to "L," the settings are initialized.
9	DB0	H/L	This is an 8-bit bi-directional data bus.
10	DB1		
11	DB2		
12	DB3		
13	DB4		
14	DB5		
15	DB6		
16	DB7		
17	LED+	+5V	Power for the backlight
18	LED-	0V	The backlight ground.

2.2 INSTRUCTION SET

2.2.1 The Command Set

Class	Command	Code											Hex	Command Description	Command Read Parameters	
		\overline{RD}	\overline{WR}	A0	D7	D6	D5	D4	D3	D2	D1	D0			No. of Bytes	Section
System control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	8.2.1
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	8.2.2
Display control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	8.3.1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	8.3.2
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	8.3.3
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	8.3.6
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	8.3.4
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	8.3.7
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	8.3.5
Drawing control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	8.4.1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	8.4.2
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	8.5.1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	8.5.2

Notes:

- In general, the internal registers of the RA8835 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged. 2-byte parameters (where two bytes are treated as 1 data item) are handled as follows: a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address. b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.
- APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

2.2.2 SYSTEM CONTROL COMMANDS

SYSTEM SET

Initializes the device, sets the window sizes, and selects the LCD interface format. Since this command sets the basic operating parameters of the RA8835 series, an incorrect SYSTEM SET command may cause other commands to operate incorrectly.

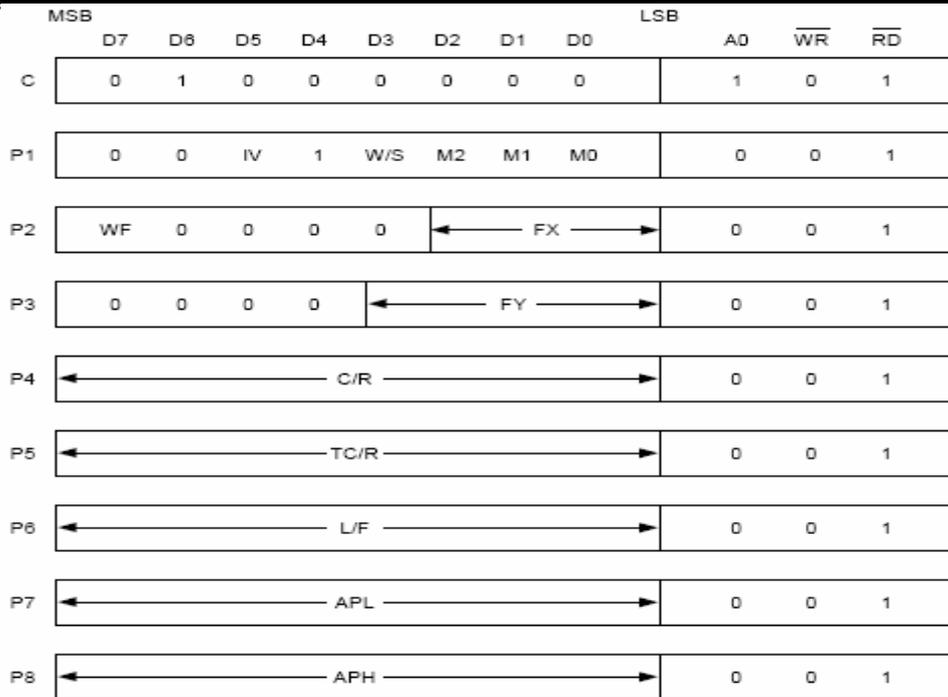


Figure 1. SYSTEM SET instruction

C

This control byte performs the following:

1. Resets the internal timing generator
2. Disables the display
3. Cancels sleep mode

Parameters following P1 are not needed if only canceling sleep mode.

M0

Selects the internal or external character generator ROM. The internal character generator ROM contains 160, 5x7 pixel characters, as shown in figure 70. These characters are fixed at fabrication by the metallization mask. The external character generator ROM, on the other hand, can contain up to 256 user-defined characters.

M0 = 0: Internal CG ROM

M0 = 1: External CG ROM

Note that if the CG ROM address space overlaps the display memory address space, that portion of the display memory cannot be written to.

M1

Selects the memory configuration for user-definable characters. The CG RAM codes select one of the 64 codes shown in figure 46.

M1 = 0: No D6 correction.

The CG RAM1 and CG RAM2 address spaces are not contiguous, the CG RAM1 address space is treated as character generator RAM, and the CG RAM2 address space is treated as character generator ROM.

M1 = 1: D6 correction.

The CG RAM1 and CG RAM2 address spaces are contiguous and are both treated as character generator RAM.

M2

Selects the height of the character bitmaps. Characters more than 16 pixels high can be displayed by

creating a bitmap for each portion of each character and using the RA8835 series graphics mode to reposition them.

M2 = 0: 8-pixel character height (2716 or equivalent ROM)

M2 = 1: 16-pixel character height (2732 or equivalent ROM)

W/S

Selects the LCD drive method.

W/S = 0: Single-panel drive

W/S = 1: Dual-panel drive

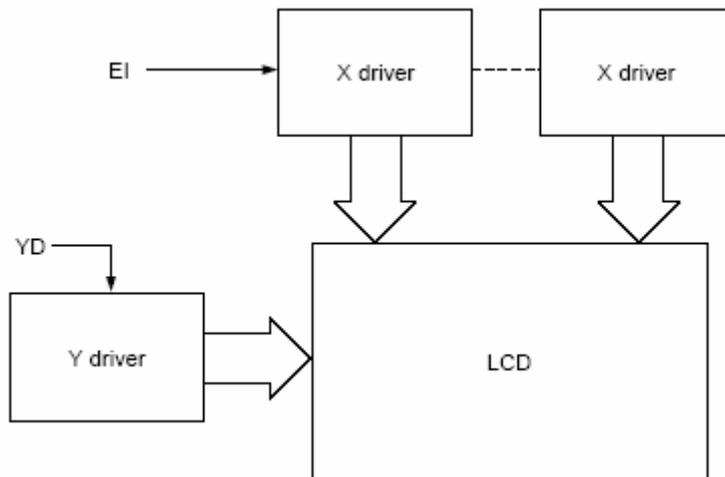


Figure 2. Single-panel display

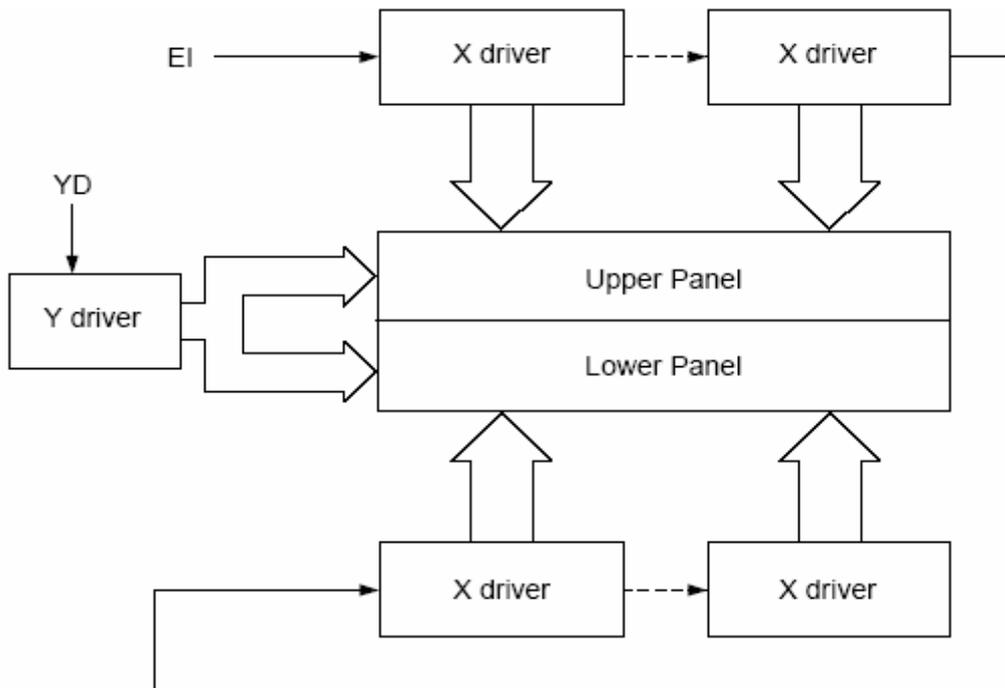


Figure 3. Above and below two-panel display

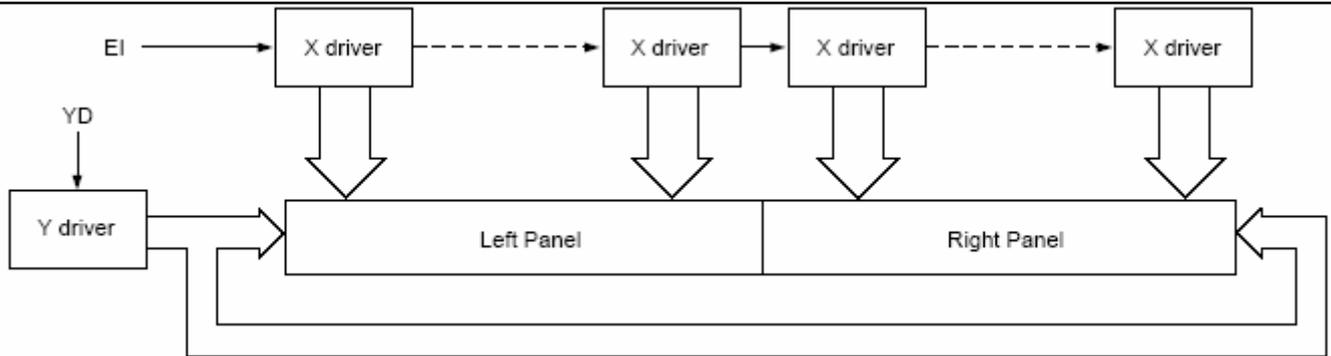


Figure 4. Left-and-right two-panel display

Note

There are no Seiko Epson LCD units in the configuration shown in Figure 4.

Table 2. LCD parameters

Parameter	W/S = 0		W/S = 1	
	IV = 1	IV = 0	IV = 1	IV = 0
C/R	C/R	C/R	C/R	C/R
TC/R	TC/R	TC/R (See note 1.)	TC/R	TC/R
L/F	L/F	L/F	L/F	L/F
SL1	00H to L/F	00H to L/F + 1 (See note 2.)	(L/F) / 2	(L/F) / 2
SL2	00H to L/F	00H to L/F + 1 (See note 2.)	(L/F) / 2	(L/F) / 2
SAD1	First screen block	First screen block	First screen block	First screen block
SAD2	Second screen block	Second screen block	Second screen block	Second screen block
SAD3	Third screen block	Third screen block	Third screen block	Third screen block
SAD4	Invalid	Invalid	Fourth screen block	Fourth screen block
Cursor movement range	Continuous movement over whole screen		Above-and-below configuration: continuous movement over whole screen	

Notes:

1. See table 26 for further details on setting the C/R and TC/R parameters when using the HDOT SCR command.
2. The value of SL when IV = 0 is equal to the value of SL when IV = 1, plus one.

IV

Screen origin compensation for inverse display. IV is usually set to 1. The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer. However, inverted characters at the top or left of the screen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters.

The IV flag causes the RA8835 series to offset the text screen against the graphics back layer by one vertical pixel. Use the horizontal pixel scroll function (HDOT SCR) to shift the text screen 1 to 7 pixels to the right. All characters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters.

See Section 10.5 for information on scrolling.

IV = 0: Screen top-line correction

IV = 1: No screen top-line correction

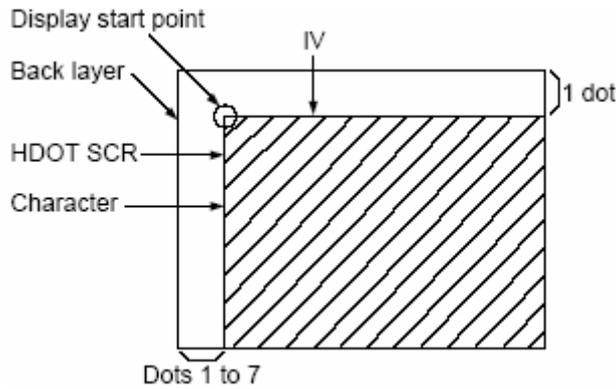


Figure 5. IV and HDOT SCR adjustment

FX

Define the horizontal character size. The character width in pixels is equal to $FX + 1$, where FX can range from 00 to 07H inclusive. If data bit 3 is set (FX is in the range 08 to 0FH) and an 8-pixel font is used, a space is inserted between characters.

Table 3. Horizontal character size selection

FX					[FX] character width (pixels)
HEX	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8

Since the RA8835 series handles display data in 8-bit units, characters larger than 8 pixels wide must be formed from 8-pixel segments. As Figure 6 shows, the remainder of the second eight bits are not displayed. This also applies to the second screen layer. In graphics mode, the normal character field is also eight pixels. If a wider character field is used, any remainder in the second eight bits is not displayed.

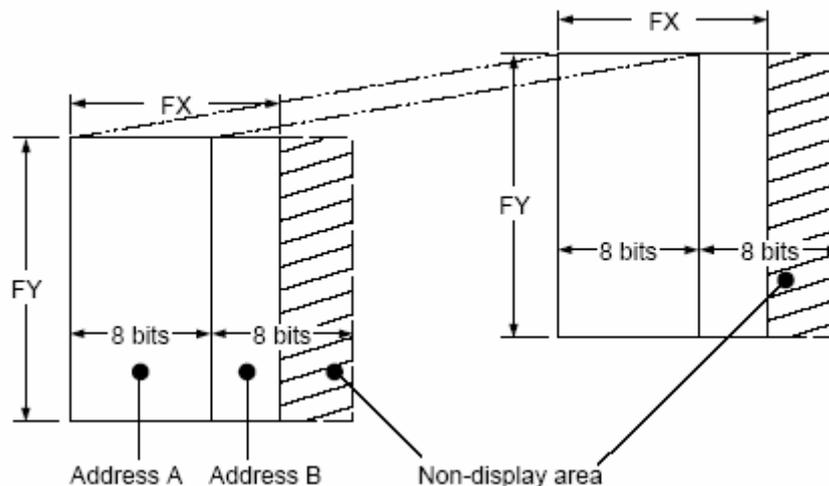


Figure 6. FX and FY display addresses

WF

Selects the AC frame drive waveform period. WF is usually set to 1.

WF = 0: 16-line AC drive

WF = 1: two-frame AC drive

In two-frame AC drive, the WF period is twice the frame period.

In 16-line AC drive, WF inverts every 16 lines.

Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

FY

Sets the vertical character size. The height in pixels is equal to FY + 1.

FY can range from 00 to 0FH inclusive.

Set FY to zero (vertical size equals one) when in graphics mode.

Table 4. Vertical character size selection

FY					[FY] character height (pixels)
HEX	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8
↓	↓	↓	↓	↓	↓
0E	1	1	1	0	15
0F	1	1	1	1	16

C/R

Sets the address range covered by one display line, that is, the number of characters less one, multiplied by the number of horizontal bytes per character.

C/R can range from 0 to 239.

For example, if the character width is 10 pixels, then the address range is equal to twice the number of characters, less 2. See Section 16.1.1 for the calculation of C/R.

[C/R] cannot be set to a value greater than the address range. It can, however, be set smaller than the address range, in which case the excess display area is blank. The number of excess pixels must not exceed 64.

Table 5. Display line address range

C/R									[C/R] bytes per display line
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4F	0	1	0	0	1	1	1	1	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

TC/R

Sets the length, including horizontal blanking, of one line. The line length is equal to $TC/R + 1$, where TC/R can range from 0 to 255.

TC/R must be greater than or equal to $C/R + 4$. Provided this condition is satisfied, $[TC/R]$ can be set according to the equation given in section 16.1.1 in order to hold the frame period constant and minimize jitter for any given main oscillator frequency, f_{OSC} .

Table 6. Line length selection

HEX	TC/R								[TC/R] line length (bytes)
	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
52	0	1	0	1	0	0	1	0	83
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

L/F

Sets the height, in lines, of a frame. The height in lines is equal to $L/F + 1$, where L/F can range from 0 to 255.

Table 7. Frame height selection

HEX	L/F								[L/F] lines per frame
	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

If W/S is set to 1, selecting two-screen display, the number of lines must be even and L/F must, therefore, be an odd number.

AP

Defines the horizontal address range of the virtual screen.

APL is the least significant byte of the address.

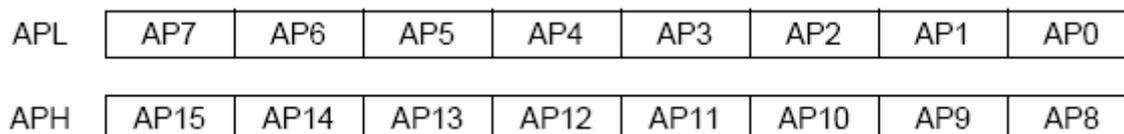


Figure 7. AP parameters

Table 8. Horizontal address range

Hex code				[AP] addresses per line
APH	APL			
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	0	5	0	80
↓	↓	↓	↓	↓
F	F	F	E	$2^{16} - 2$
F	F	F	F	$2^{16} - 1$

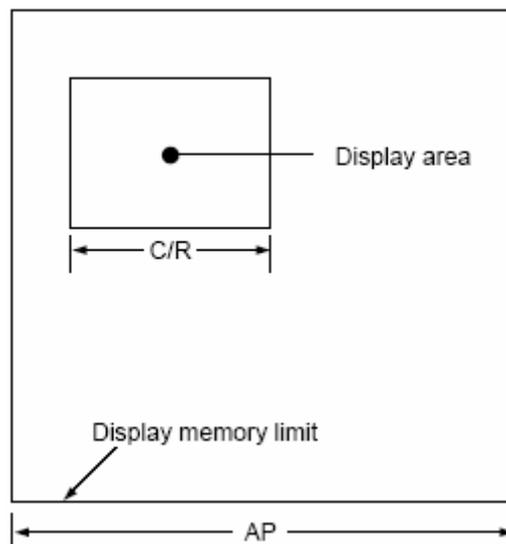


Figure 8. AP and C/R relationship

SLEEP IN

Places the system in standby mode. This command has no parameter bytes. At least one blank frame after receiving this command, the RA8835F halts all internal operations, including the oscillator, and enters the sleep state.

Blank data is sent to the X-drivers, and the Y-drivers have their bias supplies turned off by the YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays.

The internal registers of the RA8835 series maintain their values during the sleep state. The display memory control pins maintain their logic levels to ensure that the display memory is not corrupted.

The RA8835 series can be removed from the sleep state by sending the SYSTEM SET command with only the P1 parameter. The DISP ON command should be sent next to enable the display.



Figure 9. SLEEP IN instruction

- The YDIS signal goes LOW between one and two frames after the SLEEP IN command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power-down signal for the LCD unit. This can be done by having YDIS turn off the relatively high power LCD drive supplies at the same time as it blanks the display.

2. Since all internal clocks in the RA8835 series are halted while in the sleep state, a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on. If reliability is a prime consideration, turn off the LCD drive supplies before issuing the SLEEP IN command.
3. Note that, although the bus lines become high impedance in the sleep state, pull-up or pull-down resistors on the bus will force these lines to a known state.

2.2.3 Display Control Commands

DISP ON/OFF

Turns the whole display on or off. The single-byte parameter enables and disables the cursor and layered screens, and sets the cursor and screen flash rates. The cursor can be set to flash over one character or over a whole line

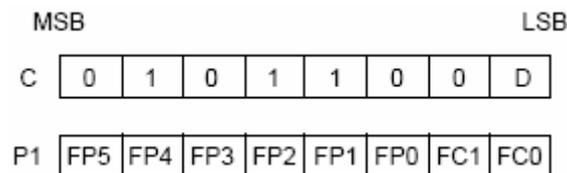


Figure 10. DISP ON/OFF parameters

(1) D

Turns the display ON or OFF. The D bit takes precedence over the FP bits in the parameter.

D = 0: Display OFF

D = 1: Display ON

(2) FC

Enables/disables the cursor and sets the flash rate. The cursor flashes with a 70% duty cycle (ON/OFF).

Table 9. Cursor flash rate selection

FC1	FC0	Cursor display	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at $f_{FR}/32$ Hz (approx. 2 Hz)
1	1		Flash at $f_{FR}/64$ Hz (approx. 1 Hz)

Note: As the MWRITE command always enables the cursor, the cursor position can be checked even when performing consecutive writes to display memory while the cursor is flashing.

(3) FP

Each pair of bits in FP sets the attributes of one screen block, as follows. The display attributes are as follows:

Table 10. Screen block attribute selection

FP1	FP0	First screen block (SAD1)	
FP3	FP2	Second screen block (SAD2, SAD4). See note.	
FP5	FP4	Third screen block (SAD3)	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at $f_{FR}/32$ Hz (approx. 2 Hz)
1	1		Flash at $f_{FR}/4$ Hz (approx. 16 Hz)

Note

If SAD4 is enabled by setting W/S to 1, FP3 and FP2 control both SAD2 and SAD4. The attributes of SAD2 and SAD4 cannot be set independently.

SCROLL
(1) C

Sets the scroll start address and the number of lines per scroll block. Parameters P1 to P10 can be omitted if not required. The parameters must be entered sequentially as shown in Figure 11.

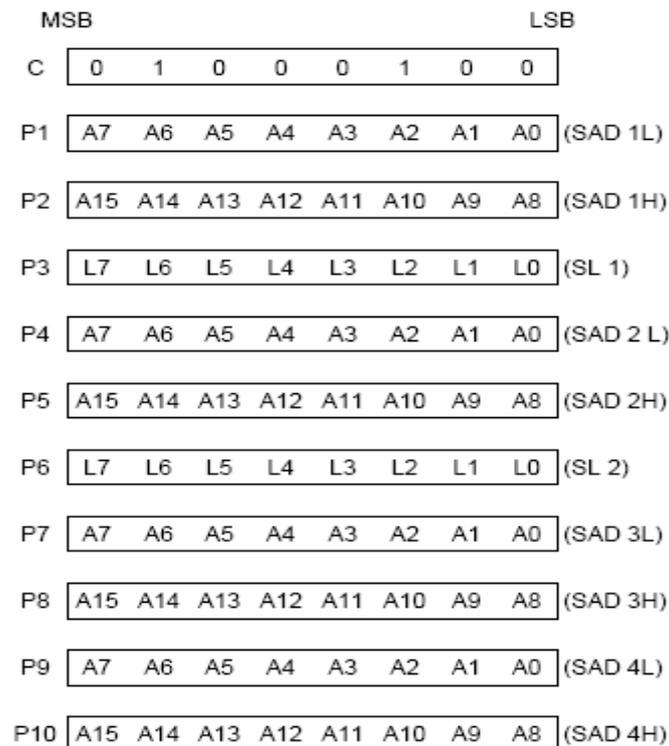


Figure 11. SCROLL instruction parameters

Note: Set parameters P9 and P10 only if both two-screen drive (W/S = 1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

Table 11. Screen block start address selection

SL1, SL2									[SL] screen lines
HEX	L7	L6	L5	L4	L3	L2	L1	L0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

(2) SL1, SL2

SL1 and SL2 set the number of lines per scrolling screen. The number of lines is SL1 or SL2 plus one. The relationship between SAD, SL and the display mode is described below.

Table 12. Text display mode

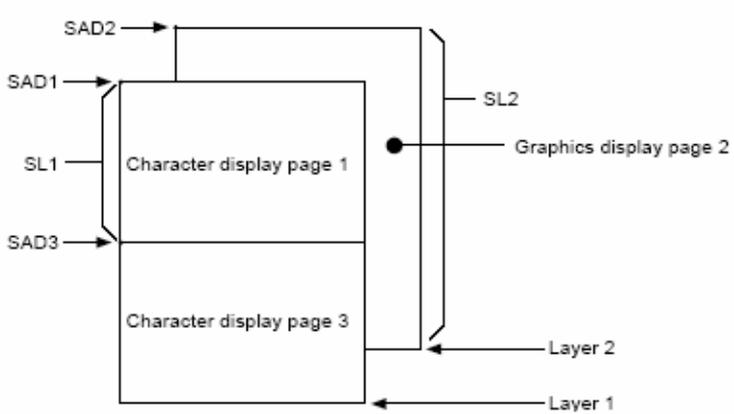
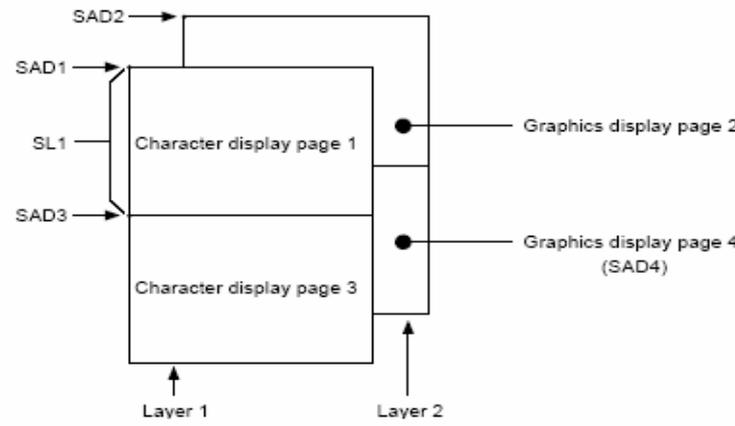
W/S	Screen	First Layer	Second Layer
0	First screen block	SAD1	SAD2
	Second screen block	SL1	SL2
	Third screen block (partitioned screen)	SAD3 (see note 1) Set both SL1 and SL2 to L/F + 1 if not using a partitioned screen.	
	Screen configuration example:		
			

Table 12. Text display mode (continued)

W/S	Screen	First Layer	Second Layer
1	Upper screen	SAD1 SL1	SAD2 SL2
	Lower screen	SAD3 (See note 2.)	SAD4 (See note 2.)
	Set both SL1 and SL2 to $((L/F) / 2 + 1)$.		
	Screen configuration example:		


Notes:

1. SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of lines (set by SL1 and SL2).
3. Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set in this mode.

Table 13. Graphics display mode

W/S	Screen	First Layer	Second Layer	Third Layer
0	Two-layer composition	SAD1 SL1	SAD2 SL2	—
	Upper screen	SAD3 (see note 3.) Set both SL1 and SL2 to $L/F + 1$ if not using a partitioned screen		—
	Screen configuration example:			

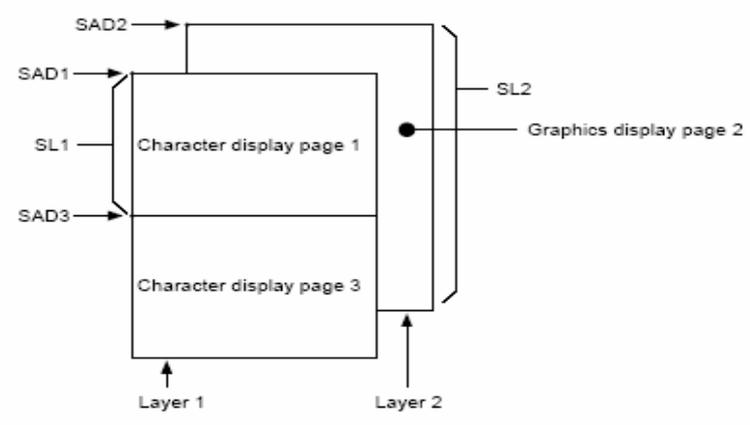
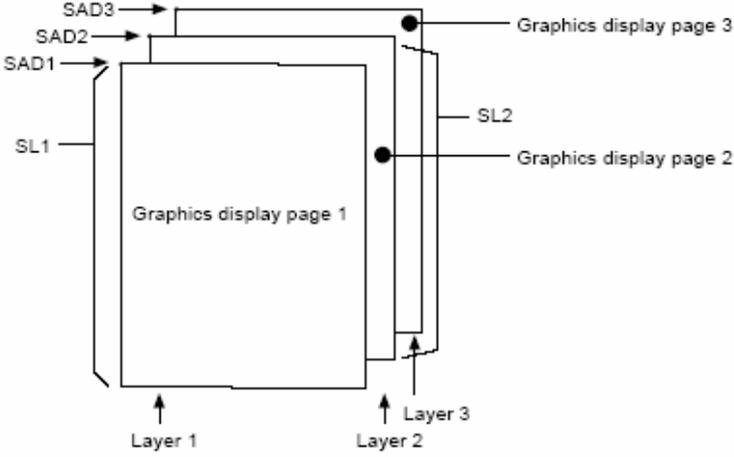
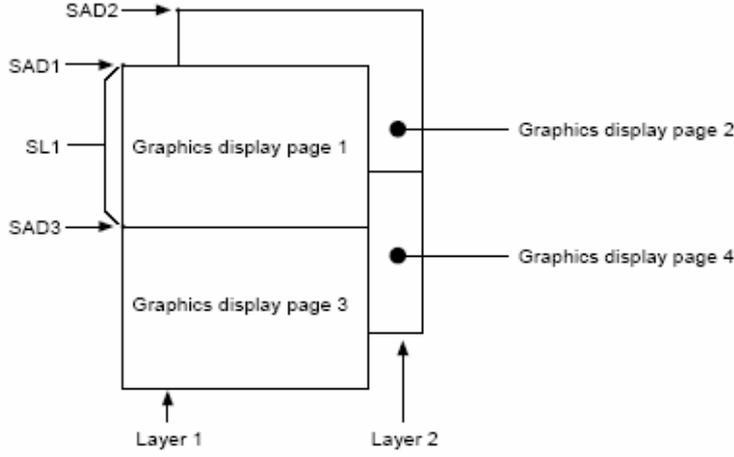


Table 13. Graphics display mode (continued)

W/S	Screen	First Layer	Second Layer	Third Layer
0	Three-layer configuration	SAD1 SL1 = L/F + 1	SAD2 SL2 = L/F + 1	SAD3 —
	Screen configuration example: 			
1	Upper screen	SAD1 SL1	SAD2 SL2	—
	Lower screen	SAD3 (See note 2.)	SAD4 (See note 2.)	—
	Set both SL1 and SL2 to $((L/F) / 2 + 1)$. Screen configuration example (See note 3.): 			

Notes:

- SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of lines (set by SL1 and SL2).
- Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set.
- If, and only if, W/S = 1, the differences between SL1 and $(L/F + 1) / 2$, and between SL2 and $(L/F + 1) / 2$, are blanked.

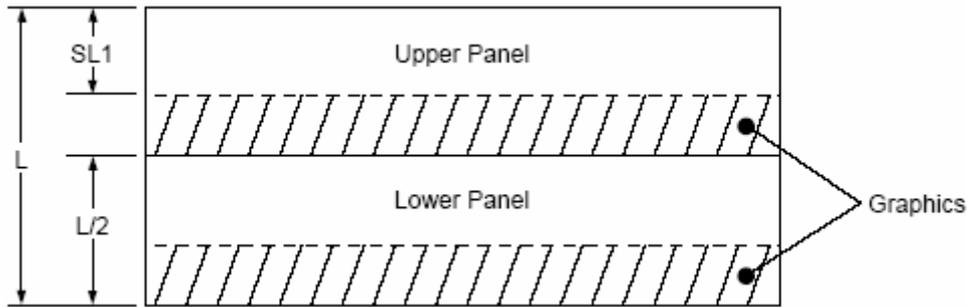


Figure 12. Two-panel display height

CSRFORM

Sets the cursor size and shape. Although the cursor is normally only used in text displays, it may also be used in graphics displays when displaying special characters.

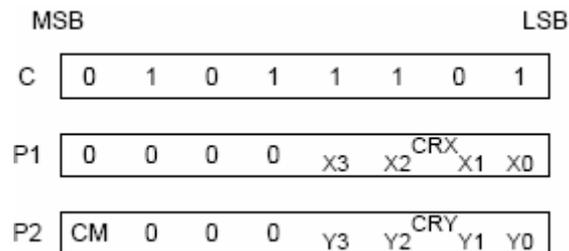


Figure 13. CSRFORM parameter bytes

(1) CRX

Sets the horizontal size of the cursor from the character origin. CRX is equal to the cursor size less one. CRX must be less than or equal to FX.

Table 14. Horizontal cursor size selection

HEX	CRX				[CRX] cursor width (pixels)
	X3	X2	X1	X0	
0	0	0	0	0	1
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
4	0	1	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

CRY

Sets the location of an underscored cursor in lines, from the character origin. When using a block cursor, CRY sets the vertical size of the cursor from the character origin. CRY is equal to the number of lines less one.

Table 15. Cursor height selection

CRY					[CRY] cursor height (lines)
HEX	Y3	Y2	Y1	Y0	
0	0	0	0	0	Illegal
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
8	1	0	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

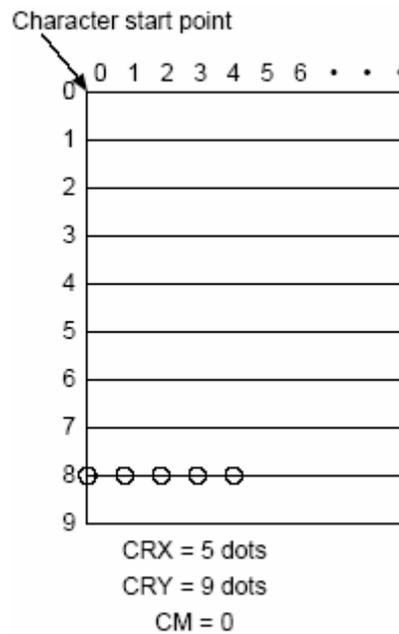


Figure 14. Cursor size and position

(2) CM

Sets the cursor shape. Always set CM to 1 when in graphics mode.

CM = 0: Underscore cursor

CM = 1: Block cursor

CSRDIR

Sets the direction of automatic cursor increment. The cursor can move left or right one character, or up or down by the number of bytes specified by the address pitch, AP. When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.



Figure 15. CSRDIR parameters

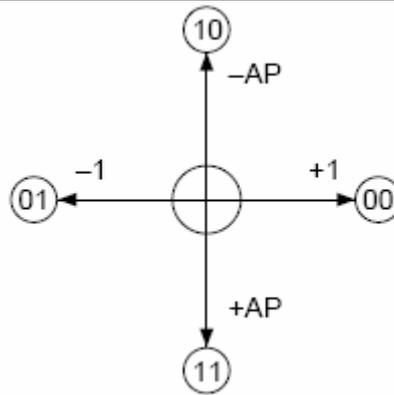


Figure 16. Cursor direction

Table 16. Cursor shift direction

C	CD1	CD0	Shift direction
4CH	0	0	Right
4DH	0	1	Left
4EH	1	0	Up
4FH	1	1	Down

Note: Since the cursor moves in address units even if FX³ 9, the cursor address increment must be preset for movement in character units. See Section 9.3.

OVLAY

Selects layered screen composition and screen text/ graphics mode.

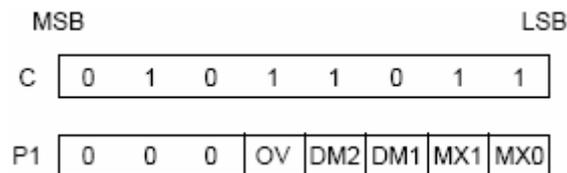


Figure 17. OVLAY parameters

(1) MX0, MX1

MX0 and MX1 set the layered screen composition method, which can be either OR, AND, Exclusive-OR or Priority-OR. Since the screen composition is organized in layers and not by screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks.

The Priority-OR mode is the same as the OR mode unless flashing of individual screens is used.

Table 17. Composition method selection

MX1	MX0	Function	Composition Method	Applications
0	0	$L1 \cup L2 \cup L3$	OR	Underlining, rules, mixed text and graphics
0	1	$(L1 \oplus L2) \cup L3$	Exclusive-OR	Inverted characters, flashing regions, underlining
1	0	$(L1 \cap L2) \cup L3$	AND	Simple animation, three-dimensional appearance
1	1	$L1 > L2 > L3$	Priority-OR	

Notes:

L1: First layer (text or graphics). If text is selected, layer L3 cannot be used.

L2: Second layer (graphics only)

L3: Third layer (graphics only)

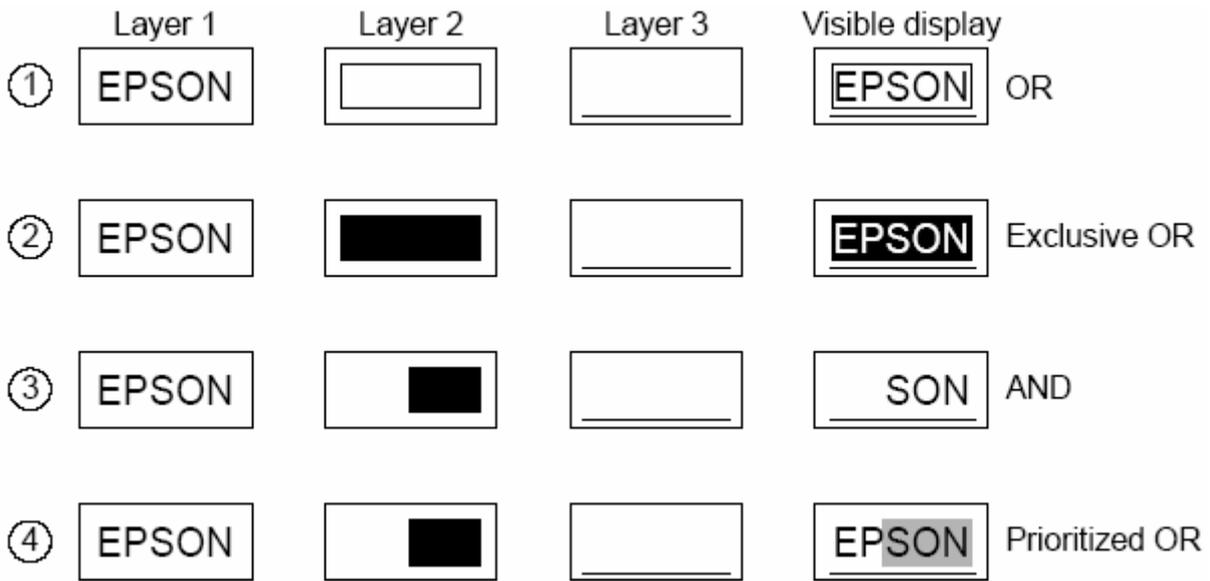


Figure 18. Combined layer display

Notes:

L1: Not flashing

L2: Flashing at 1 Hz

L3: Flashing at 2 Hz

(2) DM1, DM2

DM1 and DM2 specify the display mode of screen blocks 1 and 3, respectively.

DM1/2 = 0: Text mode

DM1/2 = 1: Graphics mode

Note 1: Screen blocks 2 and 4 can only display graphics.

Note 2: DM1 and DM2 must be the same, regardless of the setting of W/S.

(3) OV

Specifies two- or three-layer composition in graphics mode.

OV = 0: Two-layer composition

OV = 1: Three-layer composition

Set OV to 0 for mixed text and graphics mode.

CGRAM ADR

Specifies the CG RAM start address.

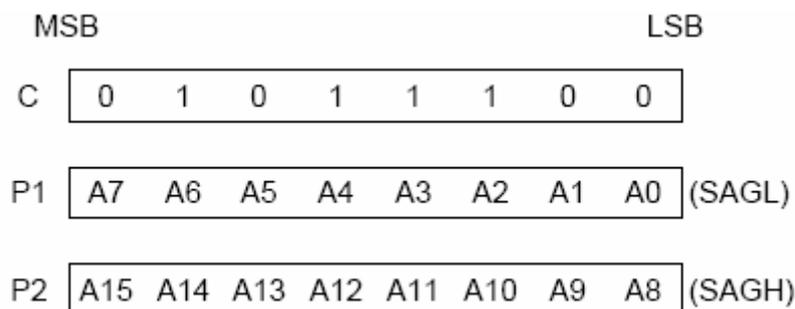


Figure 19. CGRAM ADR parameters

Note

See section 10 for information on the SAG parameters.

HDOT SCR

While the SCROLL command only allows scrolling by characters, HDOT SCR allows the screen to be scrolled horizontally by pixels. HDOT SCR cannot be used on individual layers.

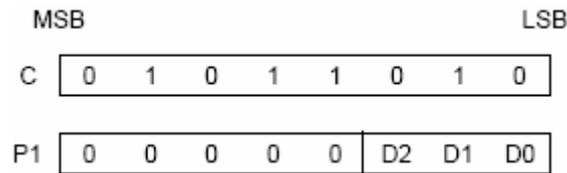


Figure 20. HDOT SCR parameters

(1) D0 to D2

Specifies the number of pixels to scroll. The C/R parameter has to be set to one more than the number of horizontal characters before using HDOT SCR. Smooth scrolling can be simulated if the controlling microprocessor repeatedly issues the HDOT SCR command to the RA8835 series. See Section 9.5 for more information on scrolling the display.

2.2.4 Drawing Control Commands
CSRW

The 16-bit cursor address register contains the display memory address of the data at the cursor position as shown in Figure 22. Note that the microprocessor cannot directly access the display memory. The MREAD and MWRITE commands use the address in this register.

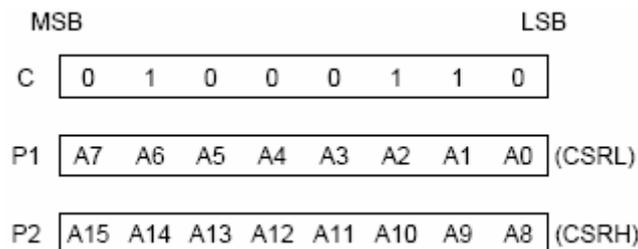


Figure 22. CSRW parameters

The cursor address register can only be modified by the CSRW command, and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.

CSRR

Reads from the cursor address register. After issuing the command, the data read address is read twice, for the low byte and then the high byte of the register.

If a new address is not set, display memory accesses will be from the last set address or the address after previous automatic increments.

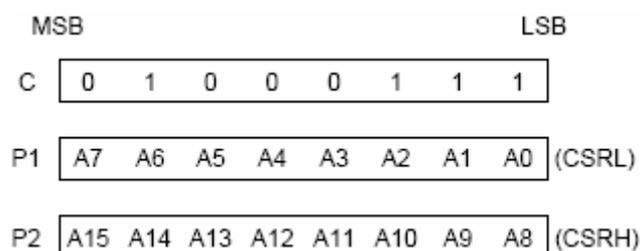


Figure 23. CSRR parameters

2.2.5. Memory Control Commands

MWRITE

The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the RA8835 series. There is no need for further MWRITE commands or for the microprocessor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR, in preparation for the next data write.

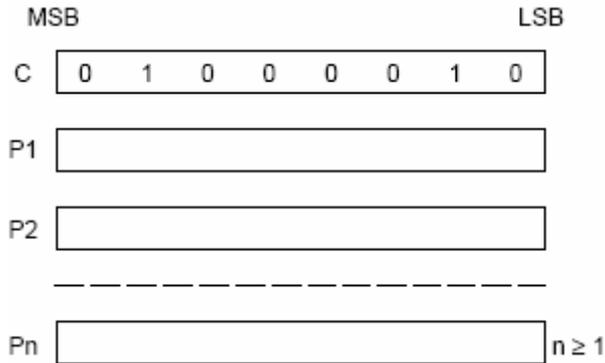


Figure 24. MWRITE parameters

Note:

P1, P2, ..., Pn: display data.

MREAD

Puts the RA8835 series into the data output state. Each time the microprocessor reads the buffer, the cursor address is incremented by the amount set by CSRDIR and the next data byte fetched from memory, so a sequence of data bytes may be read without further MREAD commands or by updating the cursor address register. If the cursor is displayed, the read data will be from two positions ahead of the cursor.

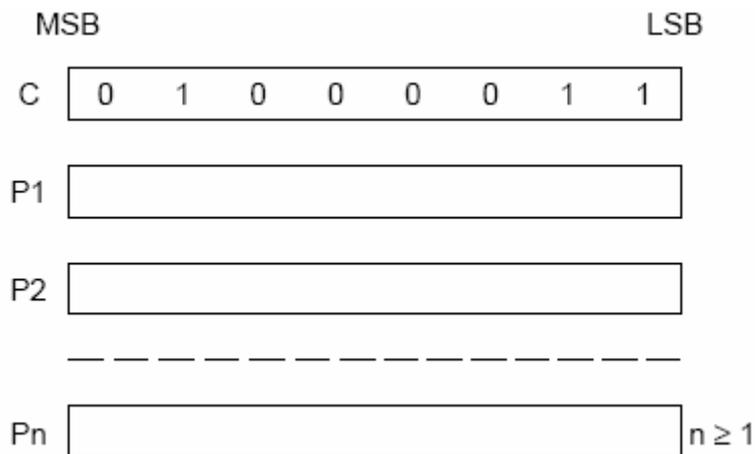


Figure 25. MREAD parameters

2.3. DISPLAY CONTROL FUNCTIONS

2.3.1. Character Configuration

The origin of each character bitmap is in the top left corner as shown in Figure 29. Adjacent bits in each byte are horizontally adjacent in the corresponding character image.

Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

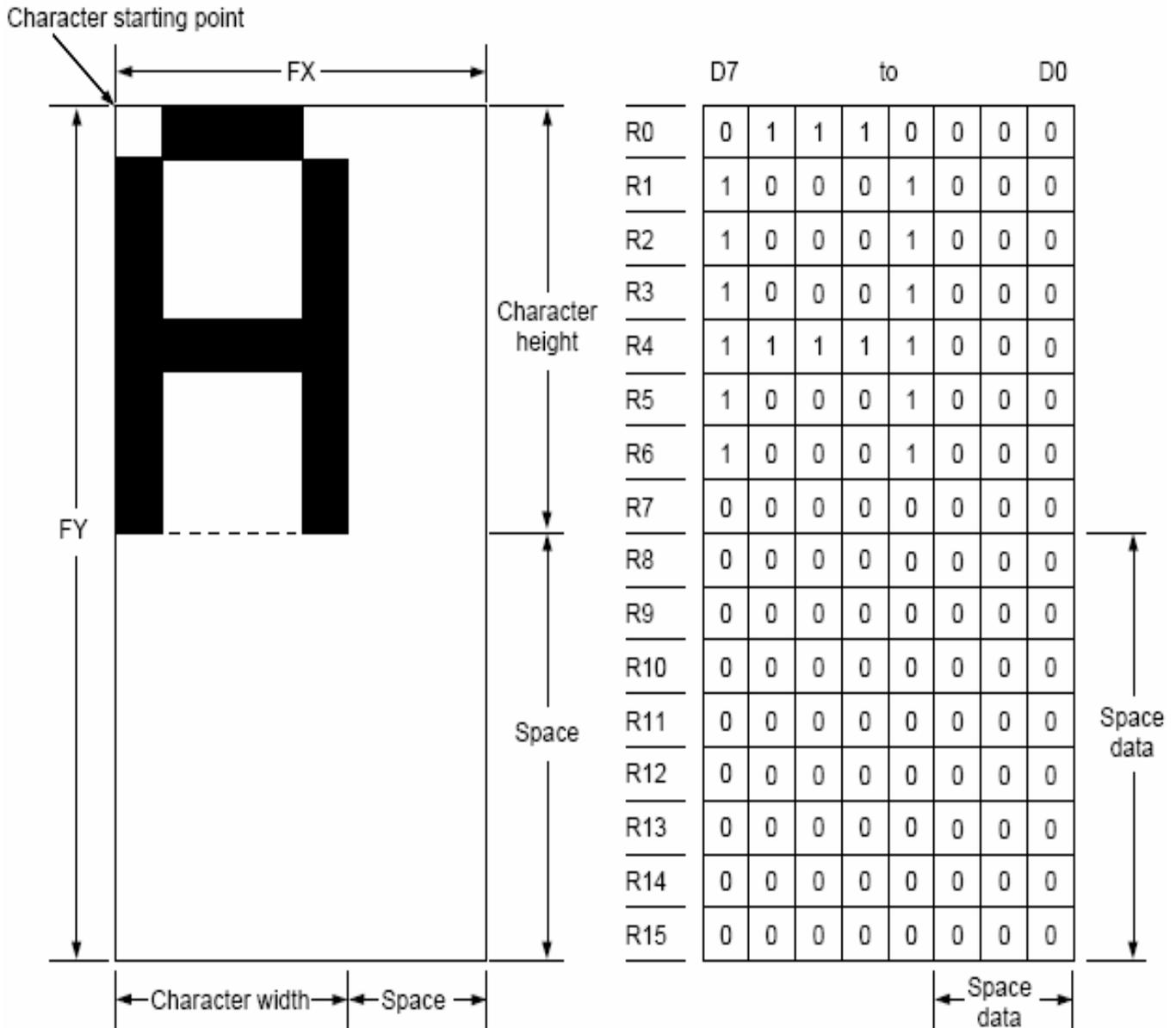


Figure 26. Example of character display ($[FX] \cong 8$) and generator bitmap

If the area outside the character bitmap contains only zeros, the displayed character size can easily be increased by increasing FX and FY, as the zeros ensure that the extra space between displayed characters is blank.

The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

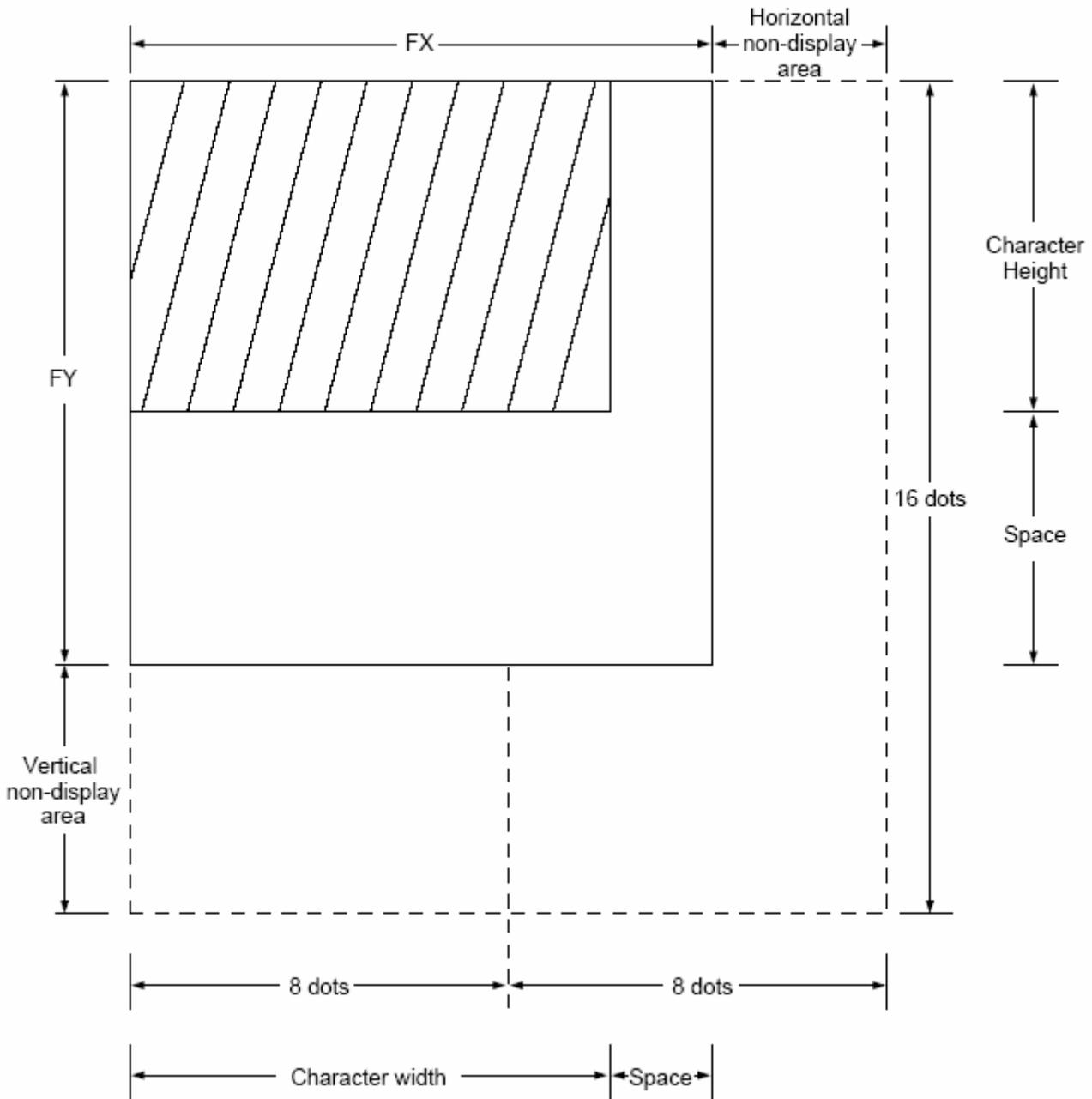


Figure 27. Character width greater than one byte wide ([FX] = 9)

Note: The RA8835 series does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

2.3.2. Screen Configuration

Screen configuration

The basic screen configuration of the RA8835 series is as a single text screen or as overlapping text and graphics screens. The graphics screen uses eight times as much display memory as the text screen.

Figure 28 shows the relationship between the virtual screens and the physical screen.

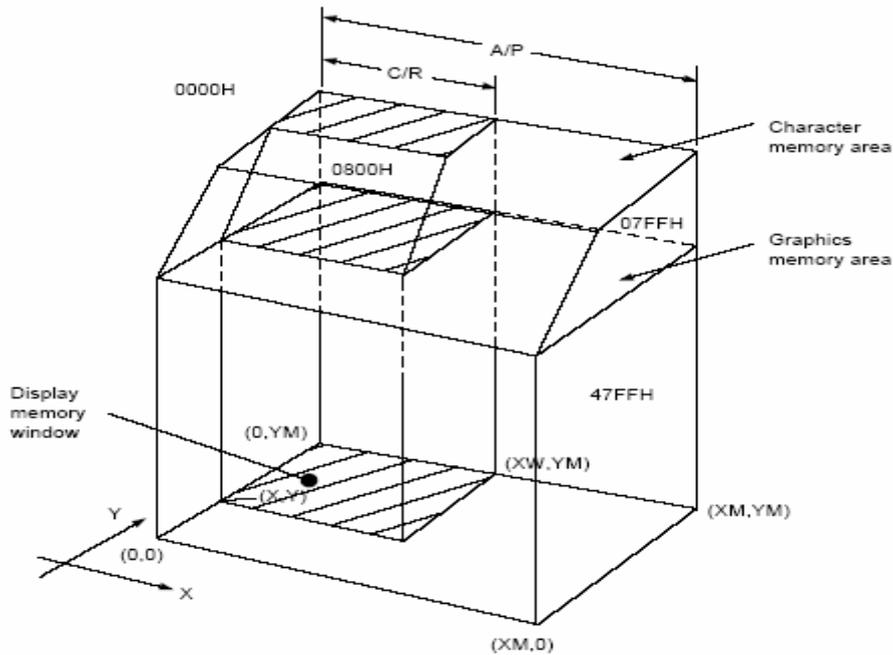


Figure 28. Virtual and physical screen relationship

Display address scanning

The RA8835 series scans the display memory in the same way as a raster scan CRT screen. Each row is scanned from left to right until the address range equals C/R. Rows are scanned from top to bottom. In graphics mode, at the start of each line, the address counter is set to the address at the start of the previous line plus the address pitch, AP.

In text mode, the address counter is set to the same start address, and the same character data is read, for each row in the character bitmap. However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed, the address counter is set to the start address plus AP and the next line of text is displayed.

1	SAD	SAD + 1	SAD + 2		SAD + C/R
8					
9	SAD + AP	SAD + AP + 1	SAD + AP + 2		SAD + AP + C/R
16					
17	SAD + 2AP				
24					
...					
...					
...					
	C/R				
	W/S = 0, FX = 8, FY = 8				

Figure 29. Character position parameters

Note: One byte of display memory corresponds to one character.

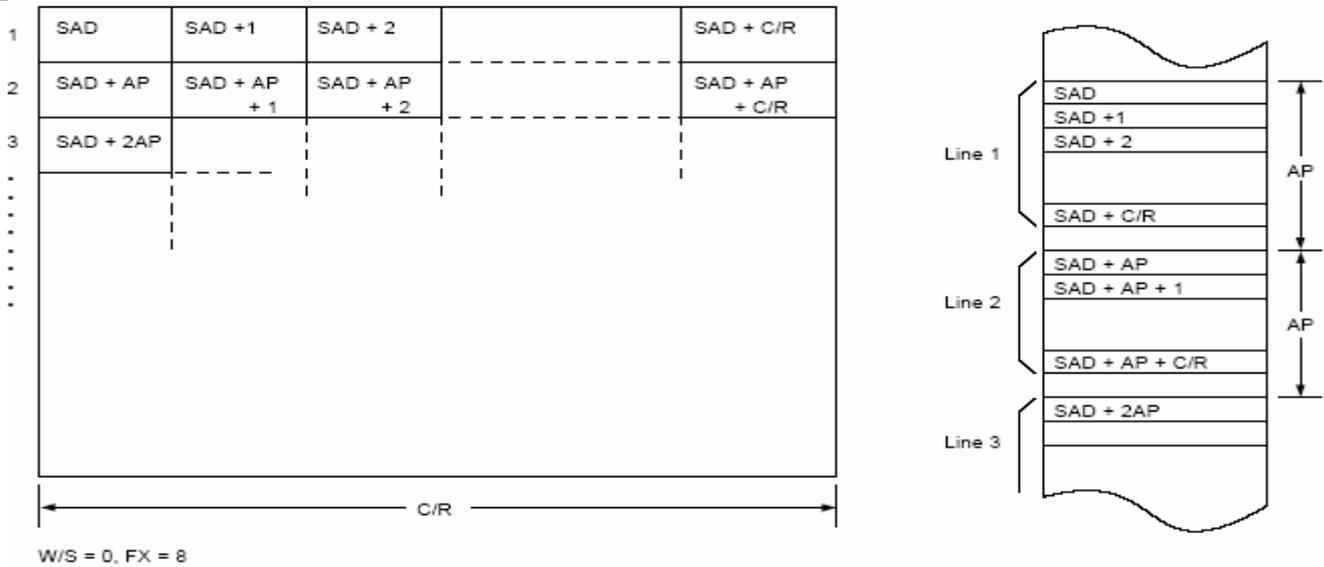


Figure 30. Character parameters vs. memory

Note: One bit of display memory corresponds to one pixel.

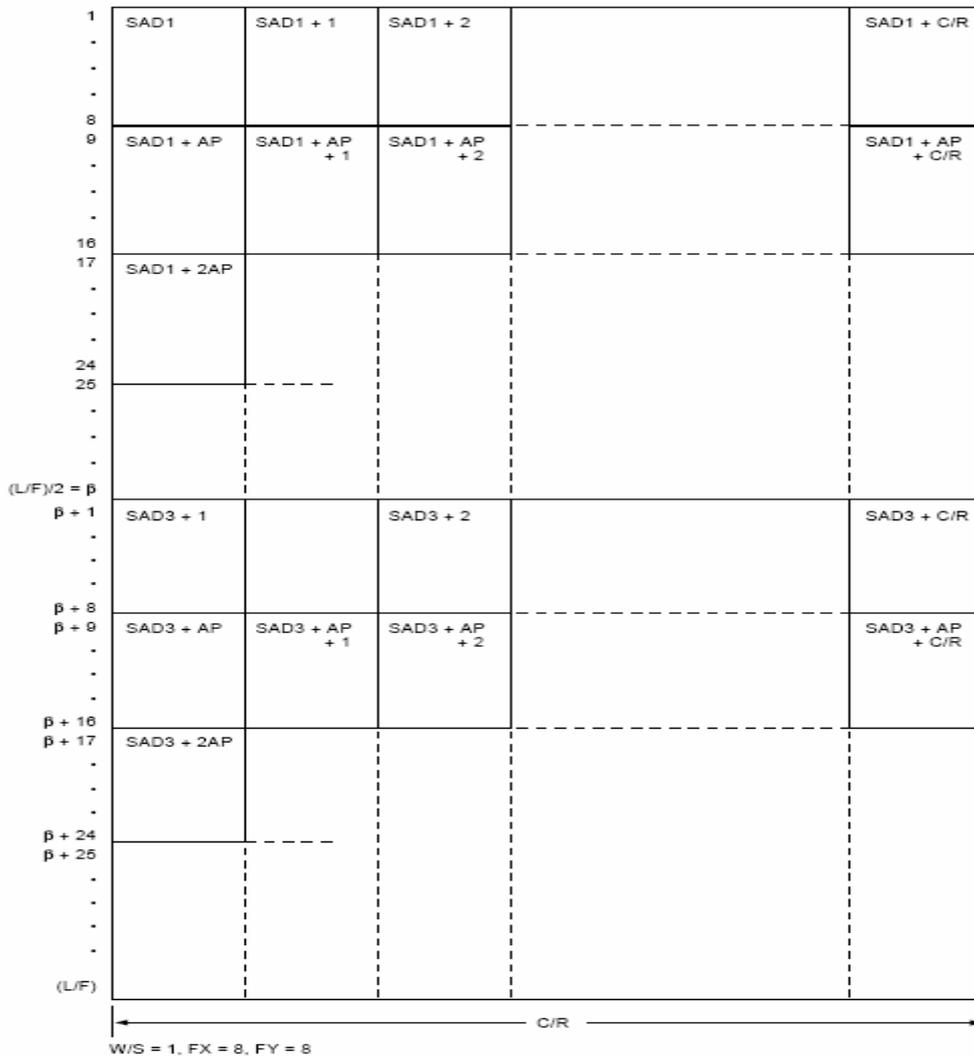


Figure 31. Two-panel display address indexing

Note In two-panel drive, the RA8835 series reads line 1 and line β + 1 as one cycle. The upper and lower panels are thus read alternately, one line at a time.

Display scan timing

Figure 32 shows the basic timing of the RA8835 series. One display memory read cycle takes nine periods of the system clock, f_0 (f_{OSC}). This cycle repeats $(C/R + 1)$ times per display line. When reading, the display memory pauses at the end of each line for $(TC/R - C/R)$ display memory read cycles, though the LCD drive signals are still generated. TC/R may be set to any value within the constraints imposed by C/R , f_{OSC} , f_{FR} , and the size of the LCD panel, and it may be used to fine tune the frame frequency. The microprocessor may also use this pause to access the display memory data.

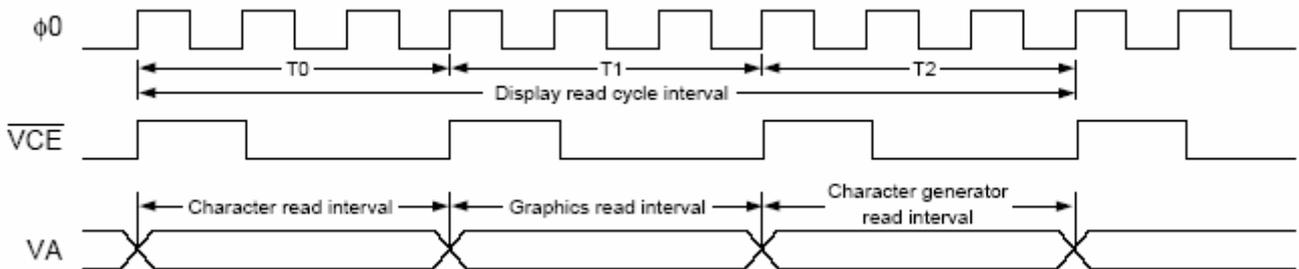


Figure 32. Display memory basic read cycle

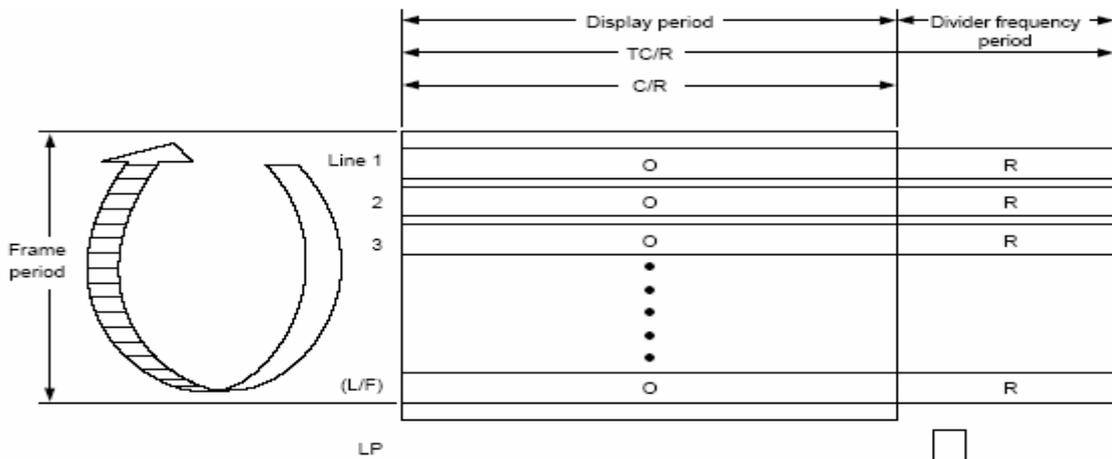


Figure 33. Relationship between TC/R and C/R

Note: The divider adjustment interval (R) applies to both the upper and lower screens even if $W/S = 1$. In this case, LP is active only at the end of the lower screen's display interval.

2.3.3. Cursor Control

Cursor register function

The RA8835 series cursor address register functions as both the displayed cursor position address register and the display memory access address register. When accessing display memory outside the actual screen memory, the address register must be saved before accessing the memory and restored after memory access is complete.

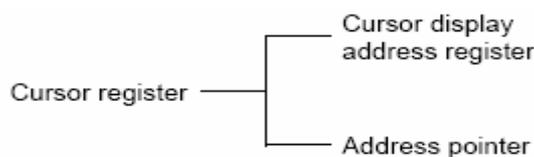


Figure 34. Cursor addressing

Note that the cursor may disappear from the display if the cursor address remains outside the displayed

screen memory for more than a few hundred milliseconds.

Cursor movement

On each memory access, the cursor address register changes by the amount previously specified with CSRDIR, automatically moving the cursor to the desired location.

Cursor display layers

Although the RA8835 series can display up to three layers, the cursor is displayed in only one of these layers: Two-layer configuration: First layer (L1) Three-layer configuration: Third layer (L3) The cursor will not be displayed if it is moved outside the memory for its layer. Layers may be swapped or the cursor layer moved within the display memory if it is necessary to display the cursor on a layer other than the present cursor layer.

Although the cursor is normally displayed for character data, the RA8835 series may also display a dummy cursor for graphical characters. This is only possible if the graphics screen is displayed, the text screen is turned off and the microprocessor generates the cursor control address.

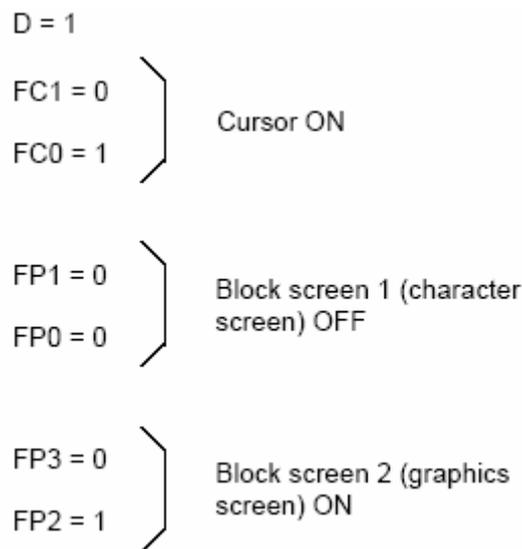


Figure 35. Cursor display layers

Consider the example of displaying Chinese characters on a graphics screen. To write the display data, the cursor address is set to the second screen block, but the cursor is not displayed. To display the cursor, the cursor address is set to an address within the blank text screen block.

Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the cursor address register when moving the cursor over the graphical characters.

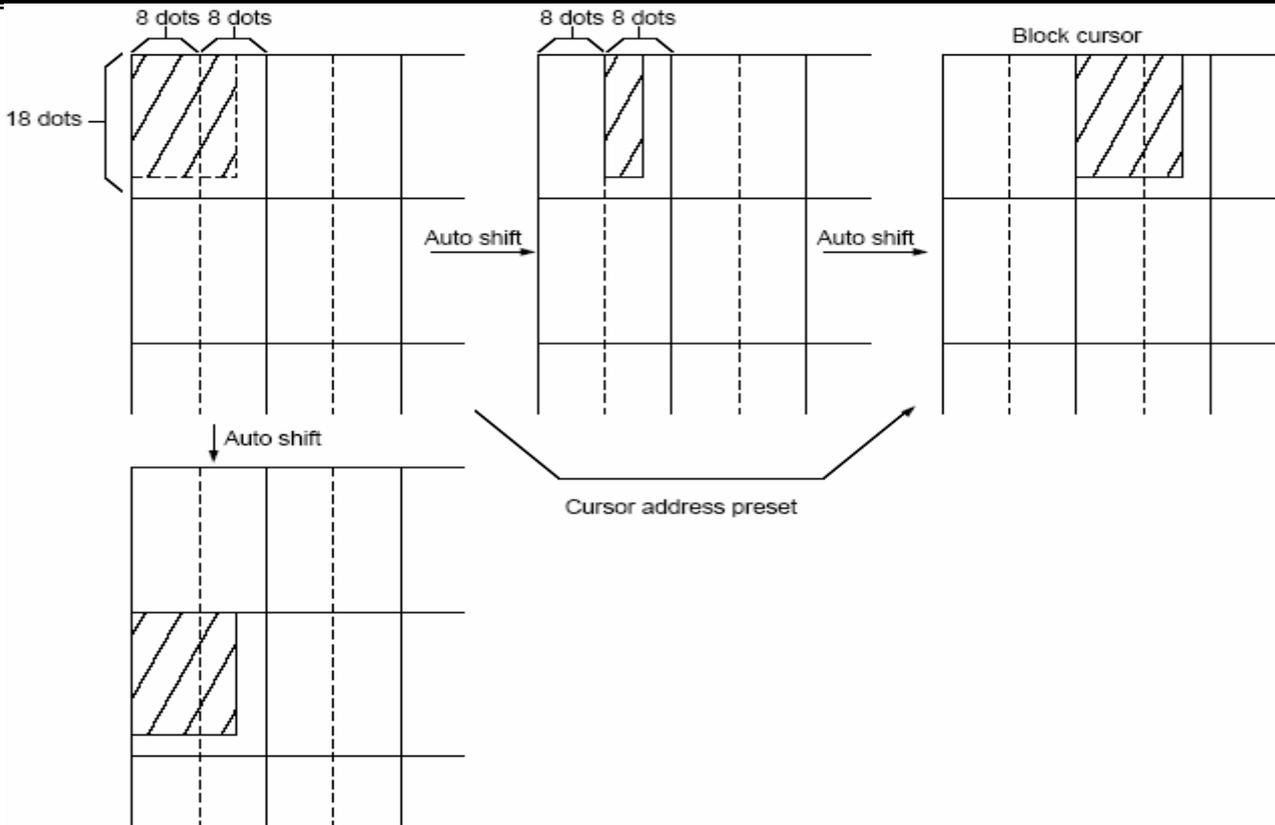
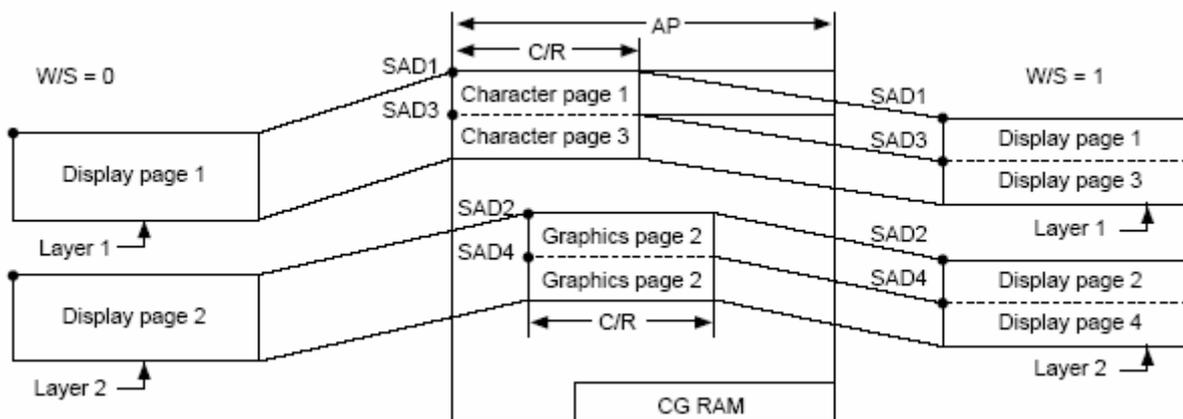


Figure 36. Cursor movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address. If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the RA8835 series automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphics screen, a bar cursor.

2.3.4 Memory to Display Relationship

The RA8835 series supports virtual screens that are larger than the physical size of the LCD panel address range, C/R. A layer of the RA8835 series can be considered as a window in the larger virtual screen held in display memory. This window can be divided into two blocks, with each block able to display a different portion of the virtual screen. This enables, for example, one block to dynamically scroll through a data area while the other acts as a status message display area. See Figure 37 and 38.



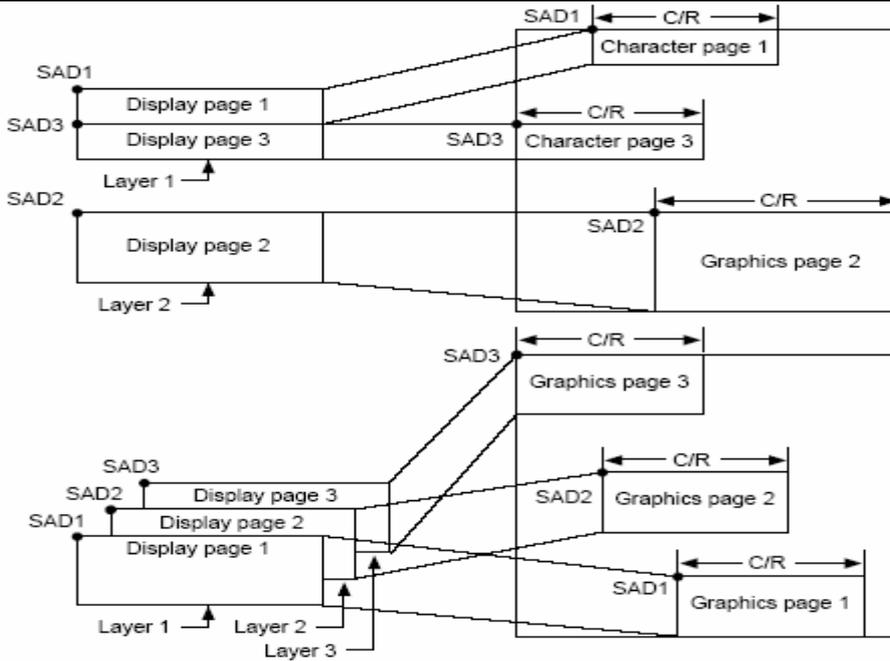


Figure 37. Display layers and memory

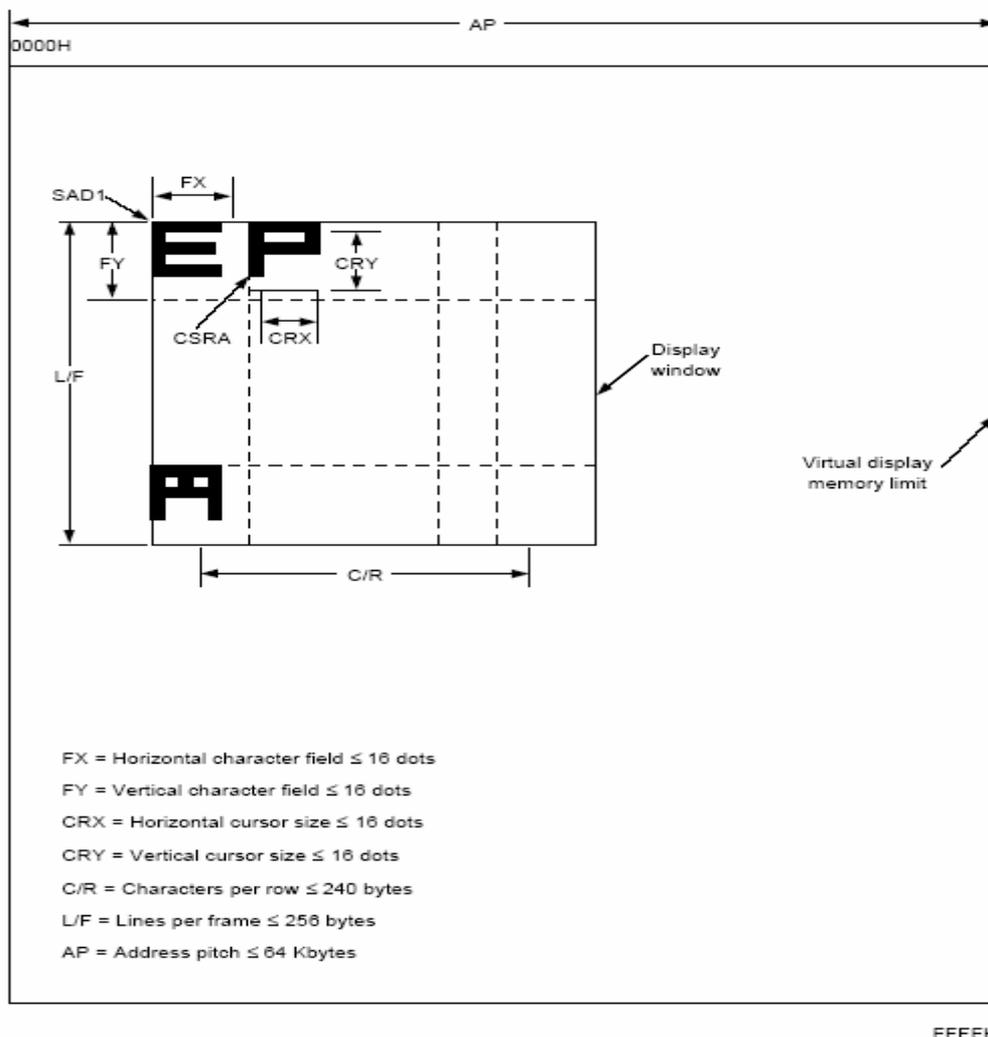


Figure 38. Display window and memory

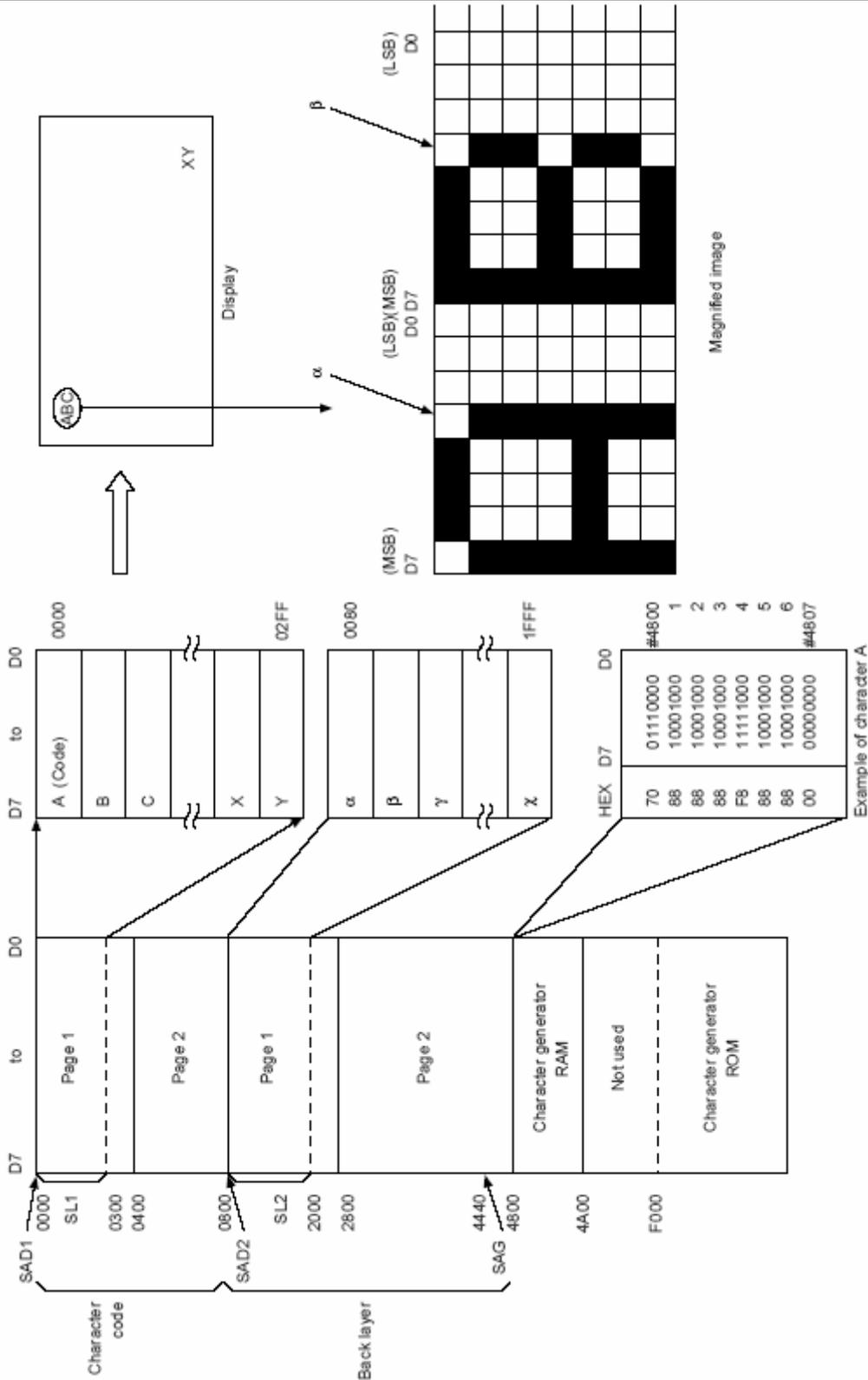


Figure 39. Memory map and magnified characters

2.3.5. Scrolling

The controlling microprocessor can set the RA8835 series scrolling modes by overwriting the scroll address registers SAD1 to SAD4, and by directly setting the scrolling mode and scrolling rate.

On-page scrolling

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line. Since the RA8835 series does not automatically erase the bottom line, it must be erased with blanking data when changing the scroll address register.

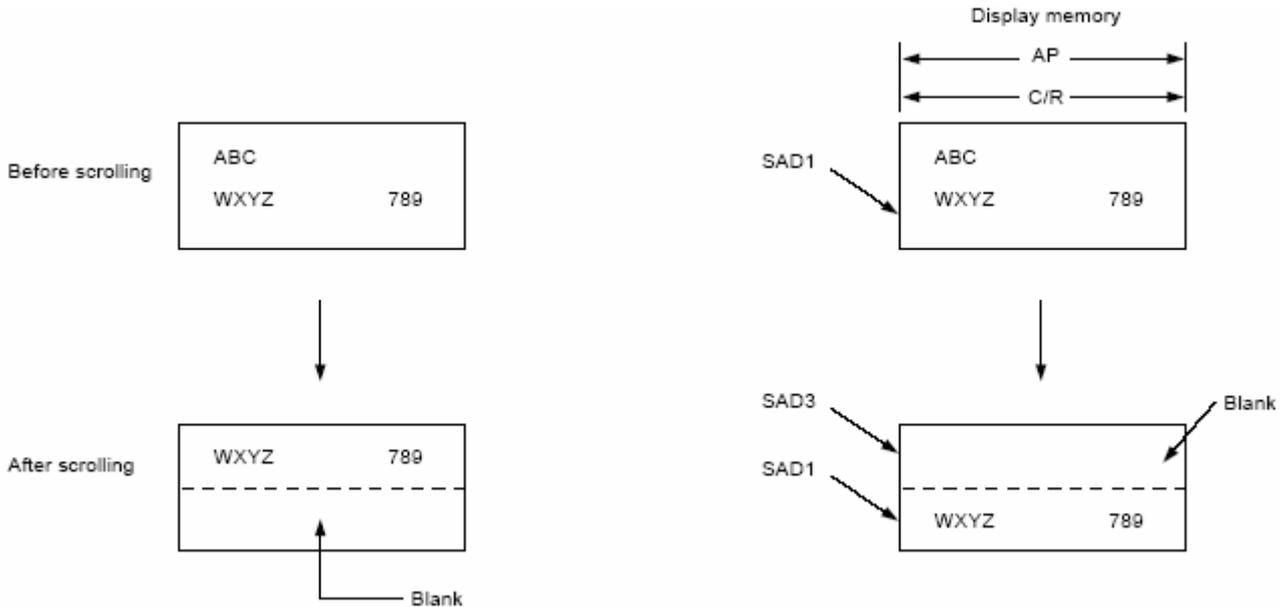


Figure 40. On-page scrolling

Inter-page scrolling

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen.

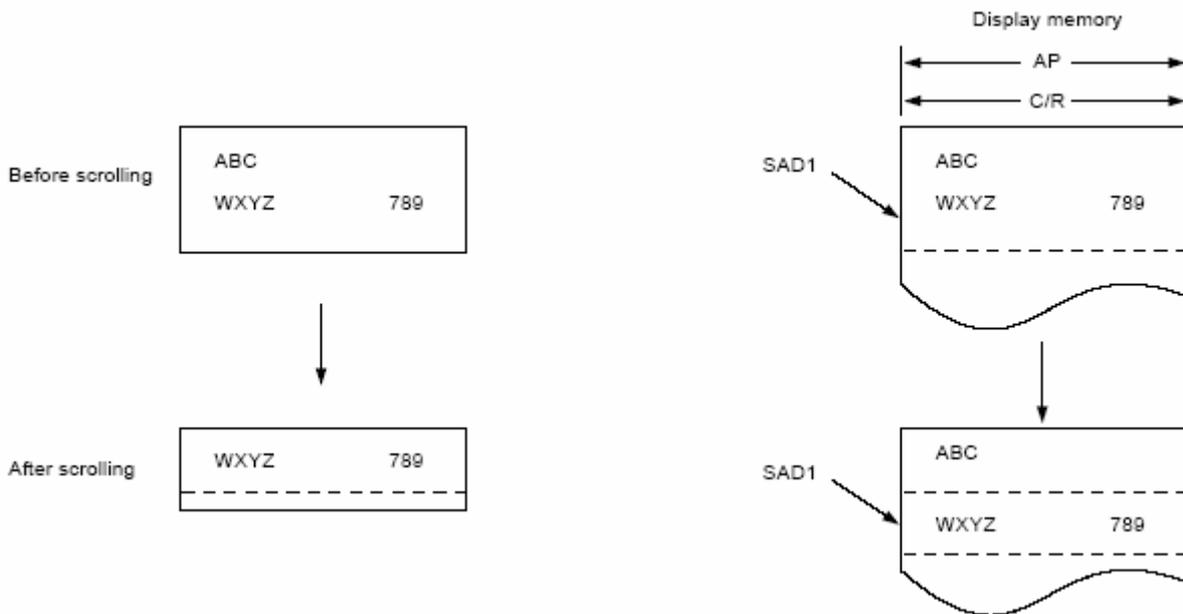


Figure 41. Inter-page scrolling

Horizontal scrolling

The display can be scrolled horizontally in one-character units, regardless of the display memory capacity.

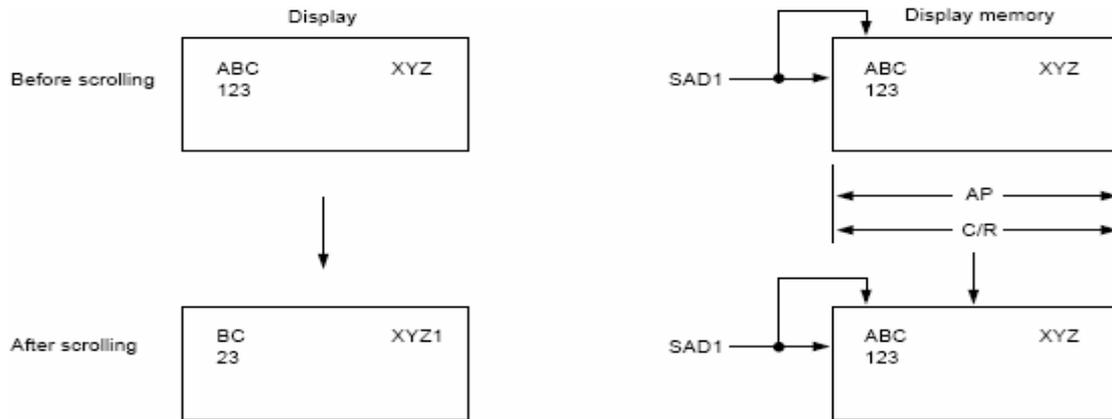


Figure 42. Horizontal wraparound scrolling

Bi-directional scrolling

Bi-directional scrolling can be performed only if the display memory is larger than the physical screen both horizontally and vertically. Although scrolling is normally done in single-character units, the HDOT SCR command can be used to scroll horizontally in pixel units. Single-pixel scrolling both horizontally and vertically can be performed by using the SCROLL and HDOT SCR commands. See Section 16.4

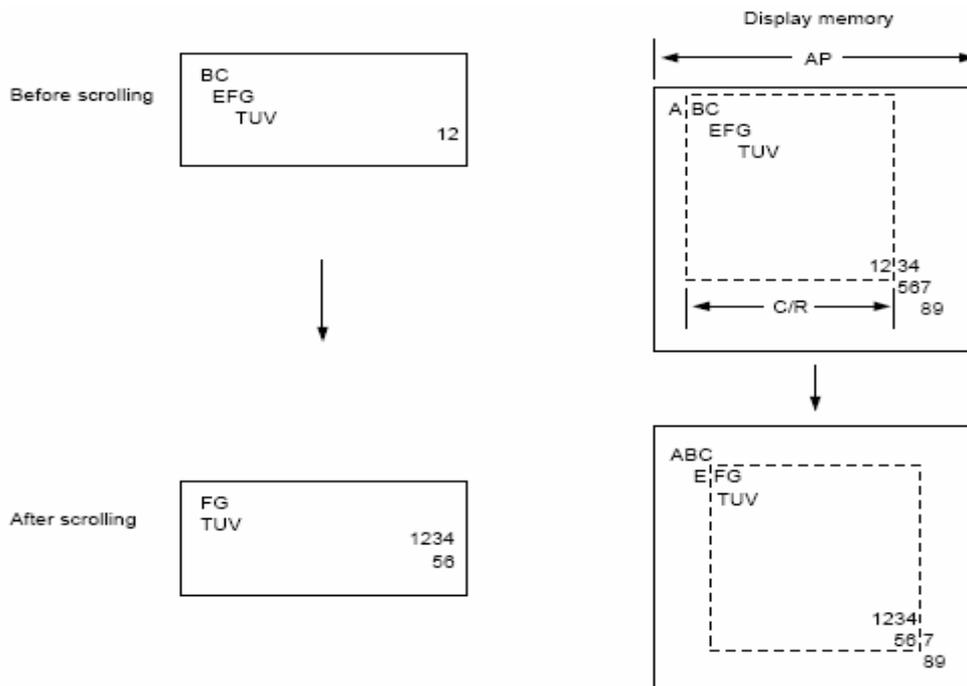


Figure 43. Bidirectional scrolling

Scroll units

Tale 19. Scroll units

Mode	Vertical	Horizontal
Text	Characters	Pixels or characters
Graphics	Pixels	Pixels

Note that in a divided screen, each block cannot be independently scrolled horizontally in pixel units.

2.4. CHARACTER GENERATOR

2.4.1 CG Characteristics

Internal character generator

The internal character generator is recommended for minimum system configurations containing a RA8835 series, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- 5X7-pixel font (See Section 17.)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CG RAM characters)
- Can be automatically spaced out up to 8 X16 pixels

External character generator ROM

The external CG ROM can be used when fonts other than those in the internal ROM are needed. Data is stored in the external ROM in the same format used in the internal ROM. (See Section 10.3.)

- Up to 8X8-pixel characters (M2 = 0) or 8X16-pixel characters (M2 = 1)
- Up to 256 characters (192 if used together with the internal ROM)
- Mapped into the display memory address space at F000H to F7FFH (M2 = 0) or F000H to FFFFH (M2 = 1)
- Characters can be up to 8X16-pixels; however, excess bits must be set to zero.

Character generator RAM

The user can freely use the character generator RAM for storing graphics characters. The character generator RAM can be mapped by the microprocessor anywhere in display memory, allowing effective use of unused address space.

- Up to 8X8-pixel characters (M2 = 0) or 8X16 characters (M2 = 1)
- Up to 256 characters if mapped at F000H to FFFFH (64 if used together with character generator ROM)
- Can be mapped anywhere in display memory address space if used with the character generator ROM
- Mapped into the display memory address space at F000H to F7FFH if not used with the character generator ROM (more than 64 characters are in the CG RAM). Set SAG0 to F000H and M1 to zero when defining characters number 193 upwards.

2.4.2 CG Memory Allocation

Since the RA8835 series uses 8-bit character codes, it can handle no more than 256 characters at a time. However, if a wider range of characters is required, character generator memory can be bank-switched using the CGRAM ADR command.

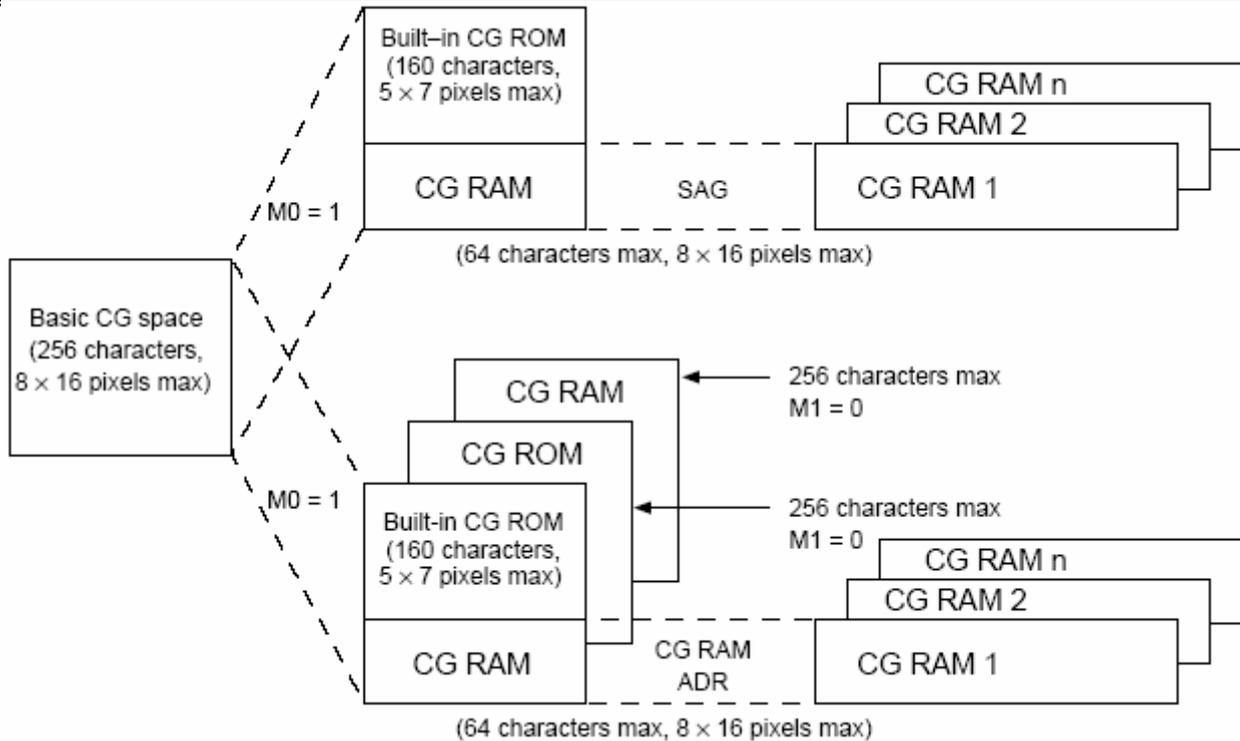


Figure 44. Internal and external character mapping

Note that there can be no more than 64 characters per bank.

Table 20. Character mapping

Item	Parameter	Remarks
Internal/external character generator selection	M0	
Character field height	1 to 8 pixels	M2 = 0
	9 to 16 pixels	M2 = 1
	Greater than 16 pixels	Graphics mode (8 bits × 1 line)
Internal CG ROM/RAM select External CG ROM/RAM select	Automatic	Determined by the character code
CG RAM bit 6 correction	M1	
CG RAM data storage address	Specified with CG RAM ADR command	Can be moved anywhere in the display memory address space
External CG ROM address	192 characters or less	Other than the area of Figure 49
	More than 192 characters	Set SAG to F000H and overly SAG and the CG ROM table

2.4.3 Setting the Character Generator Address

The CG RAM addresses in the VRAM address space are not mapped directly from the address in the SAG register. The data to be displayed is at a CG RAM address calculated from SAG + character code + ROW select address. This mapping is shown in Table 21 and 22.

Table 21. Character fonts, number of lines ≤ 8 (M2 = 0, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Table 22. Character fonts, 9 £ number of lines £ 16 (M2 = 1, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

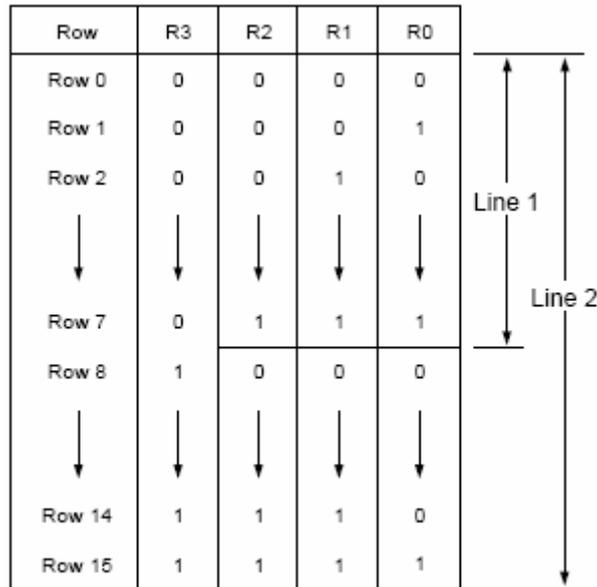


Figure 45. Row select address

Note:

Lines = 1: lines in the character bitmap ≤ 8

Lines = 2: lines in the character bitmap ≥ 9

M1 = 1

The RA8835 series automatically converts all bits set in bit 6 of character code for CG RAM 2 to zero. Because of this, the CG RAM data areas become contiguous in display memory.

When writing data to CG RAM:

- Calculate the address as for M1 = 0.
- Change bit 6 of the character code from “1” to “0”.

CG RAM addressing example

- Define a pattern for the “A” in Figure 26.
- The CG RAM table start address is 4800H.
- The character code for the defined pattern is 80H (the first character code in the CG RAM area). As the character code table in Figure 46 shows, codes 80H to 9FH and E0H to FFH are allocated to the CG RAM and can be used as desired. 80H is thus the first code for CG RAM. As characters cannot be used if only using graphics mode, there is no need to set the CG RAM data.

Table 23. Character data example

CGRAM AD	5CH	Reverse the CG RAM address calculation to calculate SAG
P1	00H	
P2	40H	
CSRDIR	4CH	Set cursor shift direction to right

Table 23. Character data example (continued)

CSRW	46H	CG RAM start address is 4800H
P1	00H	
P2	48H	
MWRITE	42H	
P	70H	Write ROW 0 data
P2	88H	Write ROW 1 data
P3	88H	Write ROW 2 data
P4	88H	Write ROW 3 data
P5	F8H	Write ROW 4 data
P6	88H	Write ROW 5 data
P7	88H	Write ROW 6 data
P8	00H	Write ROW 7 data
P8	00H	Write ROW 8 data
↓	↓	↓
P16	00H	Write ROW 15 data

2.4.4 Character Codes

The following figure shows the character codes and the codes allocated to CG RAM. All codes can be used by the CG RAM if not using the internal ROM.

Lower 4 bits	Upper 4 bits															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0				0	@	P	'	p								
1			!	1	A	Q	a	q								
2			"	2	B	R	b	r								
3			#	3	C	S	c	s								
4			\$	4	D	T	d	t								
5			%	5	E	U	e	u								
6			&	6	F	V	f	v								
7			'	7	G	W	g	w								
8			(8	H	X	h	x								
9)	9	I	Y	i	y								
A			*	:	J	Z	j	z								
B			+	;	K	[k	{								
C			,	<	L	¥	l	;								
D			.	=	M]	m	}								
E			-	>	N	^	n	→								
F			/	?	O	_	o	←								

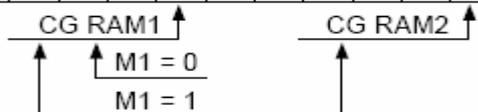


Figure 46. On-chip character codes

2.5 MICROPROCESSOR INTERFACE

2.5.1. System Bus Interface

SEL1, SEL2, A0, RD, WR and CS are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. SEL1 and SEL2 change the operation of the RD and WR pins to enable interfacing to either an 8080 or 6800 family bus, and should have a pull-up or pull-down resistor. With microprocessors using an 8080 family interface, the RA8835 series is normally mapped into the I/O address space.

8080 series

Table 24. 8080 series interface signals

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Function
0	0	1	Status flag read
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

6800 series

Table 25. 6800 series interface signals

A0	R/W	E	Function
0	1	1	Status flag read
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

2.5.2. Microprocessor Synchronization

The RA8835 series interface operates at full bus speed, completing the execution of each command within the cycle time, tCYC. The controlling microprocessor's performance is thus not hampered by polling or handshaking when accessing the RA8835 series. Display flicker may occur if there is more than one consecutive access that cannot be ignored within a frame. The microprocessor can minimize this either by performing these accesses intermittently, or by continuously checking the status flag (D6) and waiting for it to become HIGH.

Display status indication output

When CS, A0 and RD are LOW, D6 functions as the display status indication output. It is HIGH during the TV-mode vertical retrace period or the LCD-mode horizontal retrace period, and LOW, during the period the controller is writing to the display. By monitoring D6 and writing to the data memory only during retrace periods, the display can be updated without causing screen flicker.

Internal register access

The SYSTEM SET and SLEEP IN commands can be used to perform input/output to the RA8835 series independently of the system clock frequency. These are the only commands that can be used while the RA8835 series is in sleep mode.

Display memory access

The RA8835 series supports a form of pipelined processing, in which the microprocessor synchronizes its

processing to the RA8835 series timing. When writing, the microprocessor first issues the MWRITE command. It then repeatedly writes display data to the RA8835 series using the system bus timing. This ensures that the microprocessor is not slowed down even if the display memory access times are slower than the system bus access times. See Figure 47. When reading, the microprocessor first issues the MREAD command, which causes the RA8835 series to load the first read data into its output buffer. The microprocessor then reads data from the RA8835 series using the system bus timing. With each read, the RA8835 series reads the next data item from the display memory ready for the next read access. See Figure 48.

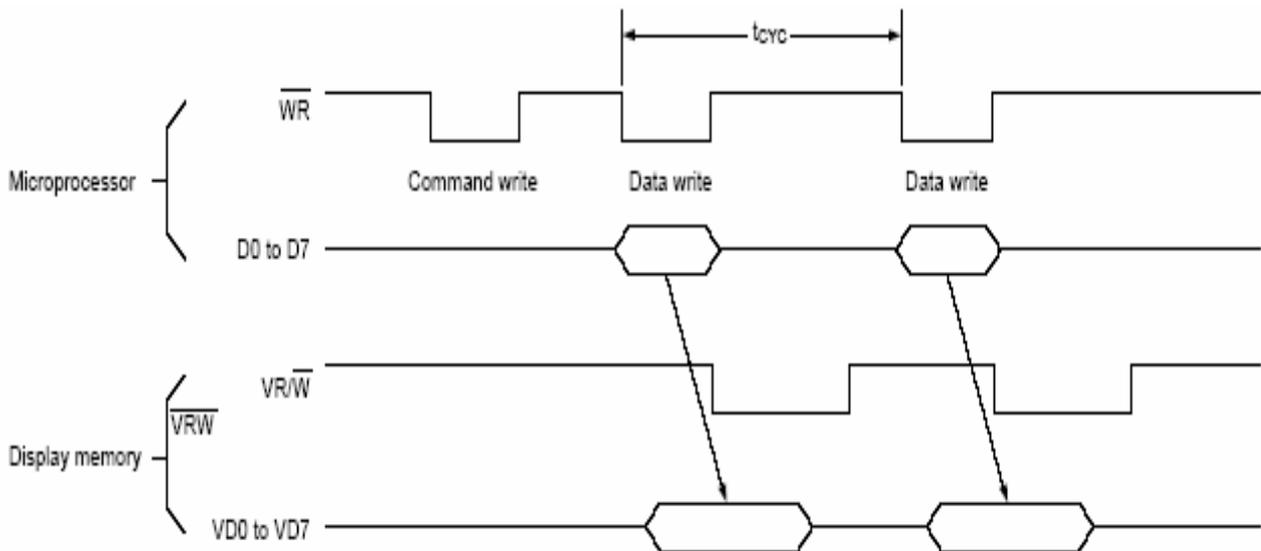


Figure 47. Display memory write cycle

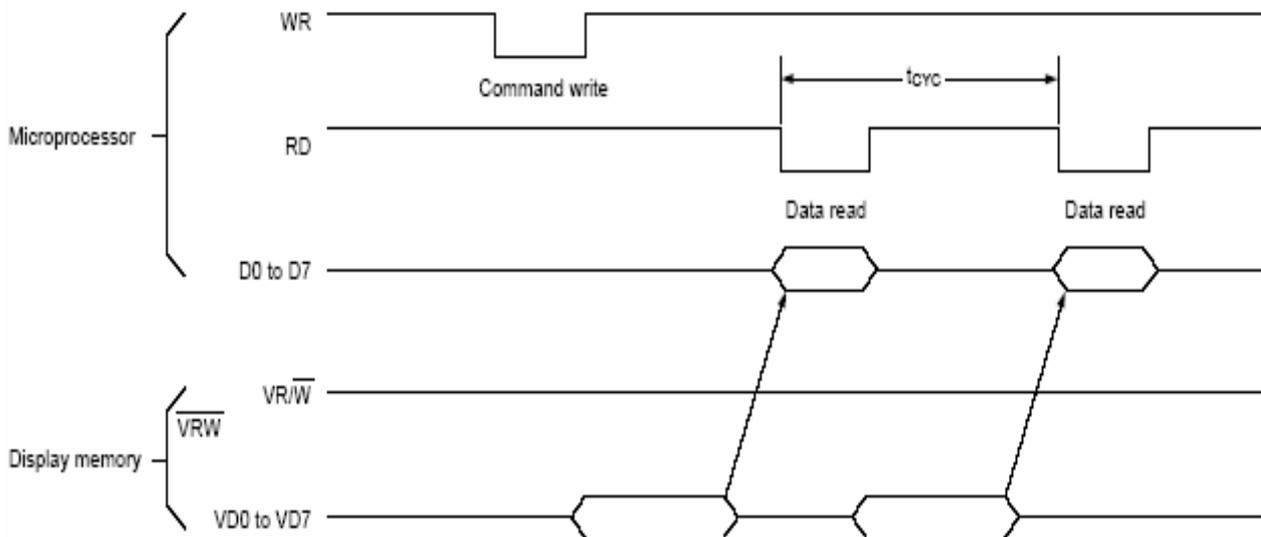


Figure 48. Display memory read cycle

Note

A possible problem with the display memory read cycle is that the system bus access time, t_{ACC} , does not depend on the display memory access time, t_{ACV} . The microprocessor may only make repeated reads if the read loop time exceeds the RA8835 series cycle time, t_{CYC} . If it does not, NOP instructions may be inserted in the program loop. t_{ACC} , t_{ACV} and t_{CYC} limits are given in section 6.2.

2.5.3 Interface Examples

Z80 to RA8835 series interface

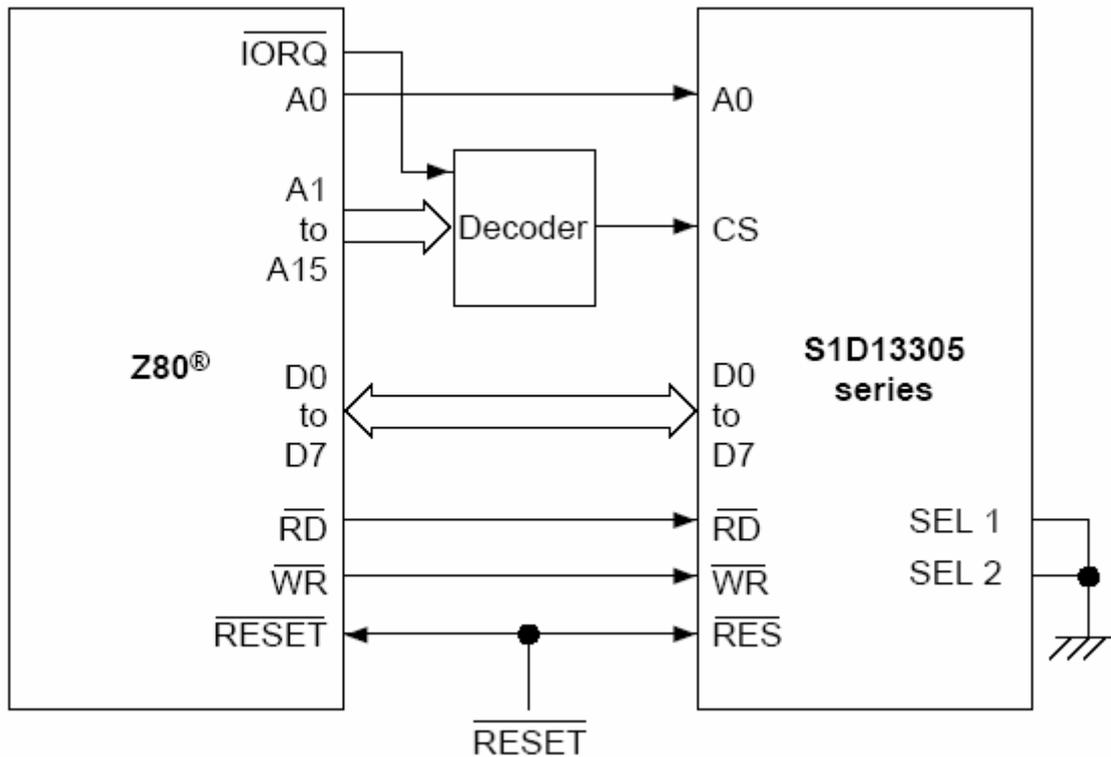


Figure 49. Z80® to RA8835 series interface

Note: Z80® is a registered trademark of Zilog Corporation.

6802 to RA8835 series interface

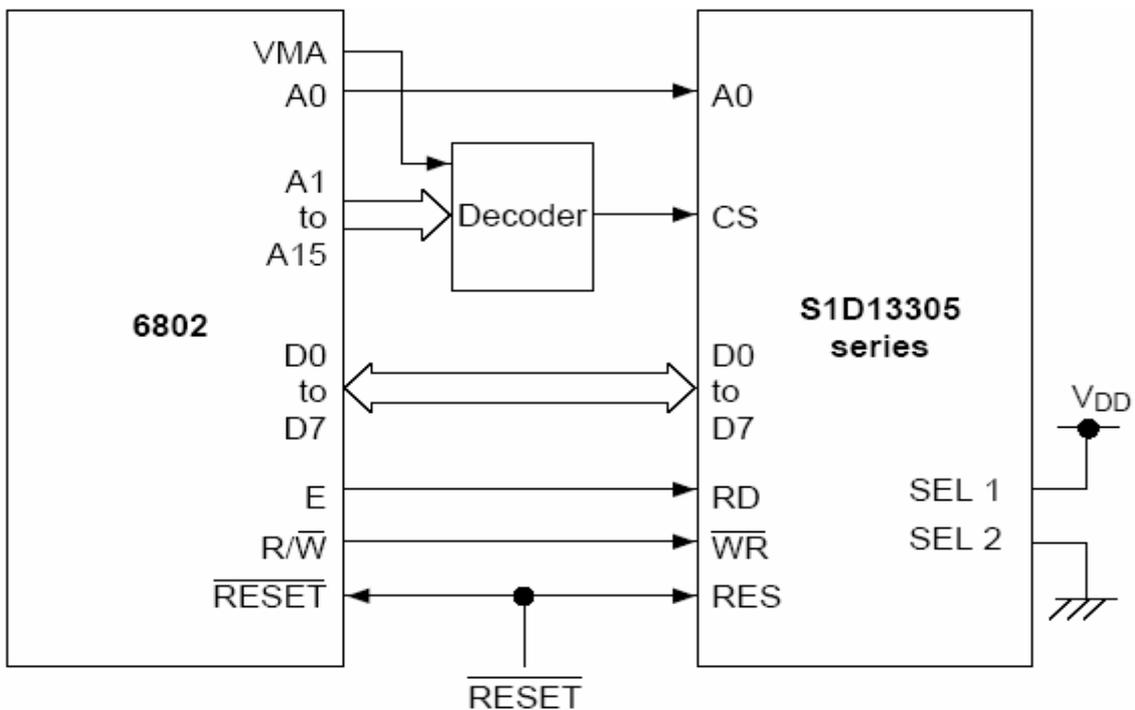


Figure 50. 6802 to RA8835 series interface

2.6 DISPLAY MEMORY INTERFACE

2.6.1. Static RAM

The figure below shows the interface between an 8KX8 static RAM and the RA8835 series. Note that bus buffers are required if the bus is heavily loaded.

- RA8835F

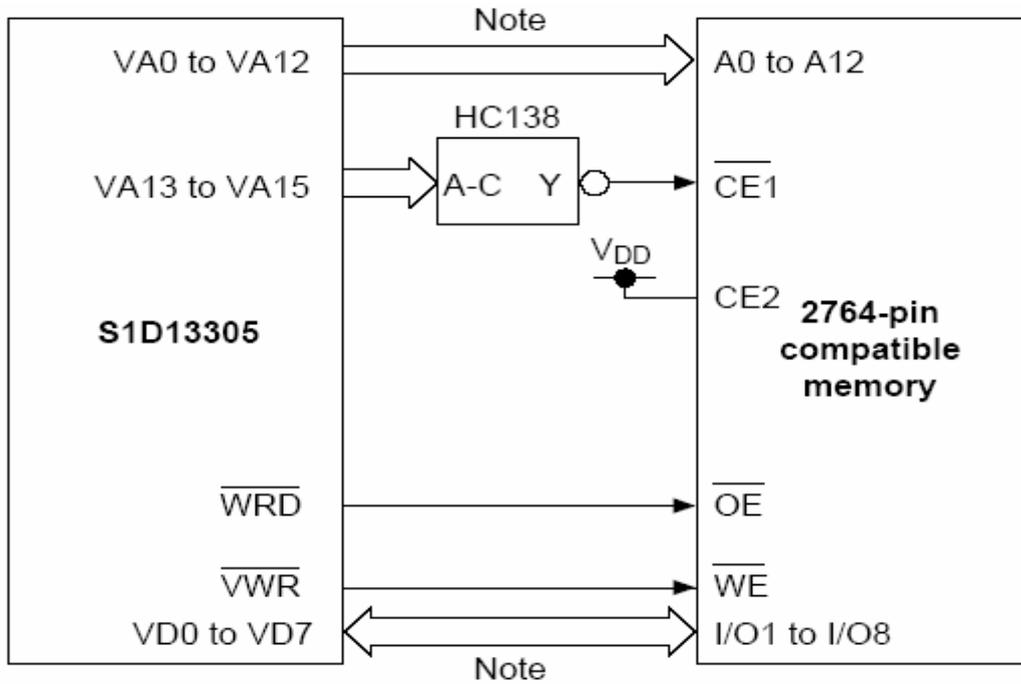


Figure 51. Static RAM interface

Note: If the bus load is too much, use a bus buffer.

2.6.2. Supply Current during Display Memory Access

The 24 address and data lines of the RA8835 series cycle at one-third of the oscillator frequency, f_{OSC} . The charge and discharge current on these pins, I_{VOP} , is given by the equation below. When I_{VOP} exceeds I_{OPR} , it can be estimated by:

$$I_{VOP} \propto V f$$

where C is the capacitance of the display memory bus, V is the operating voltage, and f is the operating frequency.

If $V_{OPR} = 5.0V$, $f = 1.0 \text{ MHz}$, and the display memory bus capacitance is 1.0 pF per line:

$$I_{VOP} \leq 120 \text{ mA} / \text{MHz} \times \text{pF}$$

To reduce current flow during display memory accesses, it is important to use low-power memory, and to minimize both the number of devices and the parasitic capacitance.

2.7. OSCILLATOR CIRCUIT

The RA8835 series incorporates an oscillator circuit. A stable oscillator can be constructed simply by connecting an AT-cut crystal and two capacitors to XG and XD, as shown in the figure below. If the oscillator frequency is increased, CD and CG should be decreased proportionally. Note that the circuit board lines to XG and XD must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption.

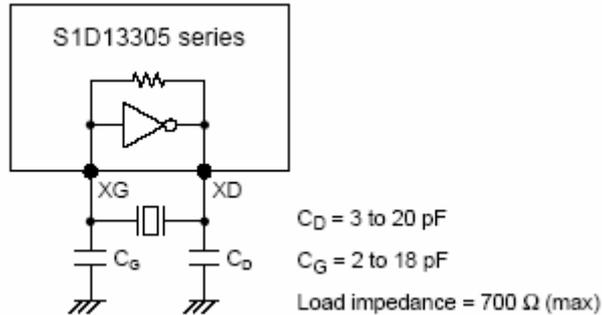


Figure 52. Crystal oscillator

2.8. STATUS FLAG

The RA8835 series has a single bit status flag.

D6: X line standby

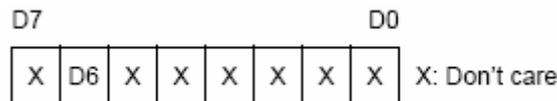


Figure 53. Status flag

The D6 status flag is HIGH for the TC/R-C/R cycles at the end of each line where the RA8835 series is not reading the display memory. The microprocessor may use this period to update display memory without affecting the display, however it is recommended that the display be turned off when refreshing the whole display.

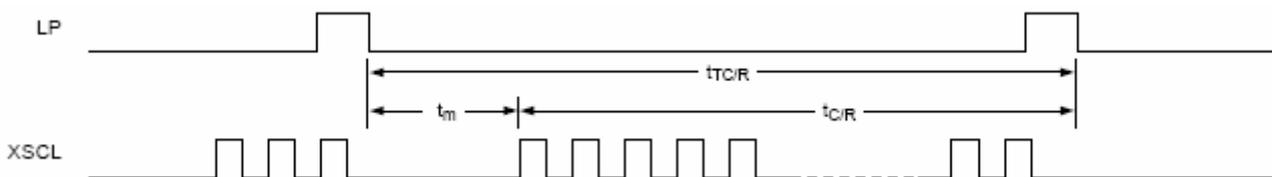


Figure 54. C/R to TC/R time difference

\overline{CS}	A0	\overline{RD}	D6 (flag)
0	0	0	0: Period of retrace lines 1: Period of display

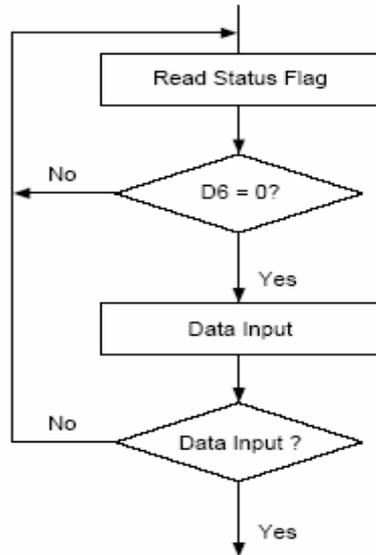
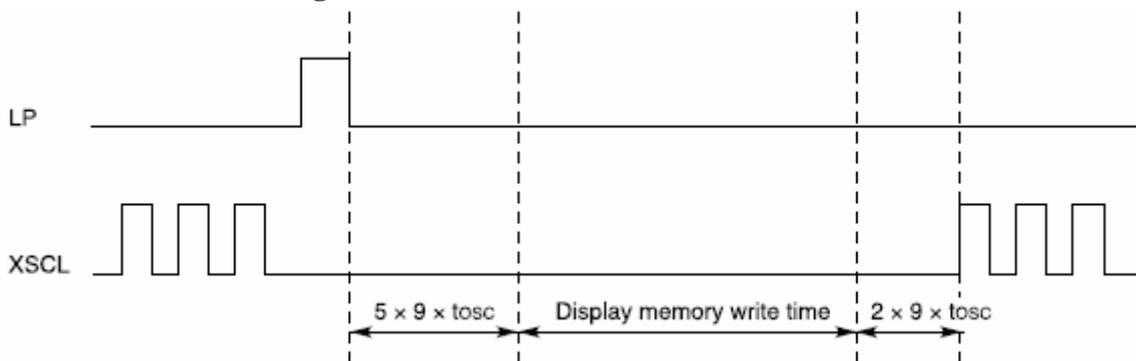


Figure 55. Flowchart for busy flag checking

<Timing To Be Observed For Avoiding S1D 13305 Series Write Noise>

• Precaution on the write timing to VRAM



The allowable writing duration is since “5 X 9 X tosc” has elapsed (to_{sc} = 1/f_{osc}: a cycle of the oscillation frequency) from the positive going edge of LP up to {(TCR) – (C/R) – 7} X 9 X tosc. Currently employed D6 status flag reading method does not identify the timing when the read D6 = Low took place. Thus, negative going edge of LP should be used as the interrupt signal when implementing the writing in above timing. If you try to access the display memory in other timing than the above, flickering of the display screen will result.

2.9 RESET



Figure 56. Reset timing

The RA8835 series requires a reset pulse at least 1 ms long after power-on in order to re-initialize its internal state. For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the RA8835 series is reset. Turn off the LCD power supplies for at least one frame period after the

start of the reset pulse. The RA8835 series cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals XD, LP and FR are halted. A delay of 3 ms (maximum) is required following the rising edges of both RES and VDD to allow for system stabilization.

2.10. APPLICATION NOTES

2.10.1. Initialization Parameters

The parameters for the initialization commands must be determined first. Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example, [FX] = FX + 1.

SYSTEM SET instruction and parameters

(1) FX

The horizontal character field size is determined from the horizontal display size in pixels [VD] and the number of characters per line [VC].

$$[VD] / [VC] \leq [FX]$$

(2) C/R

C/R can be determined from VC and FX.

$$[C/R] = \text{RND}([FX] / 8) \times [VC]$$

where RND(x) denotes 'rounded up to the next highest integer. [C/R] is the number of bytes per line, not the number of characters

(3) TC/R

TC/R must satisfy the condition $[TC/R]^3 [C/R] + 4$.

(4) fOSC and fFR

Once TC/R has been set, the frame frequency, fFR, and lines per frame [L/F] will also have been set. The lower limit on the oscillator frequency fOSC is given by:

$$f_{osc} \geq ([TC/R] \times 9 + 1) \times [L/F] \times f_{FR}$$

(5) If no standard crystal close to the calculated value of fOSC exists, a higher frequency crystal can be used and the value of TC/R revised using the above equation.

(6) Symptoms of an incorrect TC/R setting are listed below. If any of these appears, check the value of TC/R and modify it if necessary.

- Vertical scanning halts and a high-contrast horizontal line appears.
- All pixels are on or off.
- The LP output signal is absent or corrupted.
- The display is unstable.

Table 26. Epson LCD unit example parameters

Product name and resolution (X × Y)	[FX]	[FY]	[C/R]	TC/R	fosc (MHz) See Note 2.
256 × 64	[FX] = 6 pixels: 256 / 6 = 42 remainder 4 = 4 blank pixels	8 or 16, depending on the screen	[C/R] = 42 = 2AH bytes: C/R = 29H. When using HDOT SCR, [C/R] = 43 bytes	2DH	1.85
512 × 64	[FX] = 6 pixels: 512 / 6 = 85 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[C/R] = 85 = 55H bytes: C/R = 54H. When using HDOT SCR, [C/R] = 86 bytes	58H	3.59
256 × 128	[FX] = 8 pixels: 256 / 8 = 32 remainder 0 = no blank pixels	8 or 16, depending on the screen	[C/R] = 32 = 20H bytes: C/R = 19H. When using HDOT SCR, [C/R] = 33 bytes	22H	2.90
512 × 128	[FX] = 10 pixels: 512 / 10 = 51 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[C/R] = 102 = 66H bytes: C/R = 65H. When using HDOT SCR, [C/R] = 103 bytes	69H	8.55

Notes:

1. The remainder pixels on the right-hand side of the display are automatically blanked by the RA8835F. There is no need to zero the display memory corresponding to these pixels.
2. Assuming a frame frequency of 60 Hz.

Initialization example

The initialization example shown in Figure 57 is for a RA8835 series with an 8-bit microprocessor interface bus and an Epson EG4810S-AR display unit (512 X 128 pixels).

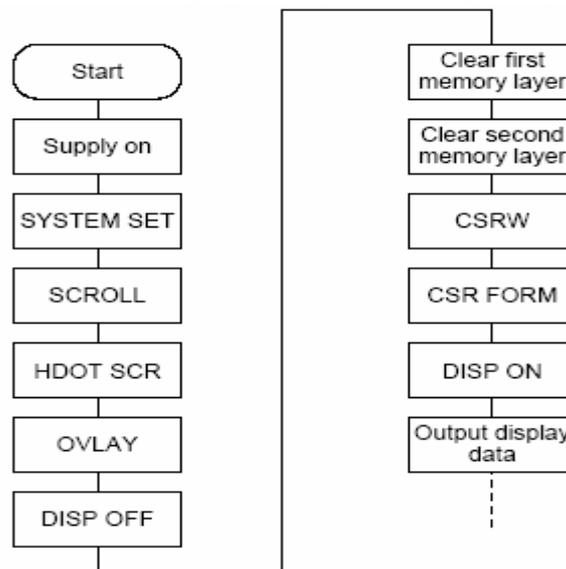


Figure 57. Initialization procedure

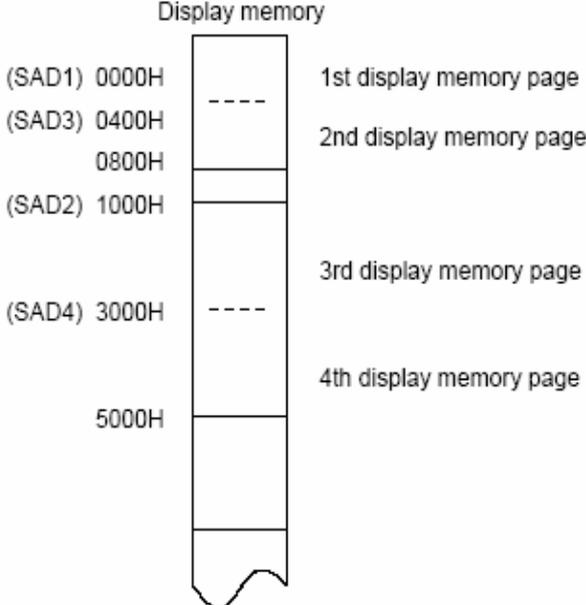
Note: Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20H (text screen only) or 00H (graphics screen only). Determining which memory to clear is explained in section 16.1.3.

Table 27. Initialization procedure

No.	Command	Operation
1	Power-up	
2	Supply	
3	SYSTEM SET C = 40H P1 = 38H P2 = 87H P3 = 07H P4 = 3FH P5 = 49H P6 = 7FH P7 = 80H P8 = 00H	M0: Internal CG ROM M1: CG RAM is 32 characters maximum M2: 8 lines per character W/S: Two-panel drive IV: No top-line compensation FX: Horizontal character size = 8 pixels WF: Two-frame AC drive FY: Vertical character size = 8 pixels C/R: 64 display addresses per line TC/R: Total address range per line = 90 fosc = 6.0 MHz, fFR = 70 Hz L/F: 128 display lines AP: Virtual screen horizontal size is 128 addresses
4	SCROLL C = 44H P1 = 00H P2 = 00H P3 = 40H P4 = 00H P5 = 10H P6 = 40H P7 = 00H P8 = 04H	First screen block start address Set to 0000H Display lines in first screen block = 64 Second screen block start address Set to 1000H Display lines in second screen block = 64 Third screen block start address Set to 0400H

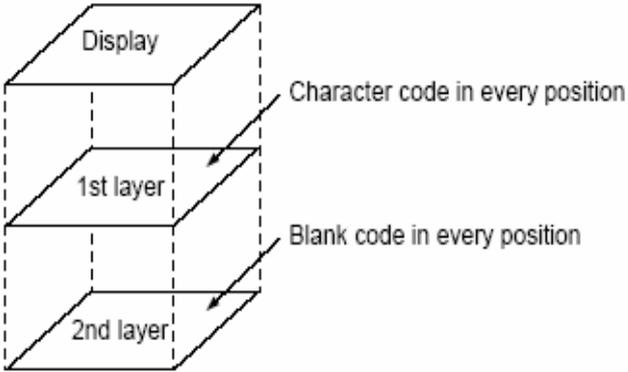
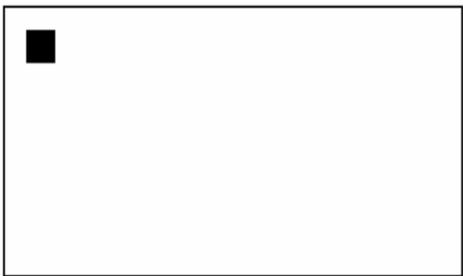
(continued)

Table 27. Initialization procedure (continued)

No.	Command	Operation
	P9 = 00H P10 = 30H	Fourth screen block start address Set to 3000H <div style="text-align: center;"> Display memory  </div>
5	HDOT SCR C = 5AH P1 = 00H	Set horizontal pixel shift to zero
6	OVLAY C = 5BH P1 = 01H	MX 1, MX 0: Inverse video superposition DM 1: First screen block is text mode DM 2: Third screen block is text mode
7	DISP ON/OFF C = 58H P1 = 56H	D: Display OFF FC1, FC0: Flash cursor at 2 Hz FP1, FP0: First screen block ON FP3, FP2: Second and fourth screen blocks ON FP5, FP4: Third screen block ON
8	Clear data in first layer	Fill first screen layer memory with 20H (space character)

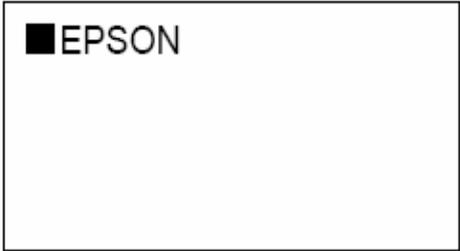
(continued)

Table 27. Initialization procedure (continued)

No.	Command	Operation
9	Clear data in second layer	Fill second screen layer memory with 00H (blank data) 
10	CSRW C = 46H P1 = 00H P2 = 00H	Set cursor to start of first screen block
11	CSR FORM C = 5DH P1 = 04H P2 = 86H	CRX: Horizontal cursor size = 5 pixels CRY: Vertical cursor size = 7 pixels CM: Block cursor
12	DISP ON/OFF C = 59H	Display ON 
13	CSR DIR C = 4CH	Set cursor shift direction to right

(continued)

Table 27. Initialization procedure (continued)

No.	Command	Operation
14	MWRITE C = 42H P1 = 20H P2 = 45H P3 = 50H P4 = 53H P5 = 4FH P6 = 4EH	‘ ‘ ‘E’ ‘P’ ‘S’ ‘O’ ‘N’ 
15	CSRW C = 46H P1 = 00H P2 = 10H	Set cursor to start of second screen block
16	CSR DIR C = 4FH	Set cursor shift direction to down
17	MWRITE C = 42H P1 = FFH ↓ P9 = FFH	Fill in a square to the left of the ‘E’ 
18	CSRW C = 46H P1 = 01H P2 = 10H	Set cursor address to 1001H
19	MWRITE C = 42H	

(continued)

Table 27. Initialization procedure (continued)

No.	Command	Operation
	P1 = FFH ↓ P9 = FFH CSRW	Fill in the second screen block in the second column of line 1
20	↓	Repeat operations 18 and 19 to fill in the background under 'EPSON'
29	MWRITE	Inverse display 
30	CSRW C = 46H P1 = 00H P2 = 01H	Set cursor to line three of the first screen block
31	CSR DIR C = 4CH	Set cursor shift direction to right
32	MWRITE C = 42H P1 = 44H P2 = 6FH P3 = 74H P4 = 20H P5 = 4DH P6 = 61H P7 = 74H P8 = 72H P9 = 69H P10 = 78H P11 = 20H P12 = 4CH P13 = 43H P14 = 44H	'D' 'o' 't' '.' Inverse display  'M' 'a' 't' 'r' 'i' 'x' '.' 'L' 'C' 'D'

Display mode setting example 1: combining text and graphics

(1) Conditions

- 320 X 200 pixels, single-panel drive (1/200 duty cycle)
- First layer: text display
- Second layer: graphics display
- 8 X 8-pixel character font
- CG RAM not required

(2) Display memory allocation

- First layer (text): $320/8 = 40$ characters per line, $200/8 = 25$ lines. Required memory size = $40 \times 25 = 1000$ bytes.
- Second layer (graphics): $320/8 = 40$ characters per line, $200/1 = 200$ lines. Required memory size = $40 \times 200 = 8000$ bytes.

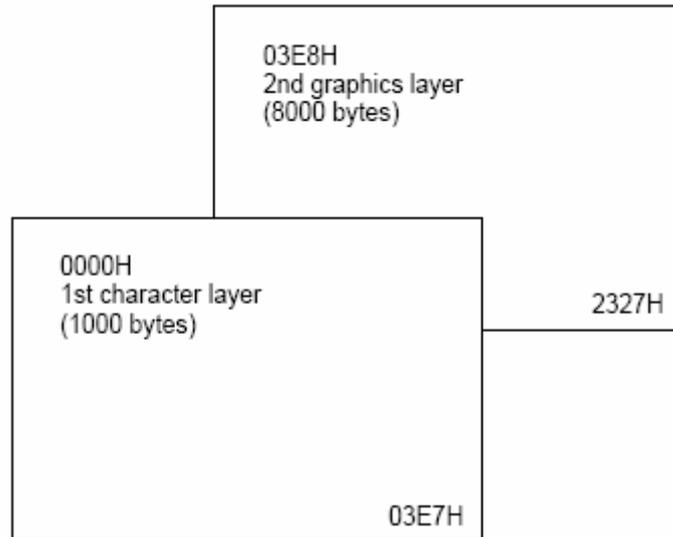


Figure 58. Character over graphics layers

(3) Register setup procedure
SYSTEM SET TC/R calculation

C = 40H
 P1 = 30H $f_{osc} = 6 \text{ MHz}$
 P2 = 87H $f_{FR} = 70 \text{ Hz}$
 P3 = 07H
 P4 = 27H $(1/6) \times 9 \times [TC/R] \times 200 = 1/70$
 P5 = 2FH $[TC/R] = 48$, so TC/R = 2FH
 P6 = C7H
 P7 = 28H
 P8 = 00H

CSR FORM

C = 5DH
 P1 = 04H
 P2 = 86H

HDOT SCR

C = 5AH
 P1 = 00H

SCROLL

C = 44H
 P1 = 00H
 P2 = 00H
 P3 = C8H
 P4 = E8H
 P5 = 03H
 P6 = C8H
 P7 = XH
 P8 = XH
 P9 = XH
 P10 = XH

OVLAY

C = 5BH
 P1 = 00H

DISP ON/OFF

C = 59H
 P1 = 16H

X = Don't care

Display mode setting example 2: combining graphics and graphics
(1) Conditions

- 320 X 200 pixels, single-panel drive (1/ 200 duty cycle)
- First layer: graphics display
- Second layer: graphics display

(2) Display memory allocation

- First layer (graphics): $320/8 = 40$ characters per line, $200/1 = 200$ lines. Required memory size = $40 \times 200 = 8000$ bytes.
- Second layer (graphics): $320/8 = 40$ characters per line, $200/1 = 200$ lines. Required memory size = 8000 bytes.

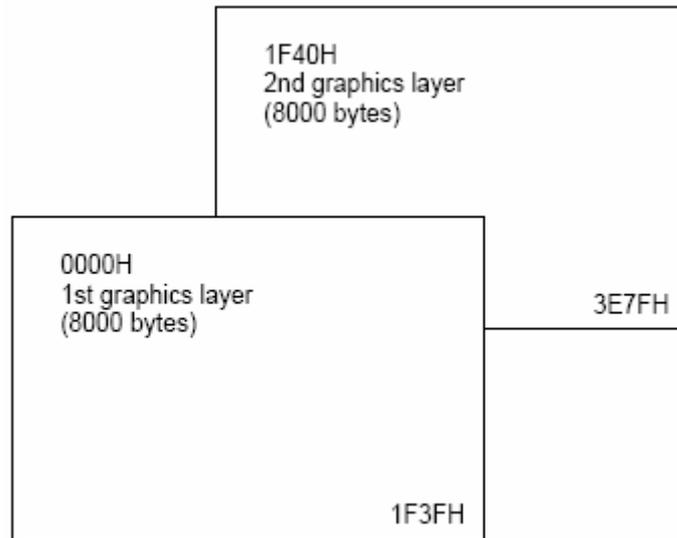


Figure 59. Two-layer graphics

(3) Register setup procedure

SYSTEM SET	TC/R calculation
C = 40H	
P1 = 30H	$f_{OSC} = 6 \text{ MHz}$
P2 = 87H	$f_{FR} = 70 \text{ Hz}$
P3 = 07H	
P4 = 27H	$(1/6) \times 9 \times [TC/R] \times 200 = 1/70$
P5 = 2FH	$[TC/R] = 48$, so $TC/R = 2FH$
P6 = C7H	
P7 = 28H	
P8 = 00H	
SCROLL	
C = 44H	
P1 = 00H	
P2 = 00H	
P3 = C8H	
P4 = 40H	
P5 = 1FH	
P6 = C8H	
P7 = XH	
P8 = XH	
P9 = XH	
P10 = XH	

CSR FORM

C = 5DH
P1 = 07H
P2 = 87H

HDOT SCR
C = 5AH
P1 = 00H

OVLAY
C = 5BH
P1 = 0CH

DISP ON/OFF
C = 59H
P1 = 16H

X = Don't care

Display mode setting example 3: combining three graphics layers

(1) Conditions

- 320 X 200 pixels, single-panel drive (1/200 duty cycle)
- First layer: graphics display

- Second layer: graphics display
 - Third layer: graphics display
- (2) Display memory allocation
- All layers (graphics): $320/8 = 40$ characters per line, $200/1 = 200$ lines. Required memory size = $40 \times 200 = 8000$ bytes.

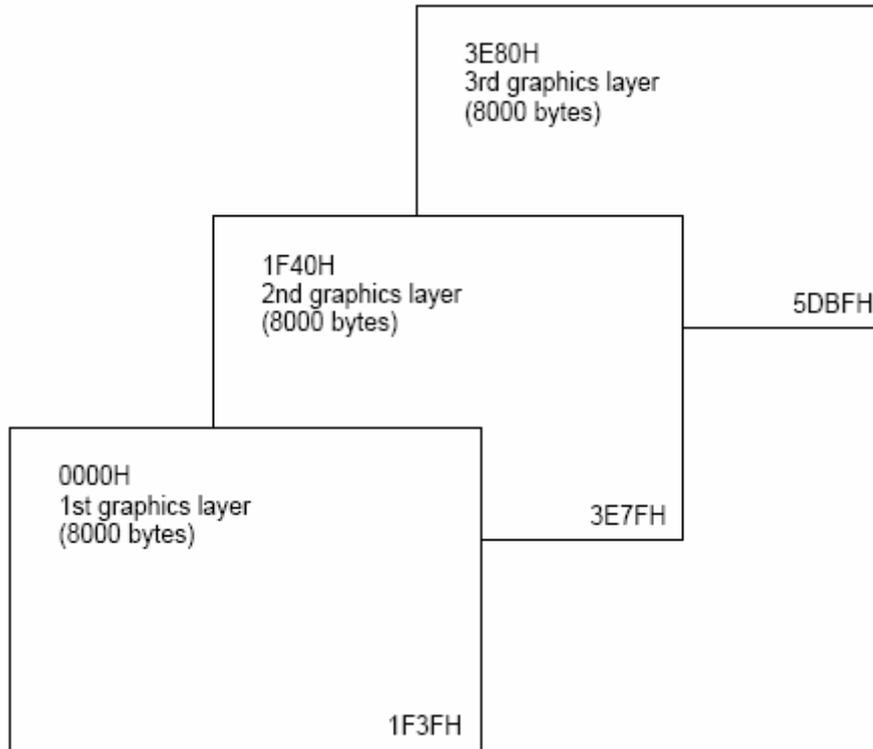


Figure 60. Three-layer graphics

Register setup procedure

SYSTEM SET TC/R calculation

C = 40H
 P1 = 30H $f_{osc} = 6 \text{ MHz}$
 P2 = 87H $f_{FR} = 70 \text{ Hz}$
 P3 = 07H
 P4 = 27H $(1/6) \times 9 \times [TC/R] \times 200 = 1/70$
 P5 = 2FH $[TC/R] = 48$, so $TC/R = 2FH$
 P6 = C7H
 P7 = 28H
 P8 = 00H

CSR FORM

C = 5DH
 P1 = 07H
 P2 = 87H

HDOT SCR

C = 5AH
 P1 = 00H

SCROLL

C = 44H
 P1 = 00H
 P2 = 00H
 P3 = C8H
 P4 = 40H
 P5 = 1FH
 P6 = C8H
 P7 = 80H
 P8 = 3EH
 P9 = XH
 P10 = XH

OVLAY

C = 5BH
 P1 = 1CH

DISP ON/OFF

C = 59H
 P1 = 16H

X = Don't care

2.10.2 System Overview

Figure 61 shows the RA8835 series in a typical system. The microprocessor issues instructions to the RA8835 series, and the RA8835 series drives the LCD panel and may have up to 64KB of display memory. Since all of the LCD control circuits are integrated onto the RA8835 series, few external components are required to construct a complete medium-resolution liquid crystal display.

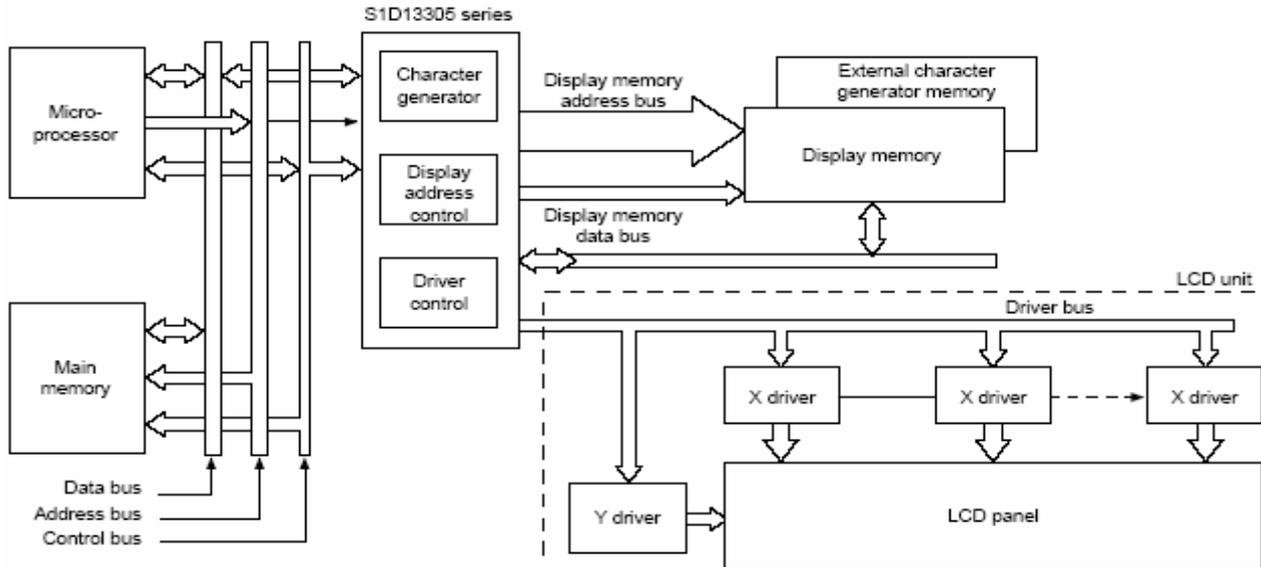


Figure 61. System block diagram

2.10.3. System Interconnection

RA8835F

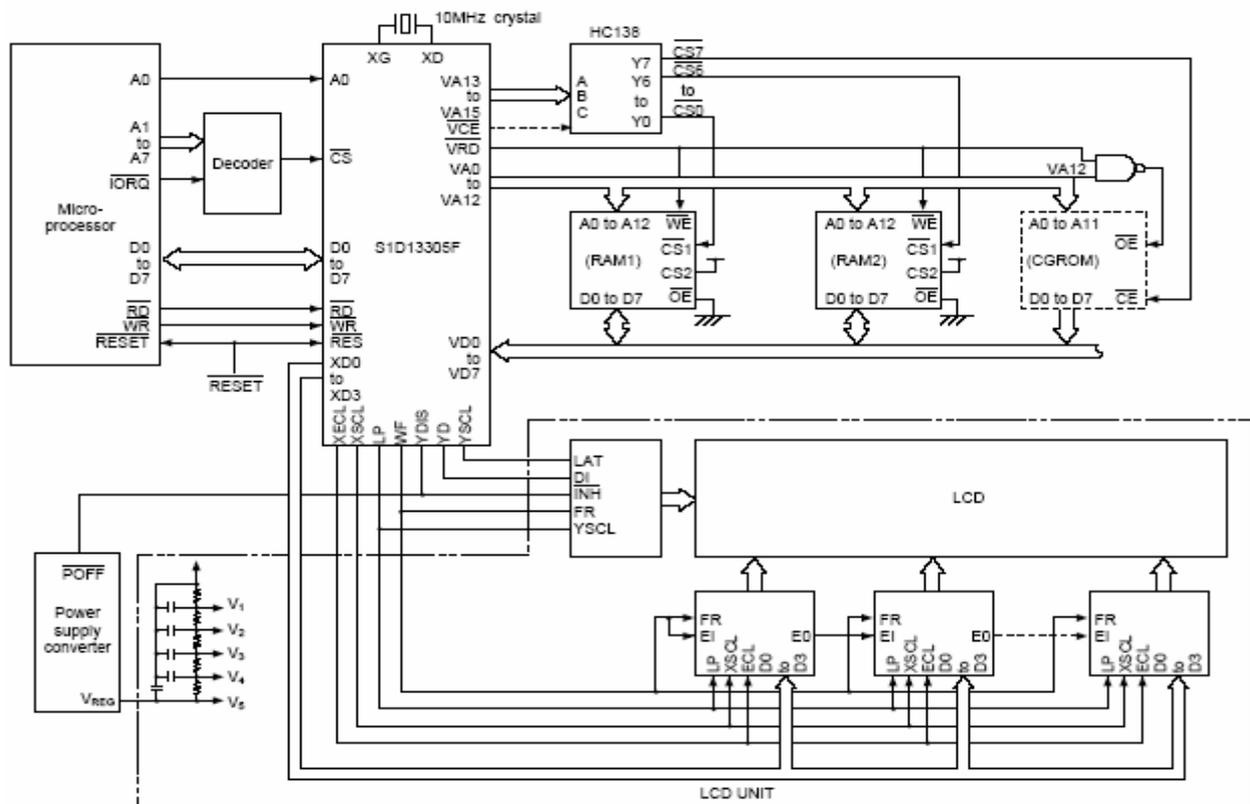


Figure 62. System interconnection diagram

The RA8835 series layered screens and flexible scrolling facilities support a range of display functions

and reduces the load on the controlling microprocessor when displaying underlining, inverse display, text overlaid on graphics or simple animation. These facilities are supported by the RA8835 series ability to divide display memory into up to four different areas.

(1) Character code table

- Contains character codes for text display
- Each character requires 8 bits
- Table mapping can be changed by using the scroll start function

(2) Graphics data table

- Contains graphics bitmaps
- Word length is 8 bits
- Table mapping can be changed

(3) CG RAM table

- Character generator memory can be modified by the external microprocessor
- Character sizes up to 8 X 16-pixels (16 bytes per character)
- Maximum of 64 characters
- Table mapping can be changed

(4) CG ROM table

- Used when the internal character generator is not adequate
- Can be used in conjunction with the internal character generator and external character generator RAM
- Character sizes up to 8 ´ 16-pixels (16 bytes per character)
- Maximum of 256 characters
- Fixed mapping at F000H to FFFFH

2.10.4 Smooth Horizontal Scrolling

Figure 63 illustrates smooth display scrolling to the left. When scrolling left, the screen is effectively moving to the right, over the larger virtual screen.

Instead of changing the display start address SAD and shifting the display by eight pixels, smooth scrolling is achieved by repeatedly changing the pixel-shift parameter of the HDOT SCR command. When the display has been scrolled seven pixels, the HDOT SCR pixel-shift parameter is reset to zero and SAD incremented by one. Repeating this operation at a suitable rate gives the appearance of smooth scrolling. To scroll the display to the right, the reverse procedure is followed.

When the edge of the virtual screen is reached, the microprocessor must take appropriate steps so that the display is not corrupted. The scroll must be stopped or the display modified.

Note that the HDOT SCR command cannot be used to scroll individual layers.

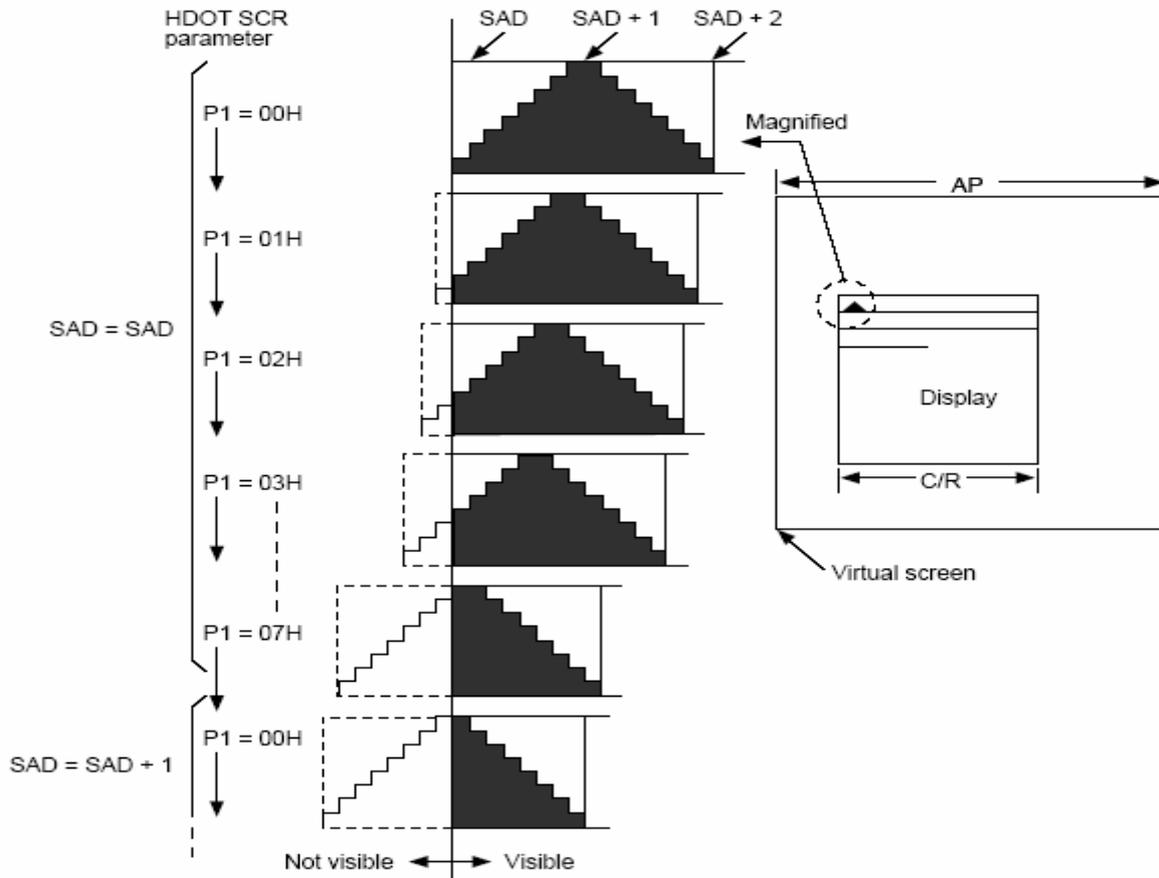


Figure 63. HDOT SCR example

Note: The response time of LCD panels changes considerably at low temperatures. Smooth scrolling under these conditions may make the display difficult to read.

2.10.5. Layered Display Attributes

RA8835 series incorporates a number of functions for enhanced displays using monochrome LCD panels. It allows the display of inverse characters, half-intensity menu pads and flashing of selected screen areas. These functions are controlled by the OVLAY and DISP ON/ OFF commands.

Attribute	MX1	MX0	Combined layer display	1st layer display	2ndt layer display
Reverse	0 1	1 1	IV	IV EPSON	
Half-tone	0 1	0 1	ME	ME Yes, No	
Local flashing	0 0	0 1	BL	BL	
Ruled line	0 0 1	0 1 1	RL	RL LINE LINE	

Figure 64. Layer synthesis

A number of means can be used to achieve these effects, depending on the display configuration. These are listed below. Note, however, that not all of these can be used in the one layer at the same time.

Inverse display

The first layer is text, the second layer is graphics.

1. CSRW, CSDIR, MWRITE

Write is into the graphics screen at the area to be inverted.

2. OVLAY: MX0 = 1, MX1 = 0

Set the combination of the two layers to Exclusive-OR.

3. DISP ON/OFF: FP0 = FP1 = 1, FP2 = FP3 = 0.

Turn on layers 1 and 2.

Half-tone display

The FP parameter can be used to generate half-intensity display by flashing the display at 17 Hz. Note that this mode of operation may cause flicker problems with certain LCD panels.

(1) Menu pad display

Turn flashing off for the first layer, on at 17 Hz for the second layer, and combine the screens using the OR function.

1. OVLAY: P1 = 00H
2. DISP ON/OFF: P1 = 34H

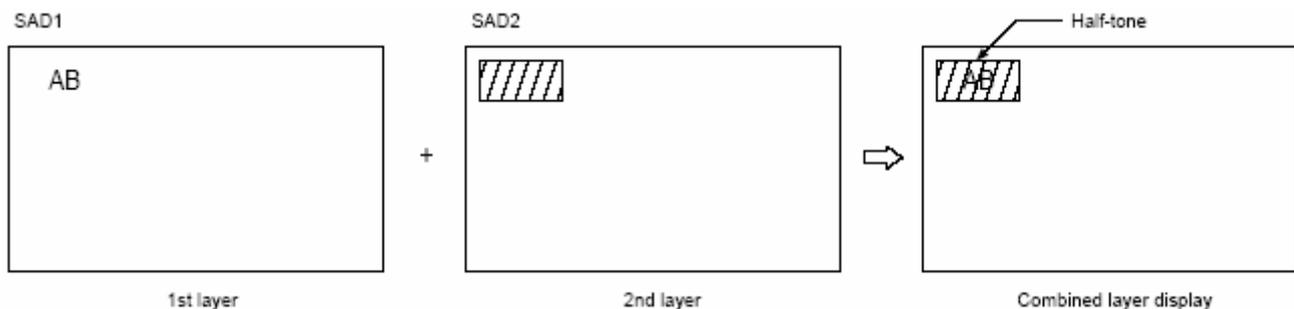


Figure 65. Half-tone character and graphics

(2) Graph display

To present two overlaid graphs on the screen, configure the display as for the menu bar display and put one graph on each screen layer. The difference in contrast between the half- and full-intensity displays will make it easy to distinguish between the two graphs and help create an attractive display.

1. OVLAY: P1 = 00H
2. DISP ON/OFF: P1 = 34H

Flashing areas

(1) Small area

To flash selected characters, the MPU can alternately write the characters as character codes and blank characters at intervals of 0.5 to 1.0 seconds.

(2) Large area

Divide both layer 1 and layer 2 into two screen blocks each, layer 2 being divided into the area to be flashed and the remainder of the screen. Flash the layer 2 screen block at 2 Hz for the area to be flashed and combine the layers using the OR function.

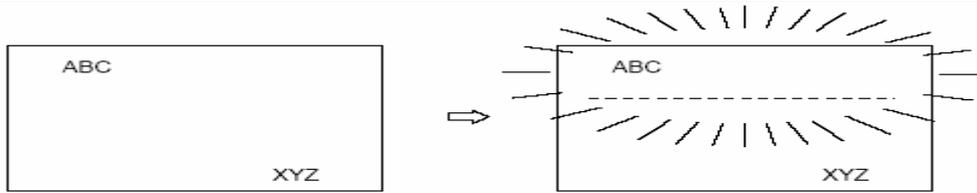


Figure 66. Localized flashing

2.10.6. 16 X 16-dot Graphic Display

Command usage

This example shows how to display 16 X 16-pixel characters. The command sequence is as follows:

CSRW Set the cursor address.

CSRDIR Set the cursor auto-increment direction.

MWRITE Write to the display memory.

Kanji character display

The program for writing large characters operates as follows:

1. The microprocessor reads the character data from its ROM.
2. The microprocessor sets the display address and writes to the VRAM. The flowchart is shown in Figure 69.

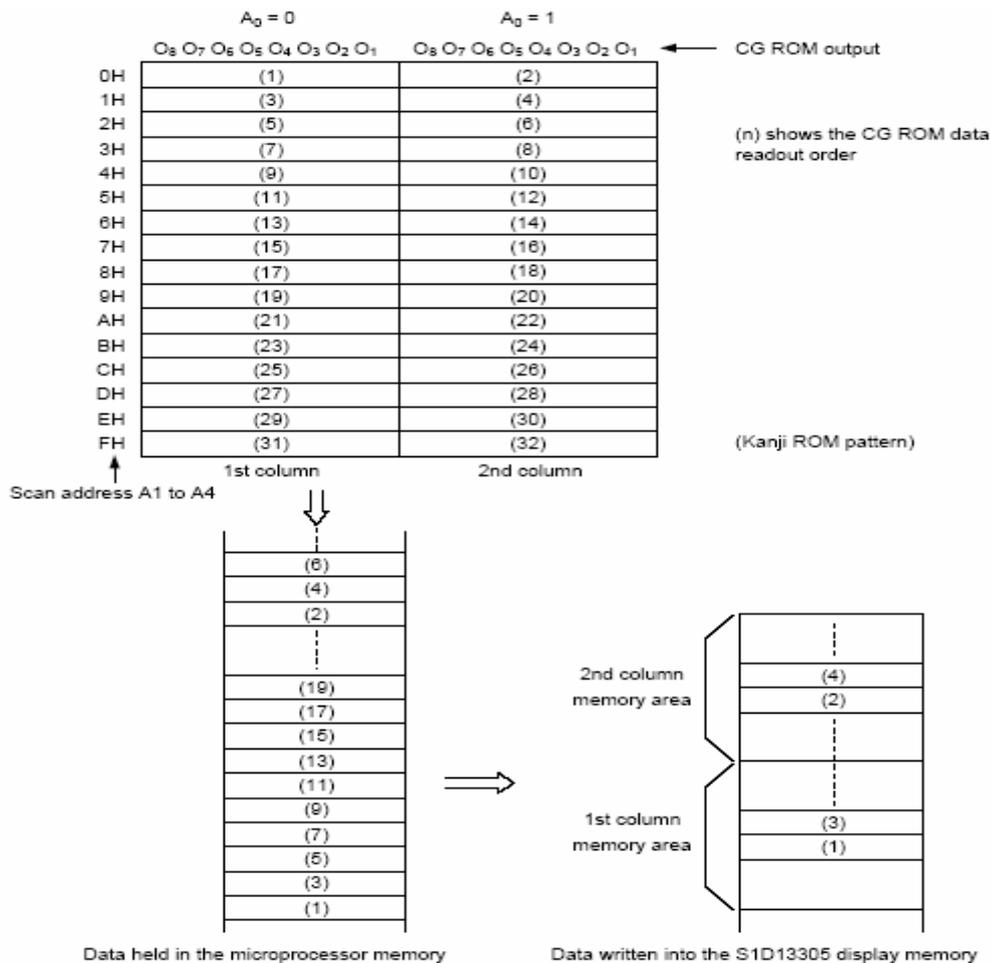


Figure 67. Graphics address indexing

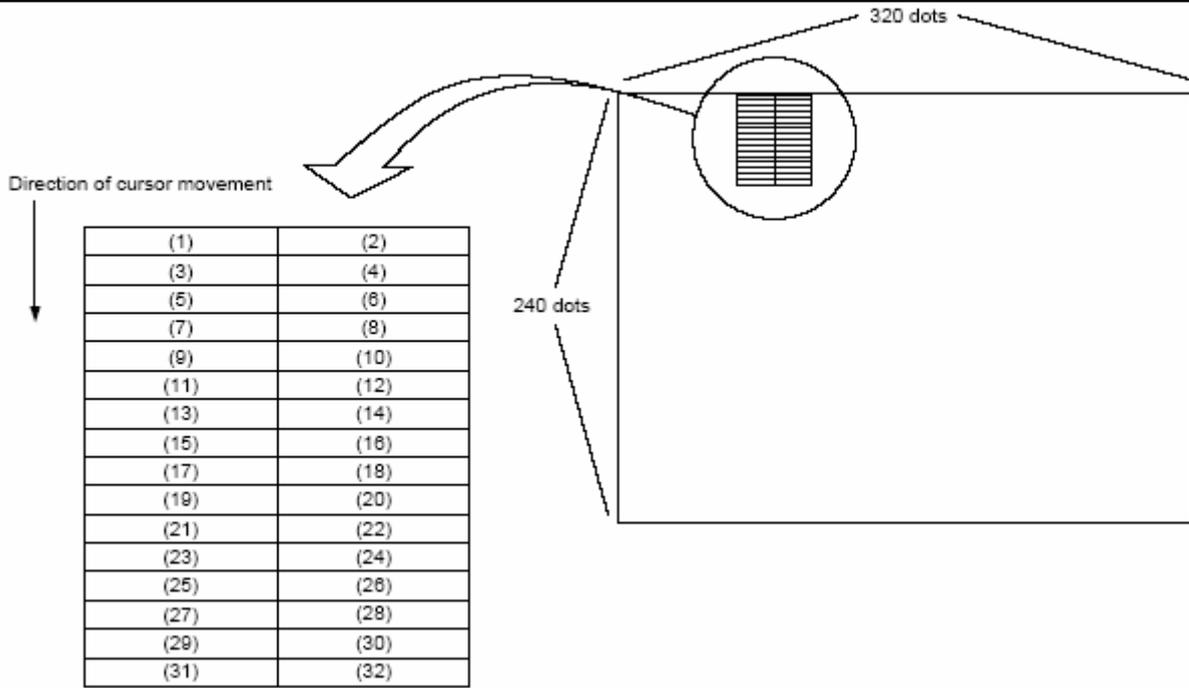


Figure 68. Graphics bit map

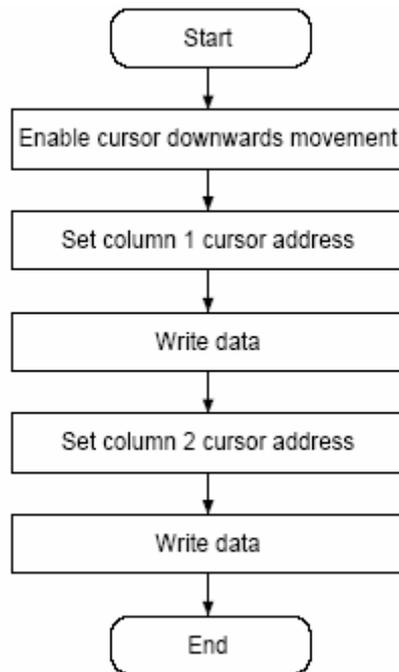


Figure 69. 16 X 16-dot display flowchart

Using an external character generator ROM, and 8 X 16- pixel font can be used, allowing a 16 X 16-pixel character to be displayed in two segments. The external CG ROM EPROM data format is described in Section 9.1. This will allow the display of up to 128, 16 X 16-pixel characters. If CG RAM is also used, 96 fixed characters and 32 bankswitchable characters can also be supported.

2.11 INTERNAL CHARACTERISTIC GENERATOR FONT

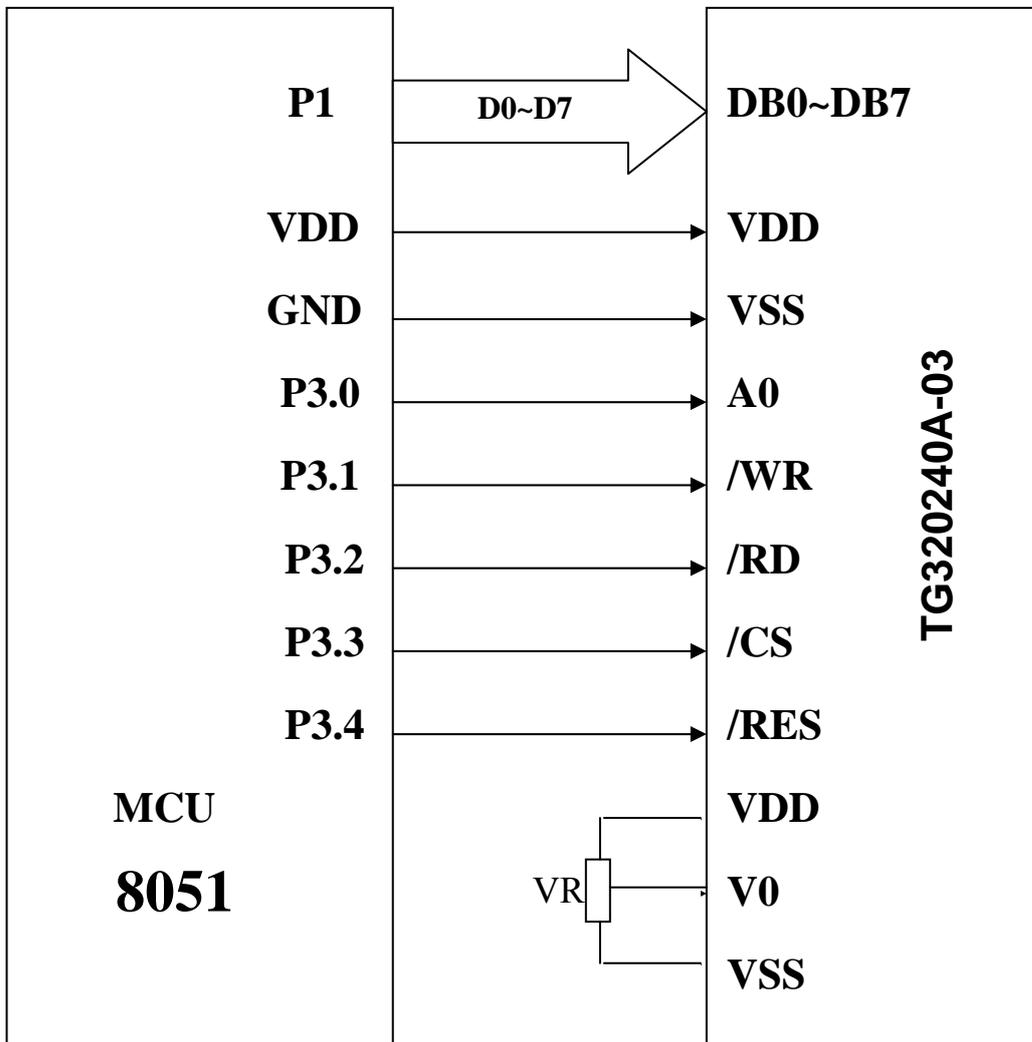
		Character code bits 0 to 3															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Character code bits 4 to 7	2		!	"	#	\$	%	&	'	()	*	+	,	-	.	/
	3	@	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
	4	@	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
	5	p	q	r	s	t	u	v	w	x	y	z	{	}	~		
	6	'	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
	7	p	q	r	s	t	u	v	w	x	y	z	{	}	~	*	*
	A		a	r	.	,	;	:	<	>	~	*	*	*	*	*	*
	B	-	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
	C	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
	D	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
1	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	

Figure 70. On-chip character set

Note

The shaded positions indicate characters that have the whole 6 X 8 bitmap blackened.

2.12 MCU And Module Connection



VR:30~50K

2.13. GLOSSARY OF TERMS

A	Address
AP	Address pitch parameter
C	Character display mode
CD	Cursor direction of movement parameter
CG	Character generator
CGRAM ADR	Character generator memory address
CM	Cursor display shape parameter
C/R	Characters per row parameter
CRX	Horizontal cursor size parameter
CRY	Vertical cursor size parameter
CSR DIR	Cursor direction of movement instruction
CSR FORM	Cursor size, position and type instruction
CSRR Read	cursor address register instruction
CSRW	Write cursor address register instruction
DM	Display mode parameter
FC	Flashing cursor parameter
fFR	Frame frequency
Fosc	Oscillator frequency
FP	Screen flashing parameter
FX	Horizontal character size parameter
FY	Vertical character size parameter
G	Graphics display mode
GLC	Graphic line control unit
HDOT	SCR Horizontal scrolling by pixels instruction
IV	Screen origin compensation for inverse display
L/F	Lines per frame instruction
MREAD	Display memory read instruction
MWRITE	Display memory write instruction
MX	Screen composition mode
OV	Graphics layer select parameter
OVLAY	Screen layer mode instruction
P	Parameter
R	Row
RAM	Random access memory
ROM	Read only memory
SAD	Display scrolling start address parameter
SL	Display scrolling length parameter
TC/R	Length, including horizontal blanking, of one screen line
VRAM	Display memory
WF	Display drive waveform parameter
W/S	Windows per screen parameter

3. RELIABILITY TEST AND QUALITY

3.1. RELIABILITY TEST CONDITION

No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	60 °C 200 hrs	-----
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-10 °C 200 hrs	-----
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50 °C 200 hrs	-----
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	0 °C 200 hrs	-----
5	High temperature / Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	60 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
6	High temperature / Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. $\begin{array}{c} -10^{\circ}\text{C} \rightleftharpoons 25^{\circ}\text{C} \rightleftharpoons 60^{\circ}\text{C} \\ \leftarrow 30\text{min} \quad \quad 5\text{min.} \quad \quad 30\text{min} \rightarrow \\ \leftarrow \quad \rightarrow \\ \text{1 cycle} \end{array}$	-10°C / 60°C 10 cycles	-----

Supply voltage for logic system = 5V. Supply voltage for LCD system = Operating voltage at 25 °C.

Mechanical Test

Vibration test	Endurance test applying the vibration during transportation and using	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hour	
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msede 3 times of each direction	
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air	115mbar 40hrs	
Static electricity test	Endurance test applying the electric stress to the terminal	VS=800V,RS-1.5KΩ CS=100pF, 1 time	

Failure Judgment criterion

Criterion Item	Test Item No.											Failure Judgment Criterion	
	1	2	3	4	5	6	7	8	9	10	11		
Basic specification													Out of the Basic specification
Electrical characteristic													Out of the DC and AC characteristic
Mechanical characteristic													Out of the Mechanical specification Color change: out of Limit Appearance Specification
Optical characteristic													Out of the Appearance Standard

3.2. QUALITY GUARANTEE

Acceptable Quality Level, Each lot should satisfy the quality level defined as follows.

-Inspection method: MIL-STD-105E LEVEL II Normal one time sampling

AQL

Partition	AQL	Description
A: Major	0.4%	Functional defective product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

Definition of ‘LOT’

One lot means the delivery quality to customer at once time.

Conditions of Cosmetic Inspection

. Environmental condition

The inspection should be performed at the 1 metre height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25°C and normal humidity 60±15%RH).

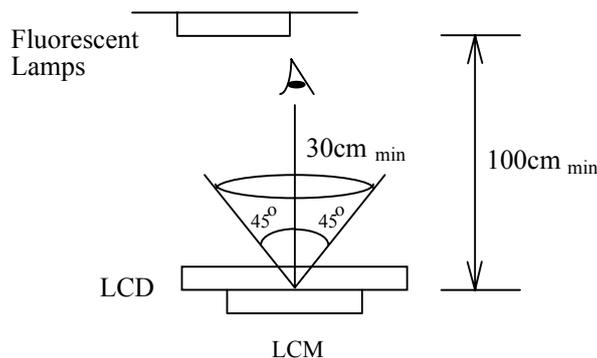
Driving voltage

The Vo value which the most optimal contrast can be obtained near the specified Vo in the specification (Within of the typical value at 25°C.).

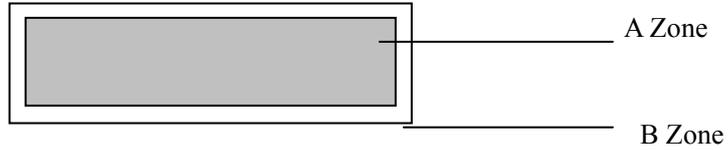
3.3. INSPECTION METHOD

The visual check should be performed vertically at more than 30cm distance from the LCD panel

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:

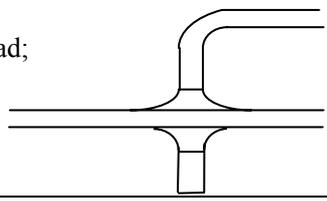
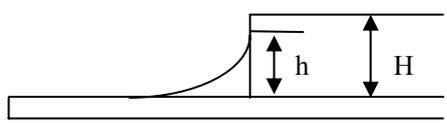


A Zone: Active display area (minimum viewing area).

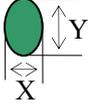
B Zone: Non-active display area (outside viewing area).

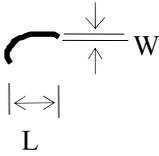
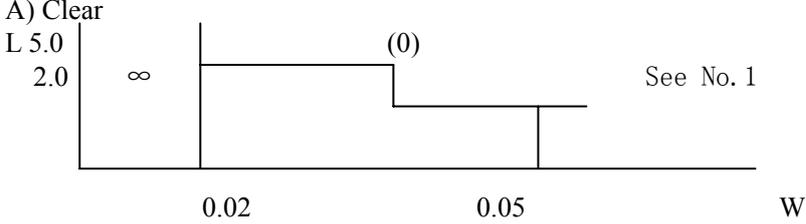
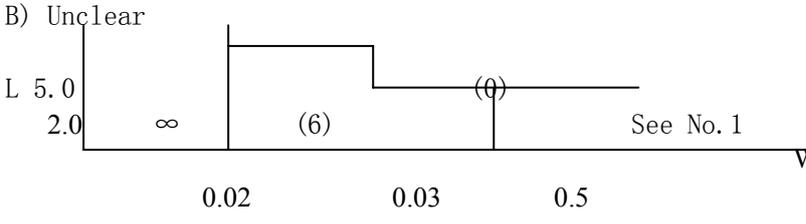
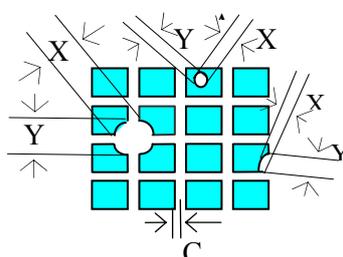
3.4. INSPECTION STANDARD FOR SOLDER

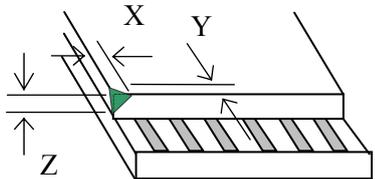
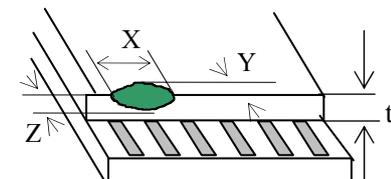
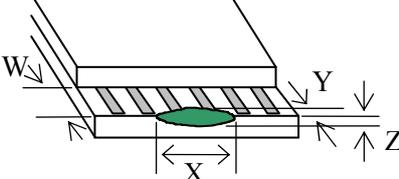
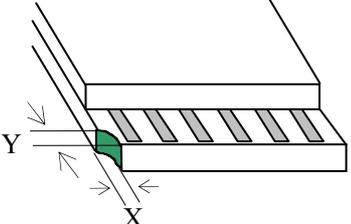
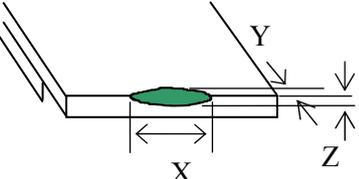
Module Cosmetic Criteria

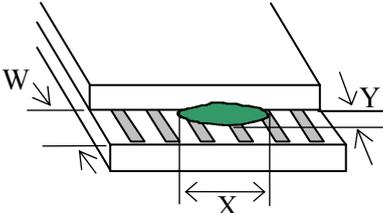
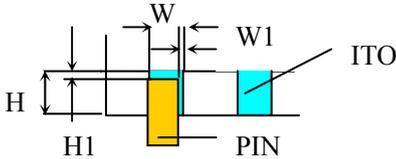
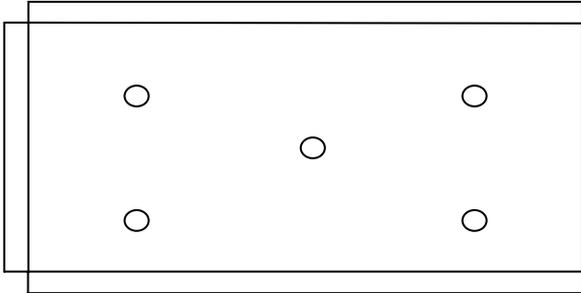
No.	Item	Judgment Criterion	Partition	
1	Difference in Spec.	None allowed	Major	
2	Pattern Peeling	No substrate pattern peeling and floating	Major	
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor	
4	Resist flaw on substrate	Invisible copper foil ($\Phi 0.5\text{mm}$ or more) on substrate pattern	Minor	
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed $\Phi 0.2\text{mm}$)	Minor Minor	
6	Stain	No stain to spoil cosmetic badly	Minor	
7	Plate discoloring	No plate fading, rusting and discoloring	Minor	
8	Plate discoloring	a. Soldering side of PCB Solder to form a 'Filet' all around the lead; Solder should not hide the lead form perfectly too much	Minor	
	1. Lead parts			
	2. Flat packages			Either "toe" (A) or "heel" (B) of The lead to be covered by 'Filet' Lead form to be assume over Solder.
3. Chips	$(3/2) H \geq h \geq (1/2) H$		Minor	

3.5. SCREEN COSMETIC CRITERIA(APPEARANCE)

No.	Item	Criterion										
1	Short or open circuit	No allow										
	LC leakage											
	Flickering											
	No display											
	Wrong viewing direction											
	Wrong Back-light											
	Wrong or missing component											
2	Contrast defect (dim, ghost)	Refer to the approval sample										
	Background color deviation											
3	Point defect, Black spot, dust (including Polarizer) $\Phi=(X+Y)/2$	 <table border="1" data-bbox="885 828 1324 1075"> <thead> <tr> <th>Point Size</th> <th>Acceptable Qty.</th> </tr> </thead> <tbody> <tr> <td>$\phi \leq 0.10$</td> <td>Disregard</td> </tr> <tr> <td>$0.10 < \phi \leq 0.20$</td> <td>6</td> </tr> <tr> <td>$0.20 < \phi \leq 0.3$</td> <td>2</td> </tr> <tr> <td>$\phi > 0.30$</td> <td>0</td> </tr> </tbody> </table>	Point Size	Acceptable Qty.	$\phi \leq 0.10$	Disregard	$0.10 < \phi \leq 0.20$	6	$0.20 < \phi \leq 0.3$	2	$\phi > 0.30$	0
			Point Size	Acceptable Qty.								
			$\phi \leq 0.10$	Disregard								
			$0.10 < \phi \leq 0.20$	6								
			$0.20 < \phi \leq 0.3$	2								
$\phi > 0.30$	0											

No.	Item	Criterion																			
4	<p>Line defect,</p> <p>Scratch: In accordance with spots and lines operating cosmetic criteria. When the light reflective on the panel surface, the scratches are not to be remarkable.</p>	 <table border="1" data-bbox="845 376 1396 638"> <thead> <tr> <th colspan="2">Line</th> <th rowspan="2">Acceptable Qty.</th> </tr> <tr> <th>L</th> <th>W</th> </tr> </thead> <tbody> <tr> <td>---</td> <td>$0.015 \geq W$</td> <td>Disregard</td> </tr> <tr> <td>$3.0 \geq L$</td> <td>$0.03 \geq W$</td> <td rowspan="2">2</td> </tr> <tr> <td>$2.0 \geq L$</td> <td>$0.05 \geq W$</td> </tr> <tr> <td>$1.0 \geq L$</td> <td>$0.1 > W$</td> <td>1</td> </tr> <tr> <td>---</td> <td>$0.05 < W$</td> <td>Applied as point defect</td> </tr> </tbody> </table> <p>Unit: mm</p> <p>A) Clear</p>  <p>B) Unclear</p>  <p>Note: () –Acceptable Qty in active area L –Length (mm) W –Width (mm) ∞ –Disregard</p>	Line		Acceptable Qty.	L	W	---	$0.015 \geq W$	Disregard	$3.0 \geq L$	$0.03 \geq W$	2	$2.0 \geq L$	$0.05 \geq W$	$1.0 \geq L$	$0.1 > W$	1	---	$0.05 < W$	Applied as point defect
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---	$0.05 < W$	Applied as point defect																			
5	Rainbow	Not more than two colors change across the viewing area																			
6	<p>Dot-matrix pattern</p> <p>$\phi = (X+Y)/2$</p>	<p>Pin hole:</p>  <table border="1" data-bbox="989 1608 1396 1765"> <thead> <tr> <th>Size</th> <th>Acceptable Qty.</th> </tr> </thead> <tbody> <tr> <td>$\phi < 0.1$</td> <td>Disregard</td> </tr> <tr> <td>$0.10 \leq \phi \leq 0.20$</td> <td>1</td> </tr> <tr> <td>$\phi > 0.20$</td> <td>0</td> </tr> </tbody> </table> <p>C: Shall not touch other dot(s).</p>	Size	Acceptable Qty.	$\phi < 0.1$	Disregard	$0.10 \leq \phi \leq 0.20$	1	$\phi > 0.20$	0											
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No.	Item	Criterion																																	
7	<p>Chip</p> <p>Remark:</p> <p>X: Length direction</p> <p>Y: Short direction</p> <p>Z: Thickness direction</p> <p>t: Glass thickness</p> <p>W: Terminal Width</p>	 <table border="1" data-bbox="970 398 1375 472"> <caption>Acceptable criterion</caption> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤ 2</td> <td>0.5mm</td> <td>$\leq t$</td> </tr> </tbody> </table>  <table border="1" data-bbox="970 678 1362 752"> <caption>Acceptable criterion</caption> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤ 2</td> <td>0.5mm</td> <td>$\leq t/2$</td> </tr> </tbody> </table>  <table border="1" data-bbox="986 1048 1391 1122"> <caption>Acceptable criterion</caption> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>Disregard</td> <td>≤ 0.2</td> <td>$\leq t$</td> </tr> </tbody> </table>  <table border="1" data-bbox="978 1308 1367 1420"> <caption>Acceptable criterion</caption> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤ 3</td> <td>≤ 2</td> <td>$\leq t$</td> </tr> <tr> <td colspan="2">shall not reach to ITO</td> <td></td> </tr> </tbody> </table>  <table border="1" data-bbox="978 1639 1351 1713"> <caption>Acceptable criterion</caption> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤ 5</td> <td>≤ 2</td> <td>$\leq t/3$</td> </tr> </tbody> </table>	X	Y	Z	≤ 2	0.5mm	$\leq t$	X	Y	Z	≤ 2	0.5mm	$\leq t/2$	X	Y	Z	Disregard	≤ 0.2	$\leq t$	X	Y	Z	≤ 3	≤ 2	$\leq t$	shall not reach to ITO			X	Y	Z	≤ 5	≤ 2	$\leq t/3$
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No.	Item	Criterion																																	

8	Total no. of acceptable Defect	<p>A. Zone</p> <p>Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm</p> <p>B. Zone</p> <p>It is acceptable when it is no trouble for quality and assembly in customer's end product.</p>
9	Protruded W: Terminal Width	 <p>Acceptable criteria: $Y \leq 0.4$</p>
10	PIN	<p>Position</p>  <div style="border: 1px solid black; padding: 5px; width: fit-content; margin-left: auto;"> $W1 \leq 1/3W$ $H1 \leq 1/3H$ </div>
11	Uneven brightness (only back-lit type module)	<p>Uneven brightness must be $B_{MAX}/B_{MIN} \leq 2$</p> <p>-B_{MAX} : Max. value by measure in 5 points -B_{MIN} : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure</p> 
12	Allowable density	Above defects should be separated more than 10mm each other.
13	Rubbing line	Not to be noticeable.
14	Dot size	To be 95% ~ 105% of the dot size (typ.) in drawing, Partial defects of each dot (ex. Pin-hole) should be treated as 'spot'.(see Screen Cosmetic Criteria (operating) No.)

No.	Item	Criterion	
15	Bubbles in polarizer	Size : d mm	Acceptable Qty in active area
		$d \leq 0.3$	Disregard
		$0.3 < d \leq 1.0$	3
		$1.0 < d \leq 1.5$	1
		$1.5 < d$	0
16	Allowable density	Above defects should be separated more than 30mm each other	
17	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Backlit type should be judged with back-lit on state only.	
18	Contamination	Not to be noticeable.	

Note:

‘Clear’= the shade and size are not changed by Vo.

‘Unclear’= the shade and size are changed by V0.

Size: $d = (\text{long length} + \text{short length}) / 2$

The limit samples for each item have priority

Complete defects are defined item by item, but if the number of defects is defined in above table, the total number should not exceed 10.

In case of ‘concentration’, even the spots or the lines of ‘disregarded size should not allowed. Following three situations Should be treated as ‘concentration’.

-7 or over defects in circle of $\Phi 2\text{mm}$

-10 or over defects in circle of $\Phi 10\text{mm}$

-20 or over defects in circle of $\Phi 20\text{mm}$

3.6. PRECAUTIONS FOR USING LCM MODULES

1. Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

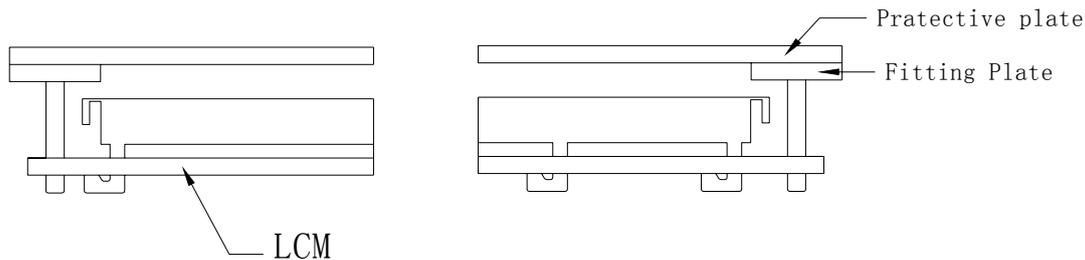
- (1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or Polarizer peel-off may occur with high humidity.
- (2) Do not touch, push or rub the exposed polarizer with anything harder than an HB Pencil lead (Glass, tweezers, etc.).
- (3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic, substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.
- (4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum. Do not scrub hard to avoid damaging the display surface.
- (5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
- (6) Avoid contacting oil and fats.
- (7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature the must be warmed up in a container before coming is contacting temperature air.
- (8) Do not put or attach anything on the display area to avoid leaving marks on.
- (9) Do not touch the display with bare hands. This will stain the display and degrade insulation between terminals (some cosmetics are determinate to the polarizers).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

3.7. INSTALLING LCM MODULES

The hole in the printed circuit board is used to fit LCM as shown in the picture below. Attend to the following items when installing the LCM

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be $\pm 0.1\text{mm}$

3.8. PRECAUTION FOR HANDING LCM MODULE

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

- (1) Do not alter, modify or change shape of the tab on the metal frame
- (2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- (3) Do not damage or modify the pattern writing on the printed circuit board.
- (4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
- (5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
- (6) Do not drop, bend or twist LCM

3.9. ELECTRO-STATIC DISCHARGE CONTROL

Since this module uses a CMOS LSI, the same attention should be paid to electrostatic discharge as for an ordinary

CMOS IC.

- (1) Make certain that you are grounded when handling LCM.
- (2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
- (3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
- (4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
- (5) As far as possible make the electric potential of your work clothes and that of the workbench the ground potential.
- (6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

3.10. PRECAUTION FOR SOLDERING TO THE LCM

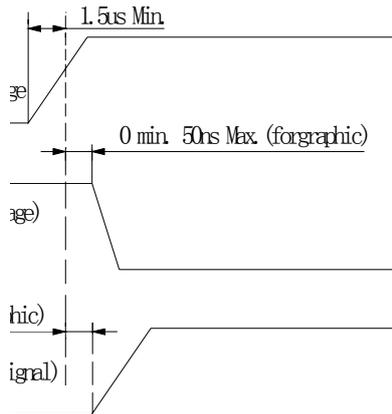
- (1) Observe the following when soldering lead wire , connector cable and etc. to the LCM
 - Soldering iron temperature: $280^{\circ}\text{C}\pm 10^{\circ}\text{C}$
 - Soldering time: 3-4 seconds
 - Solder: eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation.(This does not apply in the case of non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

- (2) When soldering the electro-luminescent panel and PC board, the panel and board should not be detached more than three times, This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
- (3) When remove the electro-luminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PX board could be damaged.

3.11. PRECAUTIONS FOR OPERATION

- (1) Viewing angle varies with the change of liquid crystal driving voltage (V_0). Adjust V_0 to show the best contrast.
- (2) Driving the LCD in the voltage above the limit shortens its life.
- (3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD cell be out of the order. It will recover when it returns to the specified temperature range.
- (4) If the display area is pushed hard during operation, the display will become abnormal, however, it will return to normal. If it is turned off and then back on. Used under the relative condition of 40°C , 50%RH.
- (5) When turning the power on input each signal after the positive/negative voltage becomes stable.



3.12. STORAGE

When storing LCD as spares for some years, the following precautions are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C
- (3) The polarizer surface should not come in contact with any other object.(we advise you to store them in the container in which they were shipped.)
- (4) Environmental conditions:
 - Don not leave them for more than 168hrs. at 60°C
 - Should not be left for more than 48hrs. at -20°C.

3.13. SAFETY

- (1) It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2)If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

3.14. LIMITED WARRANTY

Unless agreed between TINSHARP and customer, TINSHARP will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with TINSHARP LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to TINSHARP within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of TINSHARP limited to repair and/ or replacement on the terms set forth above. TINSHARP will not be responsible for any subsequent or consequential events.

3.15. RETURN LCM UNDER WARRANTY

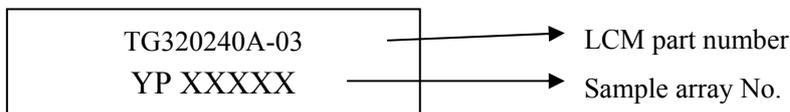
No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to or modifying the bezel in lay manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelets, conductors and terminals.

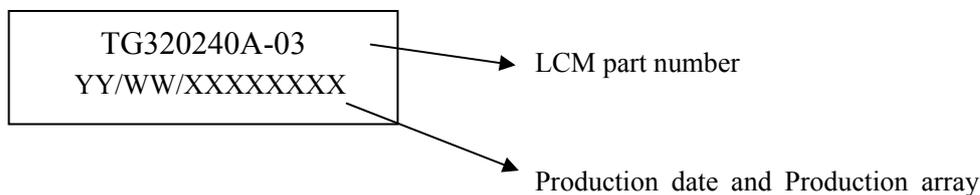
4. DATE CODE RULES

4-1. DATE CODE FOR SAMPLE



YP: meaning sample

4-2. DATE CODE FOR PRODUCTION



A. TG320240A-03 represents LCM part number

C. YY/WW represents Year, Month, and Week

YY—Year WW—Week

XXXXXXXX—Production array No.

END