# 93AA46A/B/C, 93LC46A/B/C, 93C46A/B/C

## 1-Kbit Microwire Compatible Serial EEPROM

### Device Selection Table

| Part Number | Vcc Range | ORG Pin | Word Size | Temp Ranges | Packages |
|---|---|---|---|---|---|
| 93AA46A | 1.8V-5.5V | No | 8-bit | I | P, SN, ST, MS, OT, MC, MN |
| 93AA46B | 1.8V-5-5V | No | 16-bit | I | P, SN, ST, MS, OT, MC, MN |
| 93LC46A | 2.5V-5.5V | No | 8-bit | I, E | P, SN, ST, MS, OT, MC, MN |
| 93LC46B | 2.5V-5.5V | No | 16-bit | I, E | P, SN, ST, MS, OT, MC, MN |
| 93C46A | 4.5V-5.5V | No | 8-bit | I, E | P, SN, ST, MS, OT, MC, MN |
| 93C46B | 4.5V-5.5V | No | 16-bit | I, E | P, SN, ST, MS, OT, MC, MN |
| 93AA46C | 1.8V-5.5V | Yes | 8-bit or 16-bit | I | P, SN, ST, MS, MC, MN |
| 93LC46C | 2.5V-5.5V | Yes | 8-bit or 16-bit | I, E | P, SN, ST, MS, MC, MN |
| 93C46C | 4.5V-5.5V | Yes | 8-bit or 16-bit | I, E | P, SN, ST, MS, MC, MN |

### Features

- Low-Power CMOS Technology
- ORG Pin to Select Word Size for '46C' Version
- 128 x 8-bit Organization 'A' Devices (no ORG)
- 64 x 16-bit Organization 'B' Devices (no ORG)
- Self-Timed Erase/Write Cycles (including Auto-Erase)
- Automatic Erase All (ERAL) Before Write All (WRAL)
- Power-On/Off Data Protection Circuitry
- Industry Standard 3-Wire Serial I/O
- Device Status Signal (Ready/$\overline{\text{Busy}}$)
- Sequential Read Function
- High Reliability:
  - Endurance: 1,000,000 erase/write cycles
  - Data Retention > 200 years
  - ESD protection: > 4,000V
- RoHS Compliant
- Temperature Ranges Supported:
  - Industrial (I) -40°C to +85°C
  - Extended (E) -40°C to +125°C
- Automotive AEC-Q100 Qualified

### Packages

- 8-Lead PDIP, 8-Lead MSOP, 8-Lead SOIC, 8-lead TSSOP, 6-Lead SOT-23, 8-Lead DFN and 8-Lead TDFN

### Pin Function Table

| Name | Function |
|---|---|
| CS | Chip Select |
| CLK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| Vss | Ground |
| NC | No internal connection |
| ORG | Memory Configuration |
| Vcc | Power Supply |

### Description

The Microchip Technology Inc. 93XX46A/B/C devices are 1-Kbit low-voltage serial Electrically Erasable PROMs (EEPROM). Word-selectable devices such as the 93AA46C, 93LC46C or 93C46C are dependent upon external logic levels driving the ORG pin to set word size. For dedicated 8-bit communication, the 93AA46A, 93LC46A or 93C46A devices are available, while the 93AA46B, 93LC46B and 93C46B devices provide dedicated 16-bit communication. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications.

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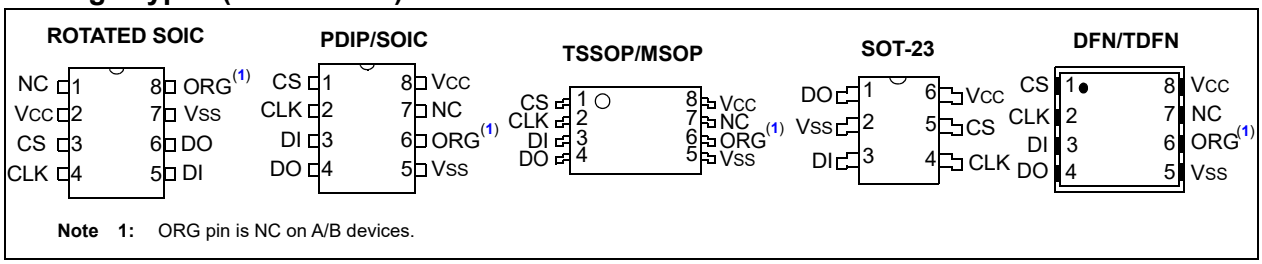
## Package Types (not to scale)




**Note 1:** ORG pin is NC on A/B devices.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## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

**† NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **All parameters apply over the specified ranges unless otherwise noted.** | | | **Industrial (I): TA = -40°C to +85°C, VCC = +1.8V TO +5.5V<br>Extended (E): TA = -40°C to +125°C, VCC = +2.5V TO +5.5V** | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Parameter** | **Min.** | **Typ** | **Max.** | **Units** | **Conditions** |
| D1 | VIH1 | High-level input voltage | 2.0 | — | VCC +1 | V | VCC ≥ 2.7V |
| | VIH2 | | 0.7 VCC | — | VCC +1 | V | VCC < 2.7V |
| D2 | VIL1 | Low-level input voltage | -0.3 | — | 0.8 | V | VCC ≥ 2.7V |
| | VIL2 | | -0.3 | — | 0.2 VCC | V | VCC < 2.7V |
| D3 | VOL1 | Low-level output voltage | — | — | 0.4 | V | IOL = 2.1 mA, VCC = 4.5V |
| | VOL2 | | — | — | 0.2 | V | IOL = 100 µA, VCC = 2.5V |
| D4 | VOH1 | High-level output voltage | 2.4 | — | — | V | IOH = -400 µA, VCC = 4.5V |
| | VOH2 | | VCC - 0.2 | — | — | V | IOH = -100 µA, VCC = 2.5V |
| D5 | ILI | Input leakage current | — | — | ±1 | µA | VIN = VSS or VCC |
| D6 | ILO | Output leakage current | — | — | ±1 | µA | VOUT = VSS or VCC |
| D7 | CIN, COUT | Pin capacitance (all inputs/outputs) | — | — | 7 | pF | VIN/VOUT = 0V **(Note 1)**<br>TA = 25°C, FCLK = 1 MHz |
| D8 | ICC write | Write current | — | — | 2 | mA | FCLK = 3 MHz, VCC = 5.5V |
| | | | — | 500 | — | µA | FCLK = 2 MHz, VCC = 2.5V |
| D9 | ICC read | Read current | — | — | 1 | mA | FCLK = 3 MHz, VCC = 5.5V |
| | | | — | — | 500 | µA | FCLK = 2 MHz, VCC = 3.0V |
| | | | — | 100 | — | µA | FCLK = 2 MHz, VCC = 2.5V |
| D10 | ICCS | Standby current | — | — | 1 | µA | I-Temp<br>CLK = CS = 0V<br>ORG = DI = VSS or VCC<br>**(Note 2) (Note 3)** |
| | | | — | — | 5 | µA | E-Temp<br>CLK = CS = 0V<br>ORG = DI = VSS or VCC<br>**(Note 2) (Note 3)** |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** ORG pin not available on ‘A’ or ‘B’ versions.

**3:** Ready/$\overline{\text{Busy}}$ status must be cleared from DO; see **Section 3.4 “Data Out (DO)”**.

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| All parameters apply over the specified ranges unless otherwise noted. | | | Industrial (I): TA = -40°C to +85°C, VCC = +1.8V TO +5.5V<br>Extended (E): TA = -40°C to +125°C, VCC = +2.5V TO +5.5V | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Parameter** | **Min.** | **Typ** | **Max.** | **Units** | **Conditions** |
| D11 | VPOR | VCC voltage detect | — | 1.5 | — | V | (Note 1)<br>93AA46A/B/C, 93LC46A/B/C |
| | | | — | 3.8 | — | V | (Note 1)<br>93C46A/B/C |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** ORG pin not available on 'A' or 'B' versions.

**3:** Ready/$\overline{\text{Busy}}$ status must be cleared from DO; see **Section 3.4 "Data Out (DO)"**.

**TABLE 1-2: AC CHARACTERISTICS**

| All parameters apply over the specified ranges unless otherwise noted. | | | Industrial (I): TA = -40°C to +85°C, VCC = +1.8V TO +5.5V<br>Extended (E): TA = -40°C to +125°C, VCC = +2.5V TO +5.5V | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Parameter** | **Min.** | **Max.** | **Units** | **Conditions** |
| A1 | FCLK | Clock frequency | — | 3 | MHz | 4.5V ≤ VCC < 5.5V, 93XX46C only |
| | | | — | 2 | MHz | 2.5V ≤ VCC < 5.5V |
| | | | — | 1 | MHz | 1.8V ≤ VCC < 2.5V |
| A2 | TCKH | Clock high time | 200 | — | ns | 4.5V ≤ VCC < 5.5V, 93XX46C only |
| | | | 250 | — | ns | 2.5V ≤ VCC < 5.5V |
| | | | 450 | — | ns | 1.8V ≤ VCC < 2.5V |
| A3 | TCKL | Clock low time | 100 | — | ns | 4.5V ≤ VCC < 5.5V, 93XX46C only |
| | | | 200 | — | ns | 2.5V ≤ VCC < 5.5V |
| | | | 450 | — | ns | 1.8V ≤ VCC < 2.5V |
| A4 | TCSS | Chip Select setup time | 50 | — | ns | 4.5V ≤ VCC < 5.5V |
| | | | 100 | — | ns | 2.5V ≤ VCC < 4.5V |
| | | | 250 | — | ns | 1.8V ≤ VCC < 2.5V |
| A5 | TCSH | Chip Select hold time | 0 | — | ns | 1.8V ≤ VCC < 5.5V |
| A6 | TCSL | Chip Select low time | 250 | — | ns | 1.8V ≤ VCC < 5.5V |
| A7 | TDIS | Data input setup time | 50 | — | ns | 4.5V ≤ VCC < 5.5V, 93XX46C only |
| | | | 100 | — | ns | 2.5V ≤ VCC < 5.5V |
| | | | 250 | — | ns | 1.8V ≤ VCC < 2.5V |
| A8 | TDIH | Data input hold time | 50 | — | ns | 4.5V ≤ VCC < 5.5V, 93XX46C only |
| | | | 100 | — | ns | 2.5V ≤ VCC < 5.5V |
| | | | 250 | — | ns | 1.8V ≤ VCC < 2.5V |
| A9 | TPD | Data output delay time | — | 200 | ns | 4.5V ≤ VCC < 5.5V, CL = 100 pF |
| | | | — | 250 | ns | 2.5V ≤ VCC < 4.5V, CL = 100 pF |
| | | | — | 400 | ns | 1.8V ≤ VCC < 2.5V, CL = 100 pF |
| A10 | TCZ | Data output disable time | — | 100 | ns | 4.5V ≤ VCC < 5.5V (Note 1) |
| | | | — | 200 | ns | 1.8V ≤ VCC < 4.5V (Note 1) |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** This parameter is not tested but ensured by characterization.


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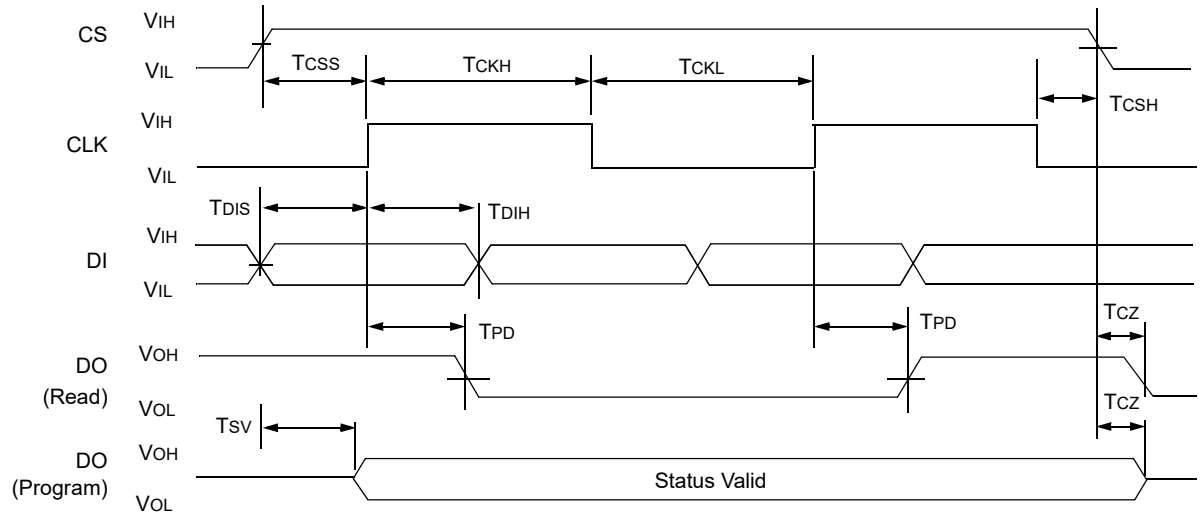
| All parameters apply over the specified ranges unless otherwise noted. | | | Industrial (I): TA = -40°C to +85°C, VCC = +1.8V TO +5.5V<br>Extended (E): TA = -40°C to +125°C, VCC = +2.5V TO +5.5V | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Parameter** | **Min.** | **Max.** | **Units** | **Conditions** |
| A11 | TSV | Status valid time | — | 200 | ns | 4.5V ≤ VCC < 5.5V, CL = 100 pF |
| | | | — | 300 | ns | 2.5V ≤ VCC < 4.5V, CL = 100 pF |
| | | | — | 500 | ns | 1.8V ≤ VCC < 2.5V, CL = 100 pF |
| A12 | TWC | Program cycle time | — | 6 | ms | Erase/Write mode (AA and LC versions) |
| A13 | TWC | | — | 2 | ms | Erase/Write mode (93C versions) |
| A14 | TEC | | — | 6 | ms | ERAL mode, 4.5V ≤ VCC ≤ 5.5V |
| A15 | TWL | | — | 15 | ms | WRAL mode, 4.5V ≤ VCC ≤ 5.5V |
| A16 | — | Endurance | 1M | — | cycles | 25°C, VCC = 5.0V, **(Note 2)** |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** This parameter is not tested but ensured by characterization.

**FIGURE 1-1: SYNCHRONOUS DATA TIMING**




**Note:** TSV is relative to CS.

**TABLE 1-3: INSTRUCTION SET FOR X16 ORGANIZATION (93XX46B OR 93XX46C WITH ORG = 1)**

| Instruction | SB | Opcode | Address | | | | | | Data In | Data Out | Req. CLK Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ERASE | 1 | 11 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/$\overline{BSY}$) | 9 |
| ERAL | 1 | 00 | 1 | 0 | X | X | X | X | — | (RDY/$\overline{BSY}$) | 9 |
| EWDS | 1 | 00 | 0 | 0 | X | X | X | X | — | High-Z | 9 |
| EWEN | 1 | 00 | 1 | 1 | X | X | X | X | — | High-Z | 9 |
| READ | 1 | 10 | A5 | A4 | A3 | A2 | A1 | A0 | — | D15 - D0 | 25 |
| WRITE | 1 | 01 | A5 | A4 | A3 | A2 | A1 | A0 | D15 - D0 | (RDY/$\overline{BSY}$) | 25 |
| WRAL | 1 | 00 | 0 | 1 | X | X | X | X | D15 - D0 | (RDY/$\overline{BSY}$) | 25 |

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**TABLE 1-4: INSTRUCTION SET FOR X8 ORGANIZATION (93XX46A OR 93XX46C WITH ORG = 0)**

| Instruction | SB | Opcode | Address | | | | | | | Data In | Data Out | Req. CLK Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ERASE | 1 | 11 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/$\overline{\text{BSY}}$) | 10 |
| ERAL | 1 | 00 | 1 | 0 | X | X | X | X | X | — | (RDY/$\overline{\text{BSY}}$) | 10 |
| EWDS | 1 | 00 | 0 | 0 | X | X | X | X | X | — | High-Z | 10 |
| EWEN | 1 | 00 | 1 | 1 | X | X | X | X | X | — | High-Z | 10 |
| READ | 1 | 10 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D7 - D0 | 18 |
| WRITE | 1 | 01 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 - D0 | (RDY/$\overline{\text{BSY}}$) | 18 |
| WRAL | 1 | 00 | 0 | 1 | X | X | X | X | X | D7 - D0 | (RDY/$\overline{\text{BSY}}$) | 18 |


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## 2.0 FUNCTIONAL DESCRIPTION

When the ORG pin (93XX46C) is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an erase/write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

### 2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

| **Note:** | When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active-high. |
|---|---|

### 2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the read operation if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

### 2.3 Data Protection

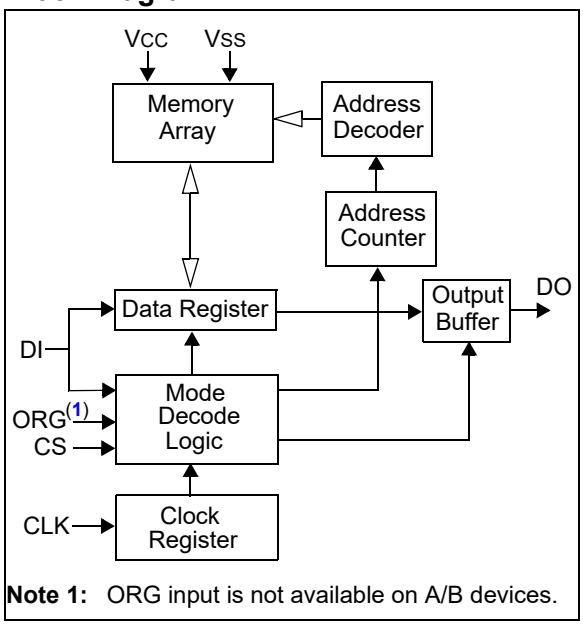
All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for ‘93AA’ and ‘93LC’ devices or 3.8V for ‘93C’ devices.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

| **Note:** | For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin. |
|---|---|

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

### Block Diagram




**Note 1:** ORG input is not available on A/B devices.

## 2.4 Erase

The ERASE instruction forces all data bits of the specified address to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on '93C' devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

| **Note:** | After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO. |
|---|---|

**FIGURE 2-1: ERASE TIMING FOR 93AA AND 93LC DEVICES**

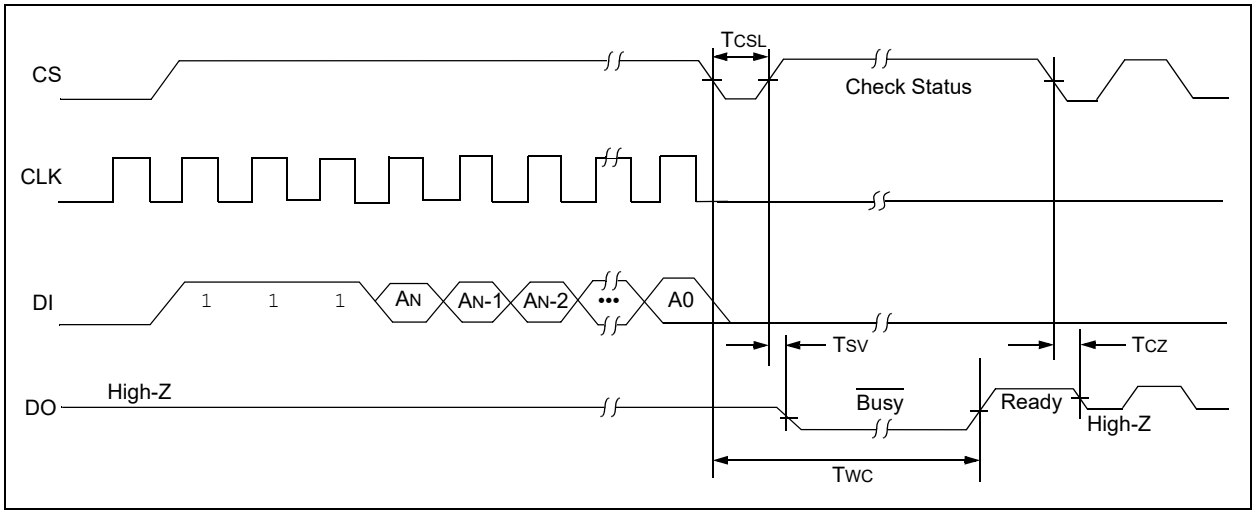
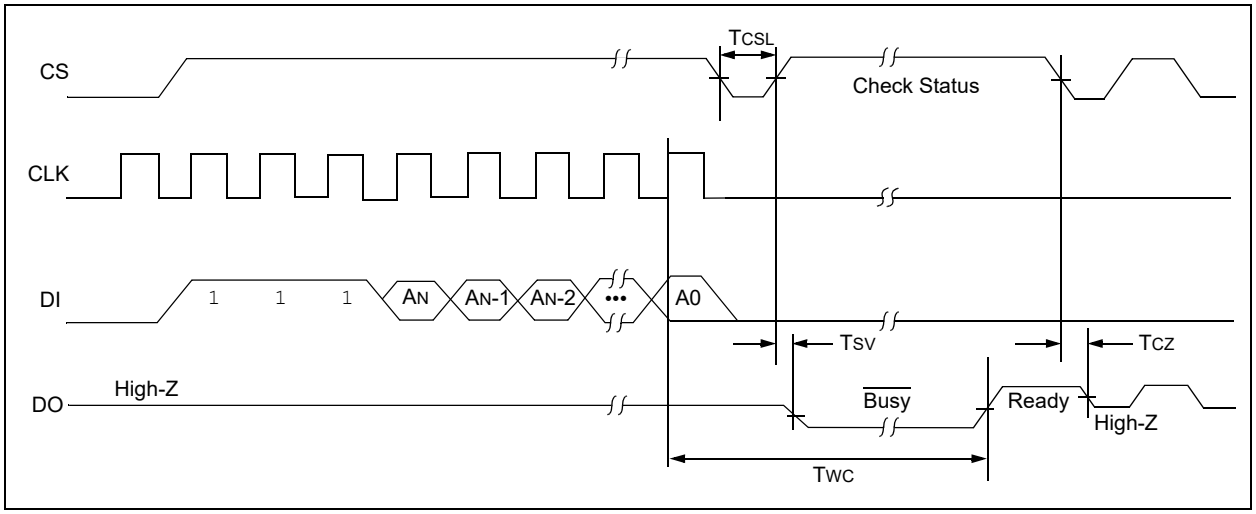



**FIGURE 2-2: ERASE TIMING FOR 93C DEVICES**





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## 2.5 Erase All (ERAL)

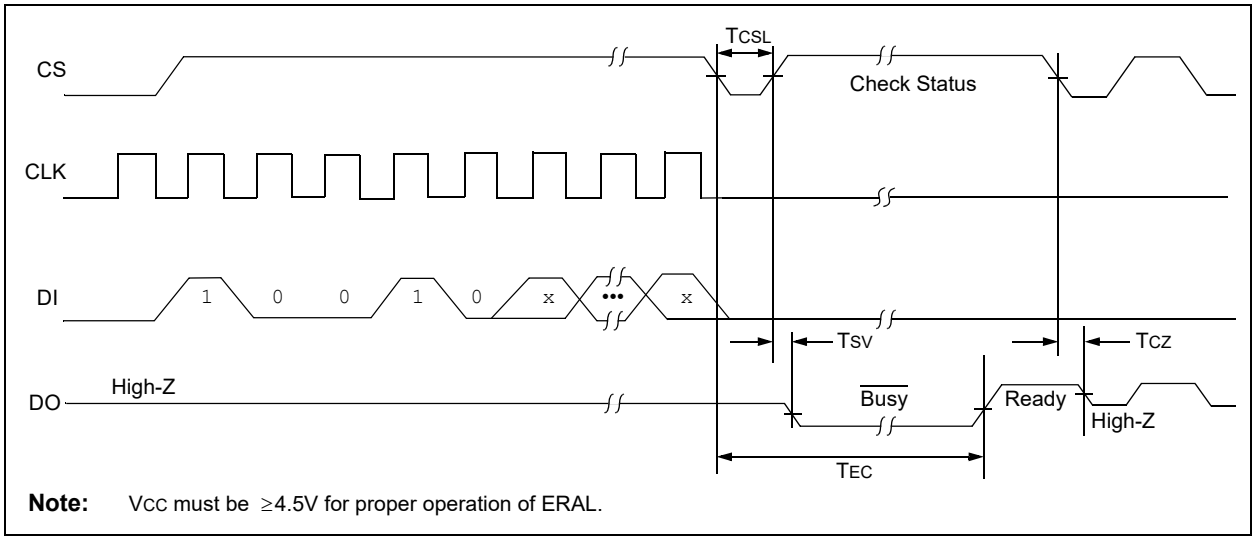
The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on '93C' devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low ($T_{CSL}$).

| | |
|---|---|
| **Note:** | After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO. |

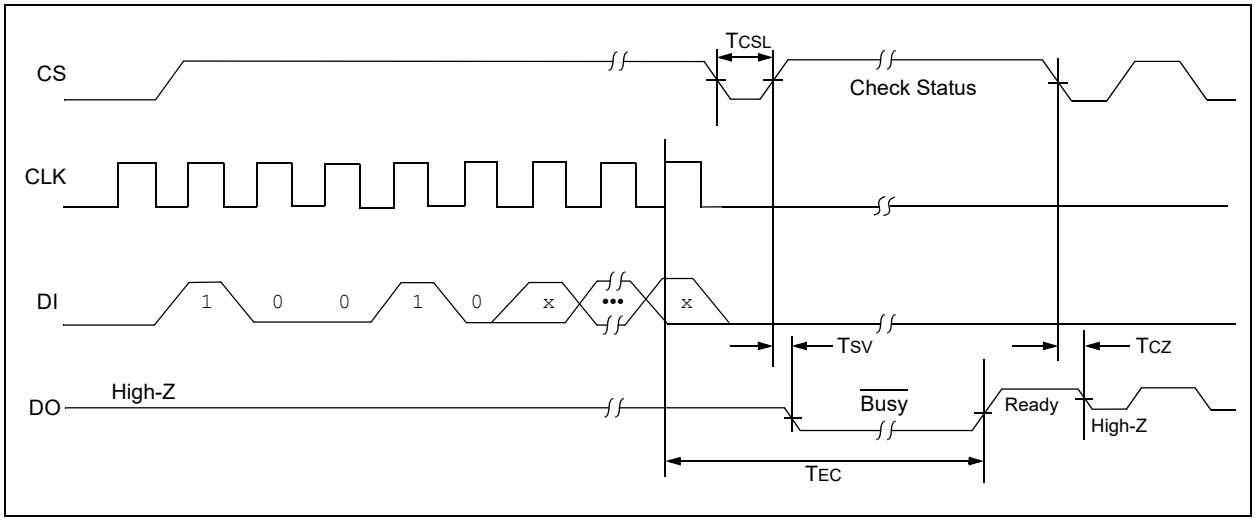
$V_{CC}$ must be ≥4.5V for proper operation of ERAL.

**FIGURE 2-3: ERAL TIMING FOR 93AA AND 93LC DEVICES**




**Note:** $V_{CC}$ must be ≥4.5V for proper operation of ERAL.

**FIGURE 2-4: ERAL TIMING FOR 93C DEVICES**



## 2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93XX46A/B/C powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

**FIGURE 2-5: EWDS TIMING**

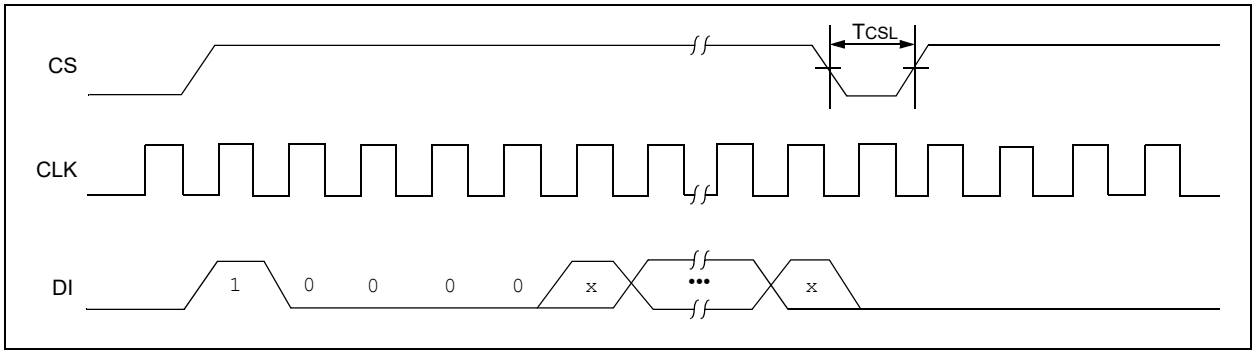
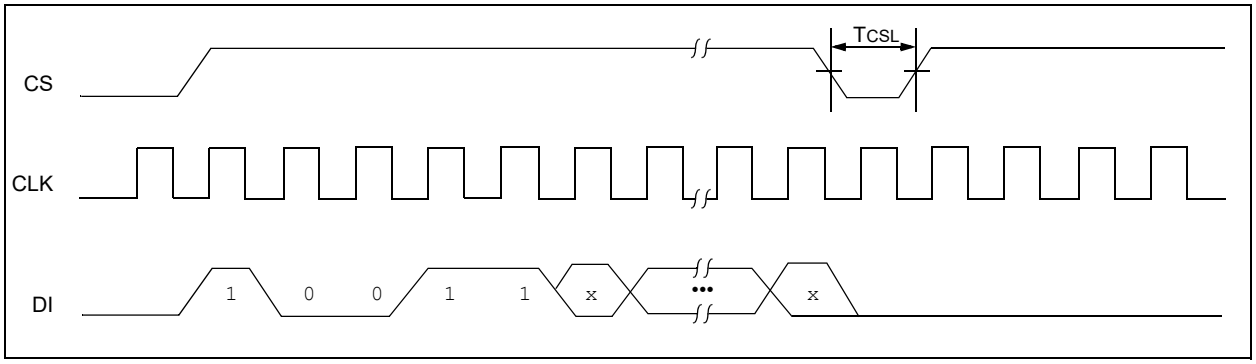



**FIGURE 2-6: EWEN TIMING**

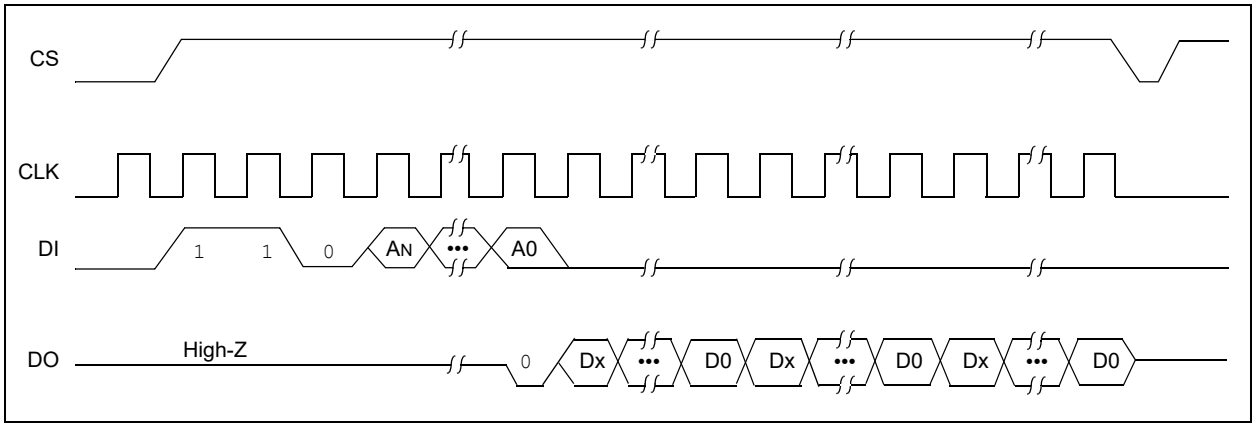



## 2.7 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (if ORG pin is low or A-version devices) or 16-bit (if ORG pin is high or B-version devices) output string.

The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

**FIGURE 2-7: READ TIMING**





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## 2.8 Write

The WRITE instruction is followed by 8 bits (if ORG is low or A-version devices) or 16 bits (if ORG pin is high or B-version devices) of data, which are written into the specified address. For 93AA46A/B/C and 93LC46A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C46A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low ($T_{CSL}$). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

| **Note:** | After the Write cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO. |
|---|---|

**FIGURE 2-8: WRITE TIMING FOR 93AA AND 93LC DEVICES**

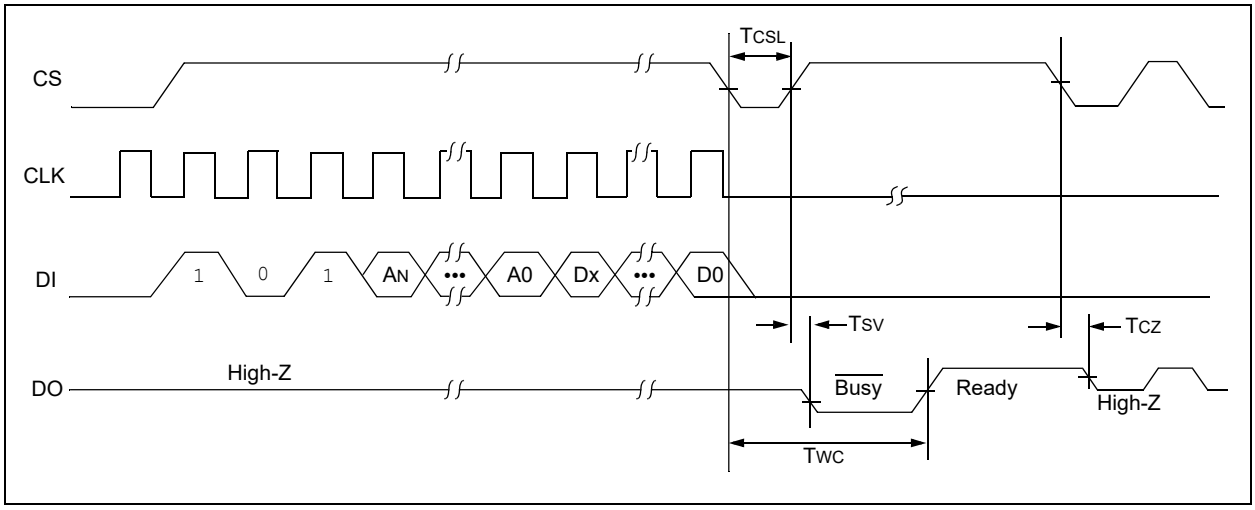
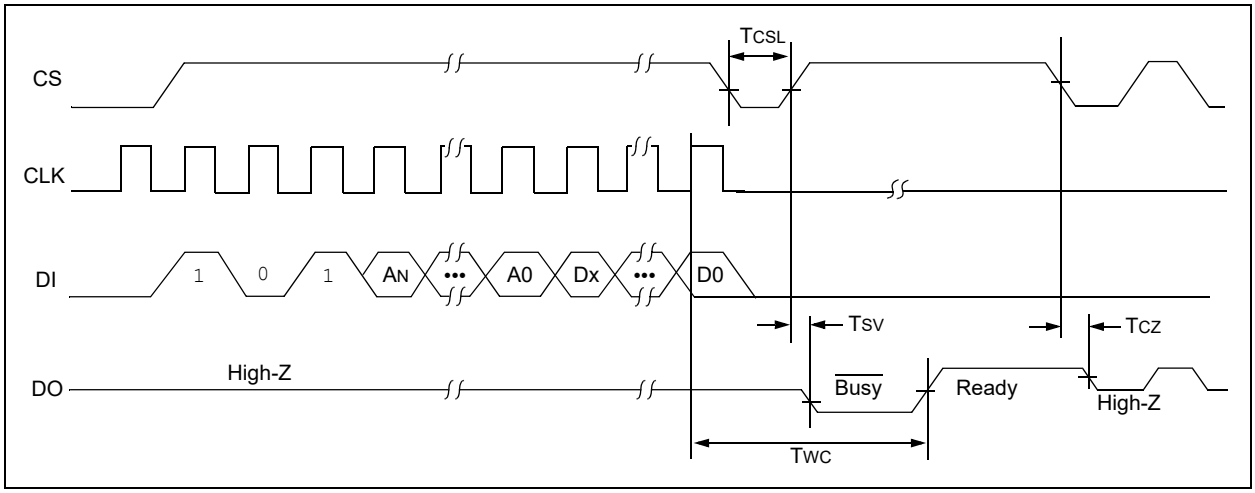



**FIGURE 2-9: WRITE TIMING FOR 93C DEVICES**



## 2.9 Write All (WRAL)

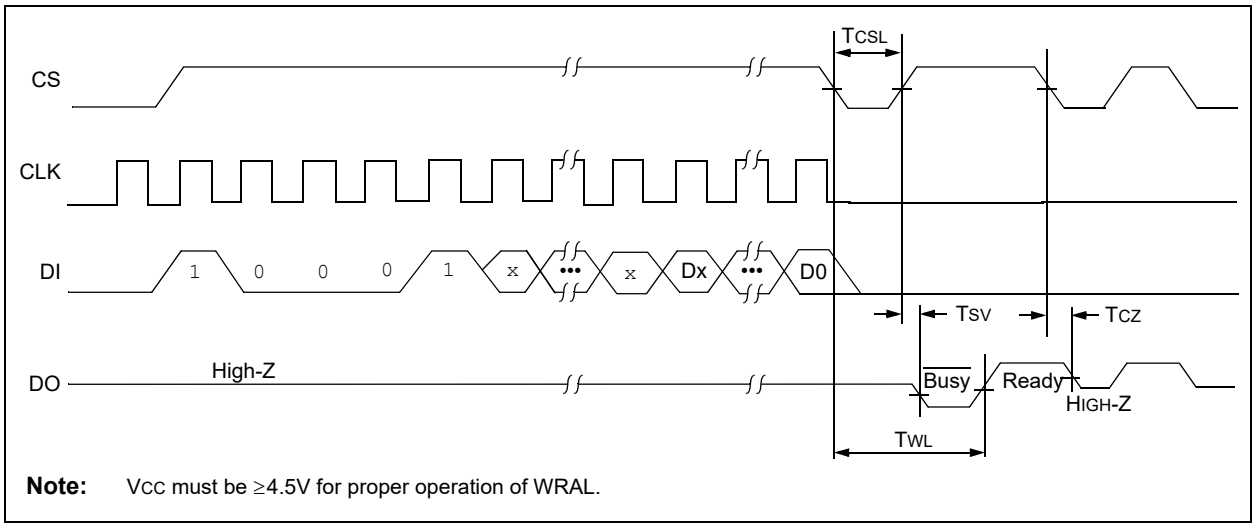
The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AA46A/B/C and 93LC46A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C46A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

| **Note:** | After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO. |
|---|---|

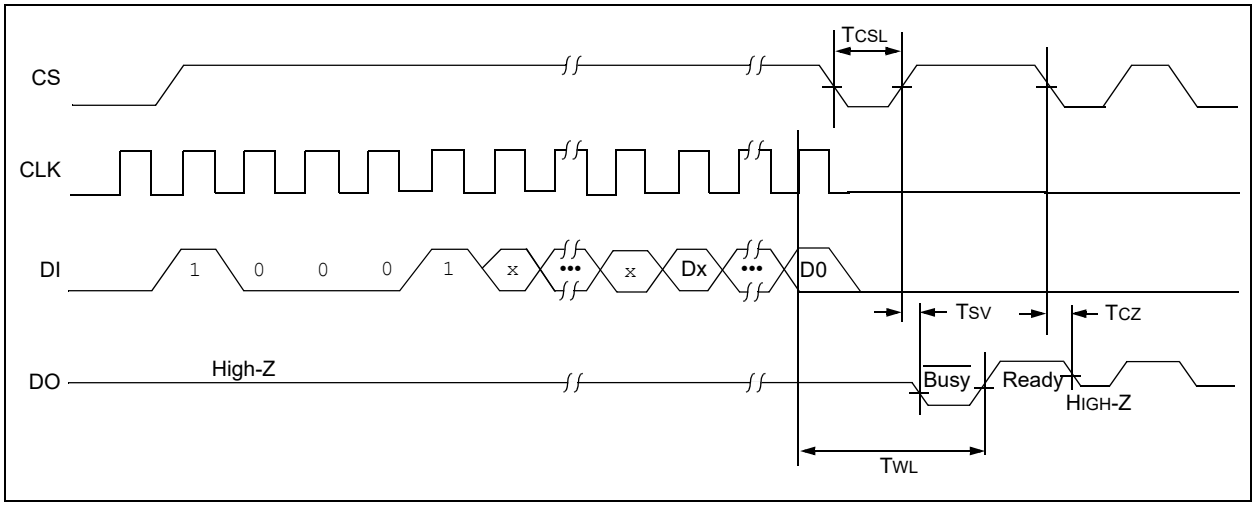
VCC must be ≥4.5V for proper operation of WRAL.

**FIGURE 2-10: WRAL TIMING FOR 93AA AND 93LC DEVICES**




**Note:** VCC must be ≥4.5V for proper operation of WRAL.

**FIGURE 2-11: WRAL TIMING FOR 93C DEVICES**





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## 3.0 PIN DESCRIPTIONS

**TABLE 3-1: PIN DESCRIPTIONS**

| Name | PDIP | SOIC | TSSOP | MSOP | DFN(1) | TDFN(1) | SOT-23 | Rotated SOIC | Function |
|---|---|---|---|---|---|---|---|---|---|
| CS | 1 | 1 | 1 | 1 | 1 | 1 | 5 | 3 | Chip Select |
| CLK | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 4 | Serial Clock |
| DI | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 5 | Data In |
| DO | 4 | 4 | 4 | 4 | 4 | 4 | 1 | 6 | Data Out |
| Vss | 5 | 5 | 5 | 5 | 5 | 5 | 2 | 7 | Ground |
| ORG/NC | 6 | 6 | 6 | 6 | 6 | 6 | — | 8 | Organization/93XX46C<br>No Internal Connection/<br>93XX46A/B |
| NC | 7 | 7 | 7 | 7 | 7 | 7 | — | 1 | No Internal Connection |
| VCC | 8 | 8 | 8 | 8 | 8 | 8 | 6 | 2 | Power Supply |

**Note 1:** The exposed pad on the DFN/TDFN packages can be connected to VSS or left floating.

### 3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle that is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

### 3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a host device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling host freedom in preparing opcode, address and data.

CLK is a “don't care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become “don't care” inputs waiting for a new Start condition to be detected.

### 3.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

### 3.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides Ready/$\overline{\text{Busy}}$ status information during erase and write cycles. Ready/$\overline{\text{Busy}}$ status information is available on the DO pin if CS is brought high after being low for minimum Chip Select low time (TCSL) and an erase or write operation has been initiated.

The Status signal is not available on DO if CS is held low during the entire erase or write cycle. In this case, DO is in the High-Z mode. If status is checked after the erase/write cycle, the data line will be high to indicate the device is ready.

| **Note:** | After a programming cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO. |
|---|---|

### 3.5 Organization (ORG)

When the ORG pin is connected to VCC or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to VSS or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

93XX46A devices are always (x8) organization and 93XX46B devices are always (x16) organization.

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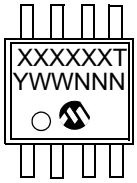
## 4.0 PACKAGING INFORMATION

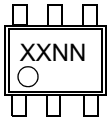
### 4.1 Package Marking Information

8-Lead MSOP (150 mil)

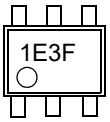



Example:

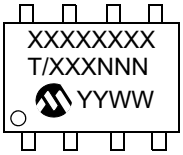
6-Lead SOT-23




Example:




8-Lead PDIP

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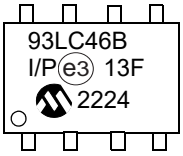
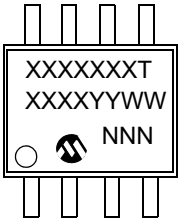



8-Lead SOIC

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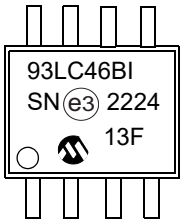
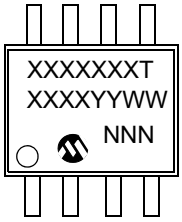
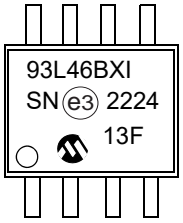



8-Lead Rotated SOIC

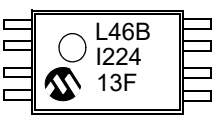



Example:




8-Lead TSSOP

Example:





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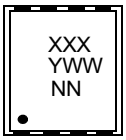
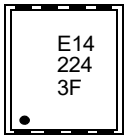
8-Lead 2x3 DFN




Example:

8-Lead 2x3 TDFN

Example:




| Part Number | 1st Line Marking Codes | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | TSSOP | MSOP | SOIC | Rotated SOIC | SOT-23 | | DFN | | TDFN | |
| | | | | | I Temp. | E Temp. | I Temp. | E Temp. | I Temp. | E Temp. |
| 93AA46A | A46A | 3A46AT | 93AA46AT | 93A46AXT | 1BNN | — | 301 | — | E01 | — |
| 93AA46B | A46B | 3A46BT | 93AA46BT | 93A46BXT | 1LNN | — | 311 | — | E11 | — |
| 93AA46C | A46C | 3A46CT | 93AA46CT | 93A46CXT | — | — | 321 | — | E21 | — |
| 93LC46A | L46A | 3L46AT | 93LC46AT | 93L46AXT | 1ENN | 1FNN | 304 | — | E04 | E05 |
| 93LC46B | L46B | 3L46BT | 93LC46BT | 93L46BXT | 1PNN | 1RNN | 314 | — | E14 | E15 |
| 93LC46C | L46C | 3L46CT | 93LC46CT | 93L46CXT | — | — | 324 | — | E24 | E25 |
| 93C46A | C46A | 3C46AT | — | — | 1HNN | 1JNN | 307 | — | E07 | E08 |
| 93C46B | C46B | 3C46BT | — | — | 1TNN | 1UNN | 317 | — | E17 | E18 |
| 93C46C | C46C | 3C46CT | — | — | — | — | 327 | — | E27 | E28 |

| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note**: For very small packages with no room for the RoHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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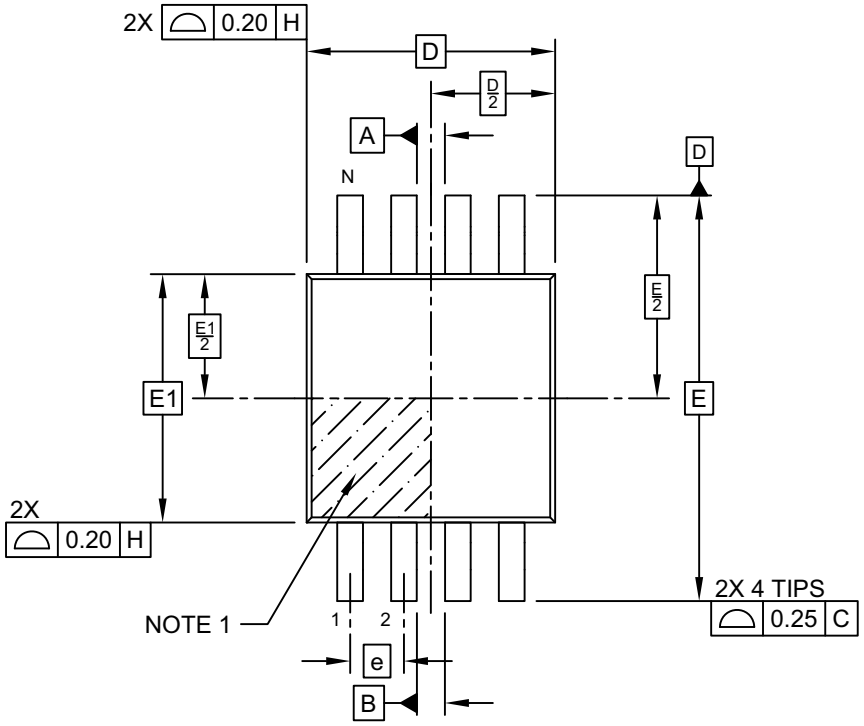
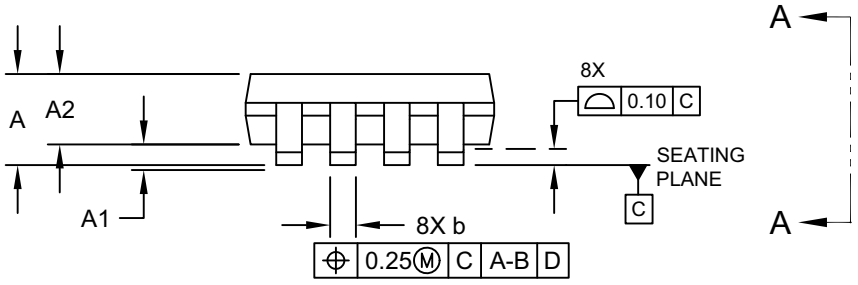
### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

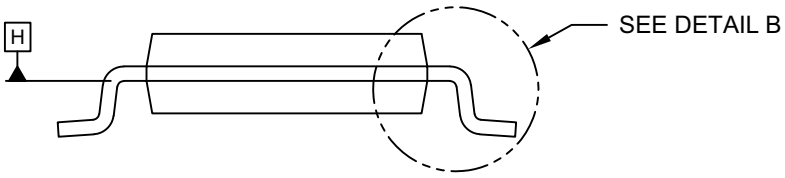
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW




VIEW A–A

Microchip Technology Drawing C04-111-MS Rev D Sheet 1 of 2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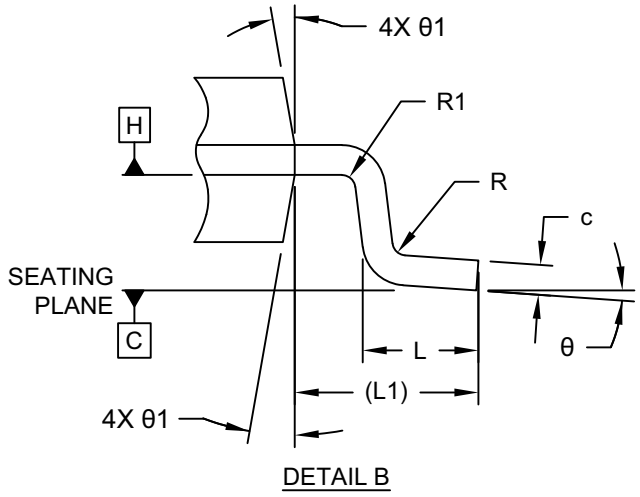
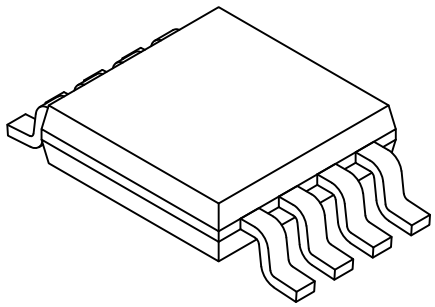
## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Overall Length | D | | 3.00 BSC | |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Terminal Width | b | 0.22 | – | 0.40 |
| Terminal Thickness | c | 0.08 | – | 0.23 |
| Terminal Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev D Sheet 2 of 2

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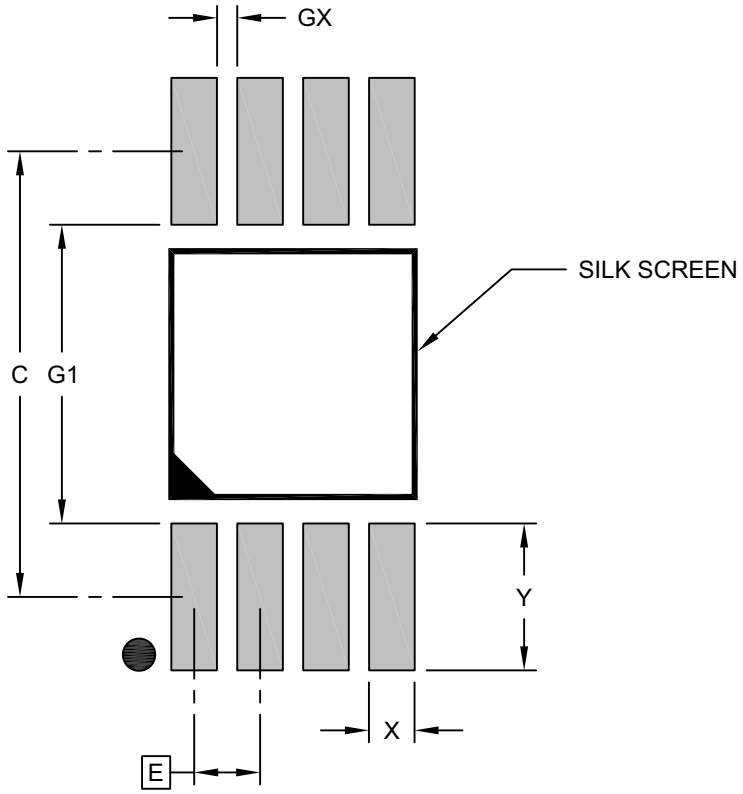
### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 4.40 | |
| Contact Pad Width (X8) | X | | | 0.45 |
| Contact Pad Length (X8) | Y | | | 1.45 |
| Contact Pad to Contact Pad (X4) | G1 | 2.95 | | |
| Contact Pad to Contact Pad (X6) | GX | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev D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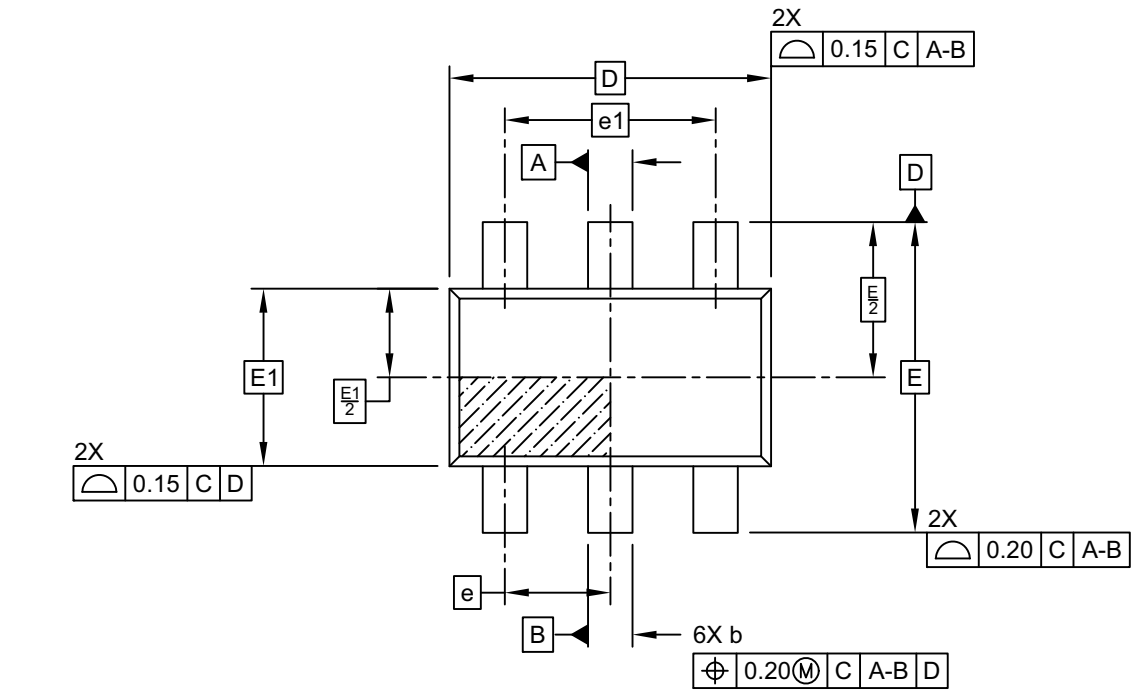
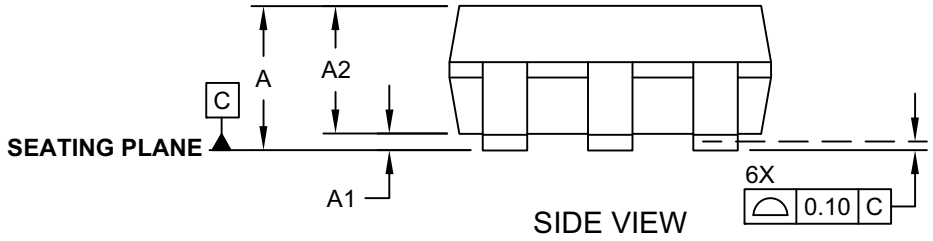
### 6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

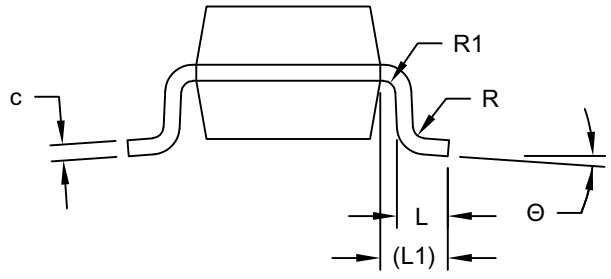
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

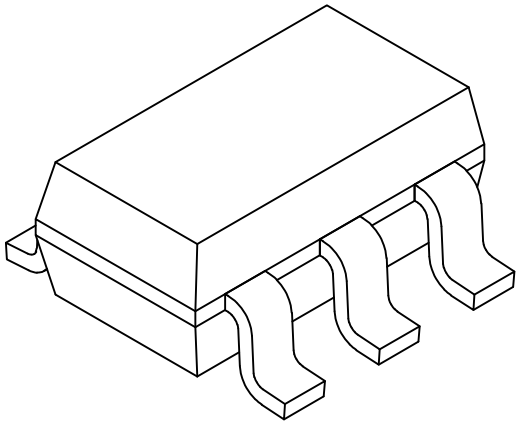



END VIEW

Microchip Technology Drawing C04-028D (OT) Sheet 1 of 2

### 6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 6 | |
| Pitch | e | | 0.95 BSC | |
| Outside lead pitch | e1 | | 1.90 BSC | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | 1.15 | 1.30 |
| Standoff | A1 | 0.00 | - | 0.15 |
| Overall Width | E | | 2.80 BSC | |
| Molded Package Width | E1 | | 1.60 BSC | |
| Overall Length | D | | 2.90 BSC | |
| Foot Length | L | 0.30 | 0.45 | 0.60 |
| Footprint | L1 | | 0.60 REF | |
| Foot Angle | $\phi$ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028D (OT) Sheet 2 of 2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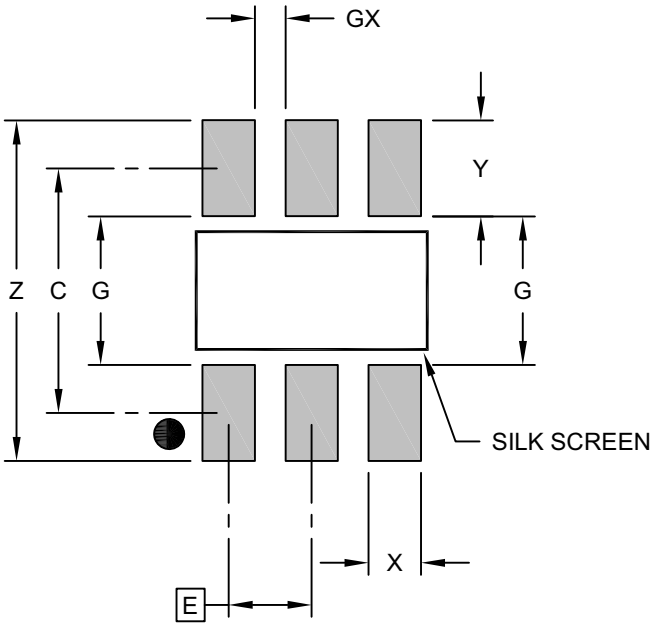
### 6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.95 BSC | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X3) | X | | | 0.60 |
| Contact Pad Length (X3) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028D (OT)

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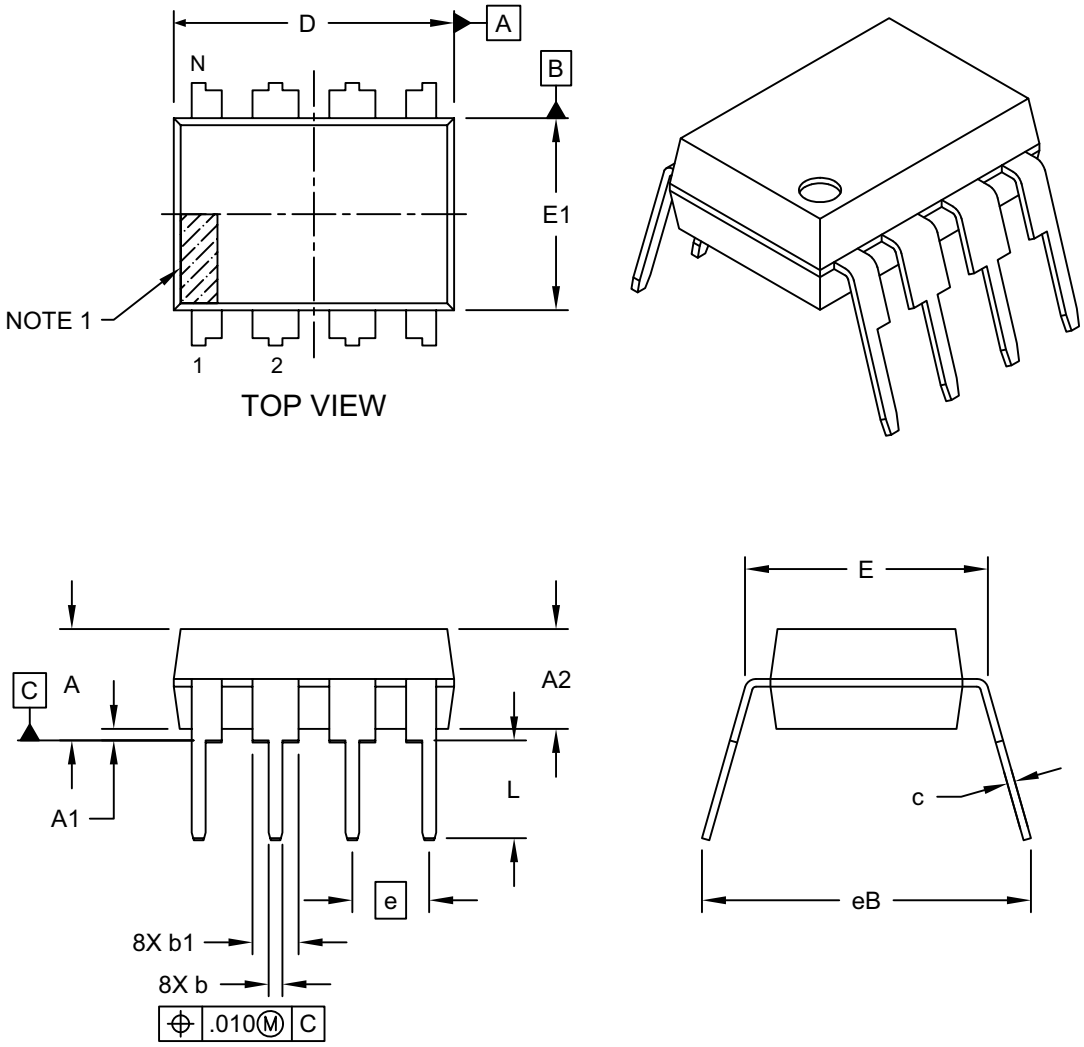
### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2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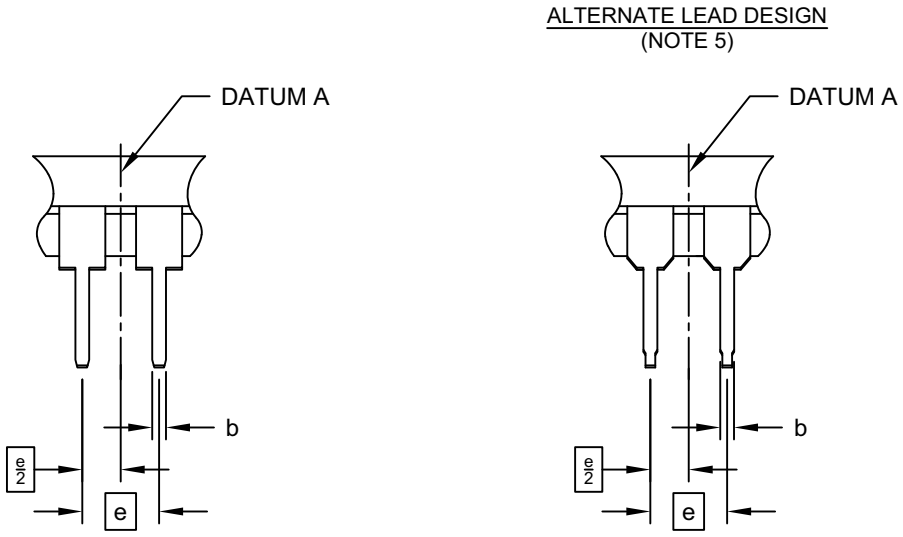
### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

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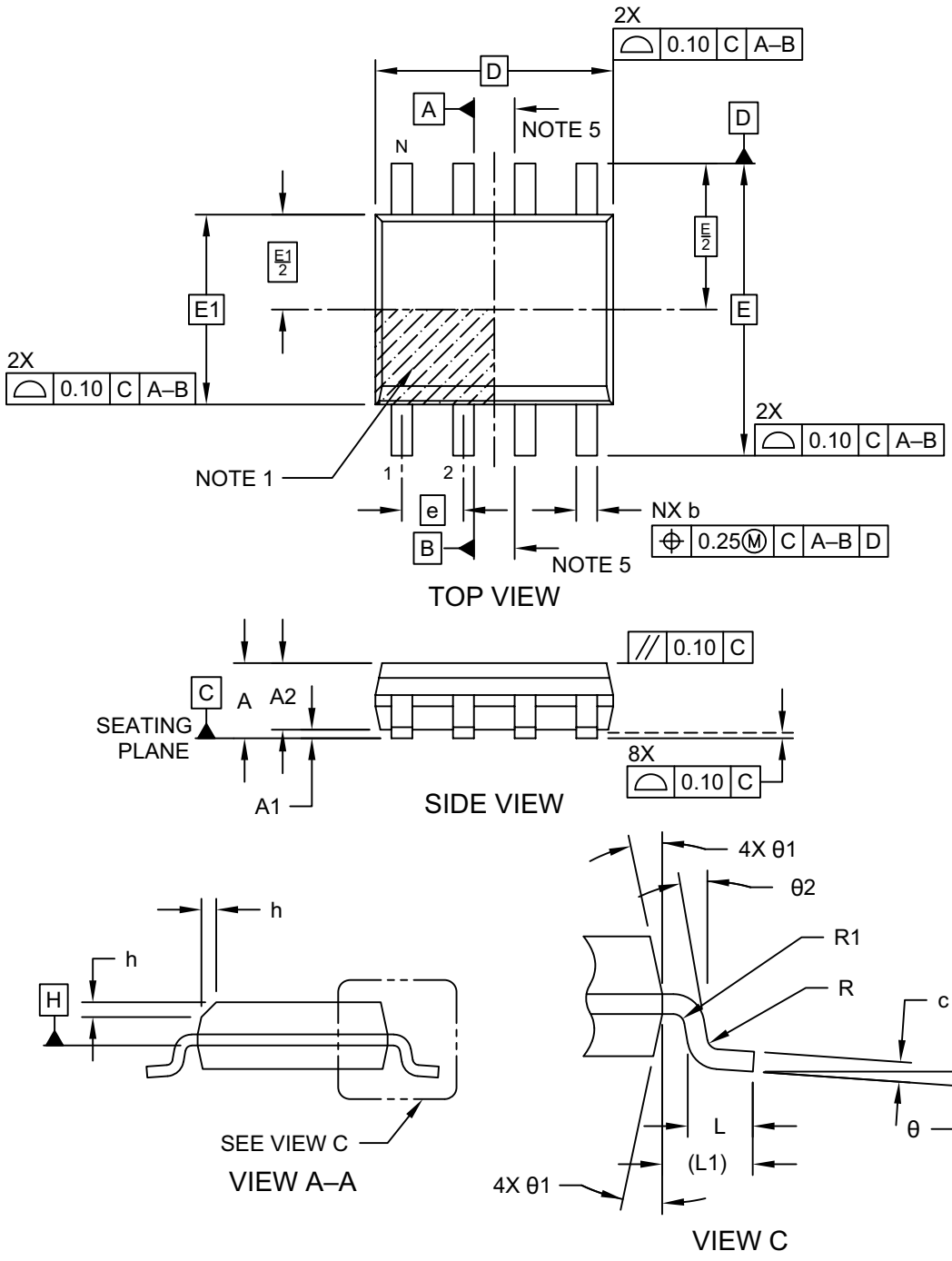
### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-057-SN Rev J Sheet 1 of 2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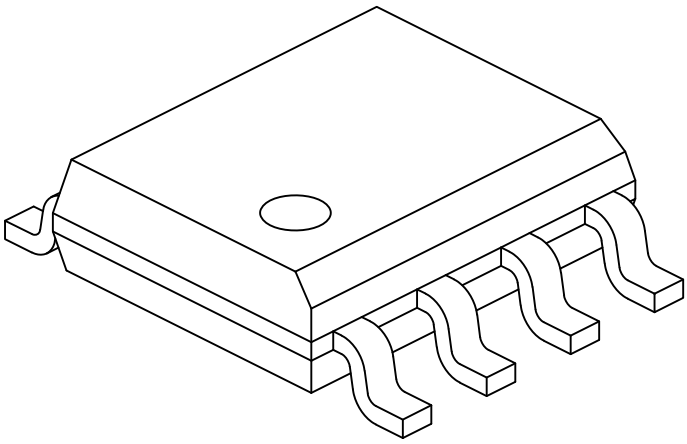
## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | - |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |
| Lead Angle | θ2 | 0° | – | 8° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev J Sheet 2 of 2

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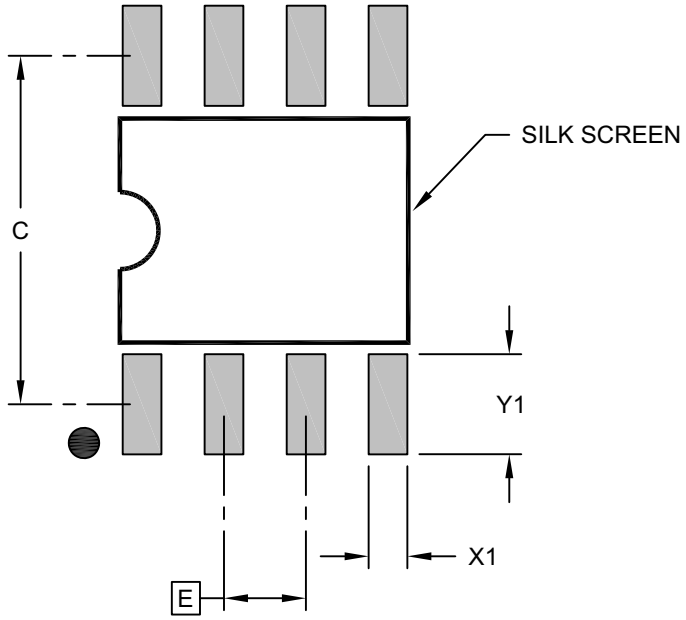
### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev J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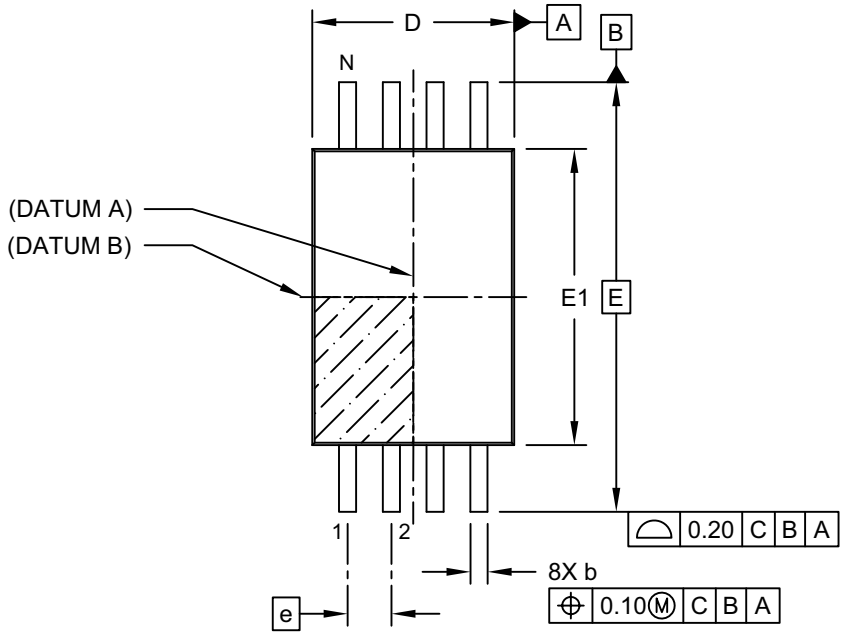
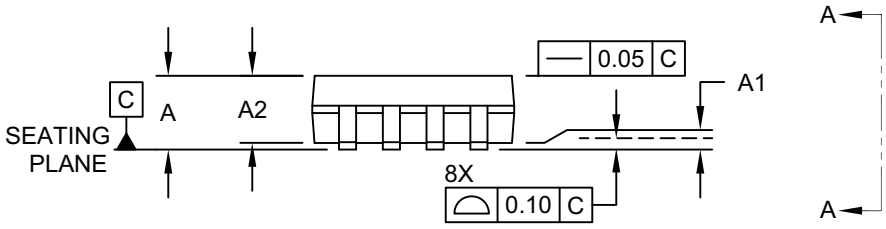
### 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

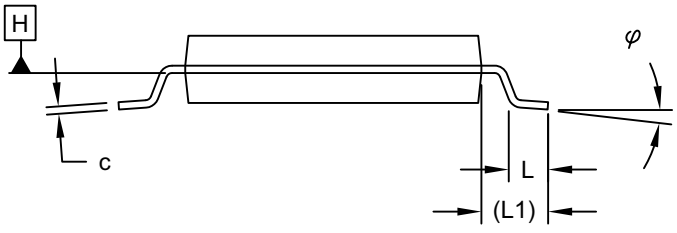
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

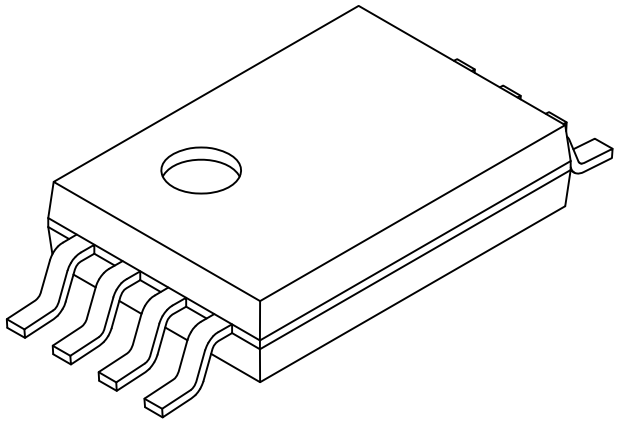



VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

### 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | - |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Overall Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Lead Thickness | c | 0.09 | - | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.19 | - | 0.30 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2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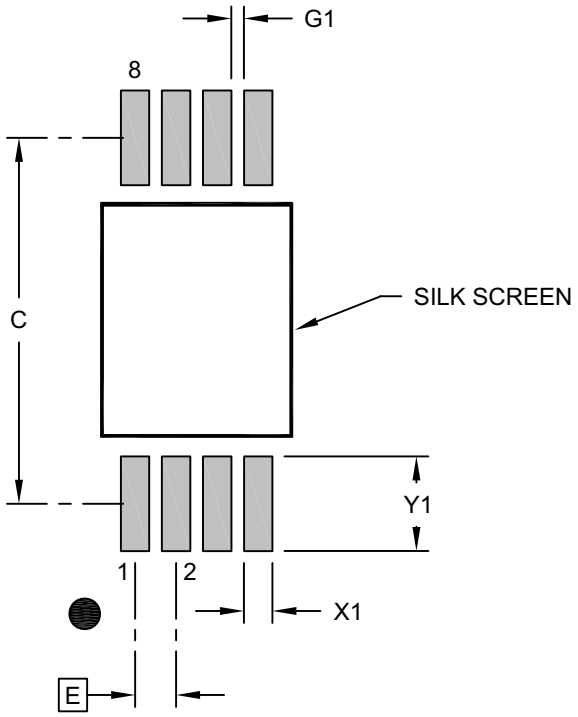
## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 5.80 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.50 |
| Contact Pad to Center Pad (X6) | G1 | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

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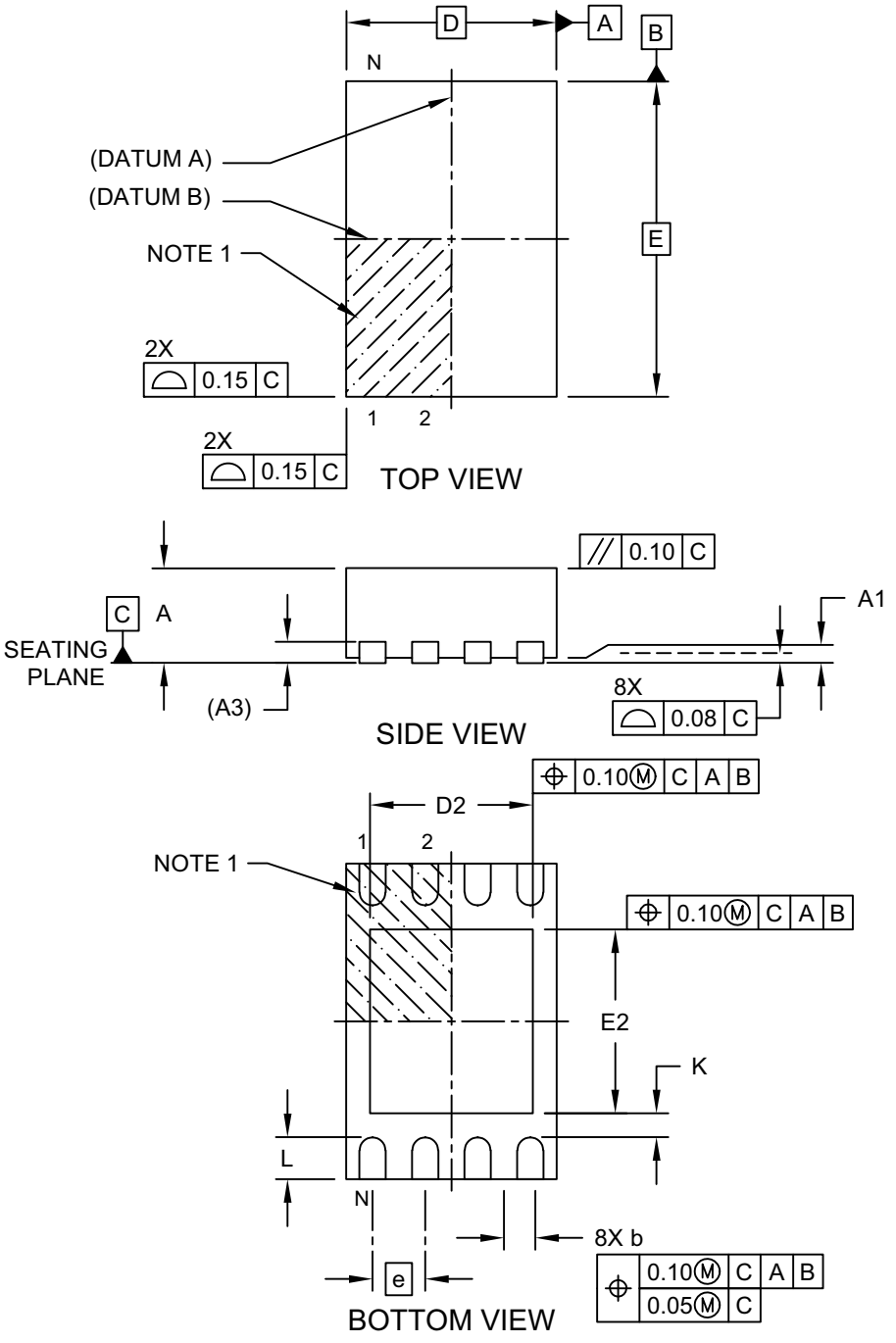
### 8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-123 Rev E Sheet 1 of 2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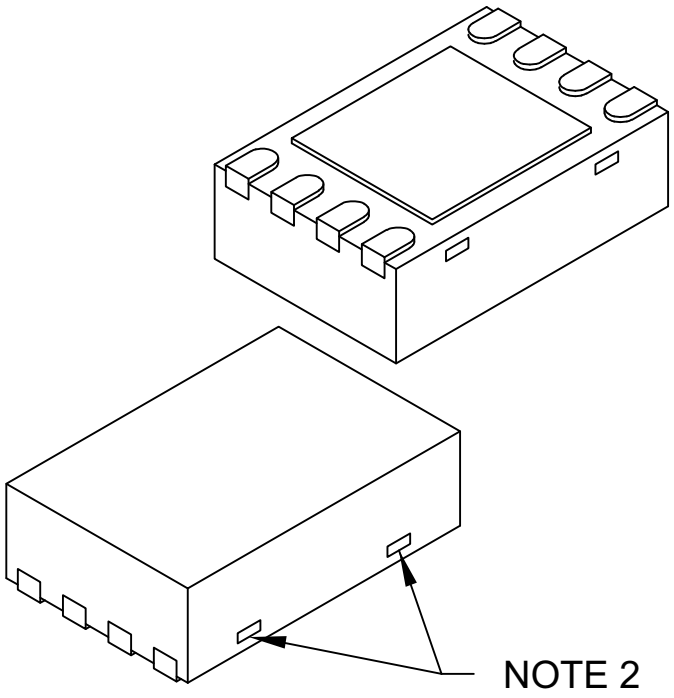
## 8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Exposed Pad Length | D2 | 1.30 | - | 1.55 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.50 | - | 1.75 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123 Rev E Sheet 2 of 2

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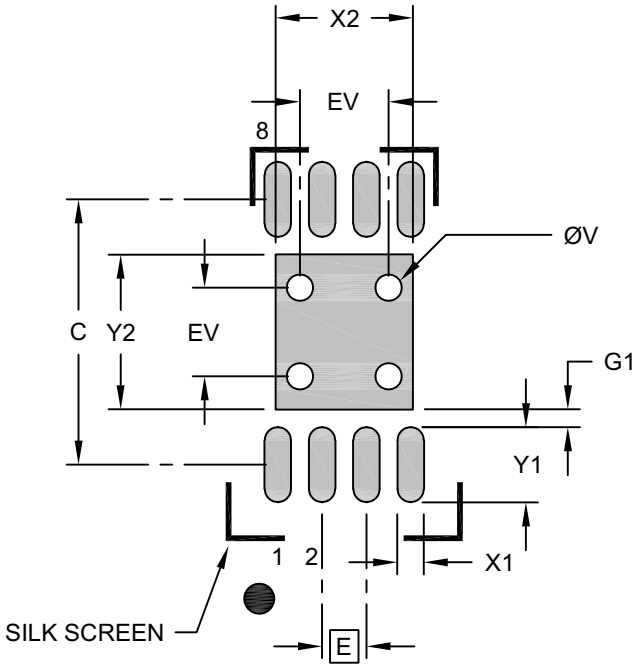
### 8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.55 |
| Optional Center Pad Length | Y2 | | | 1.75 |
| Contact Pad Spacing | C | | 3.00 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X8) | G1 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2123 Rev E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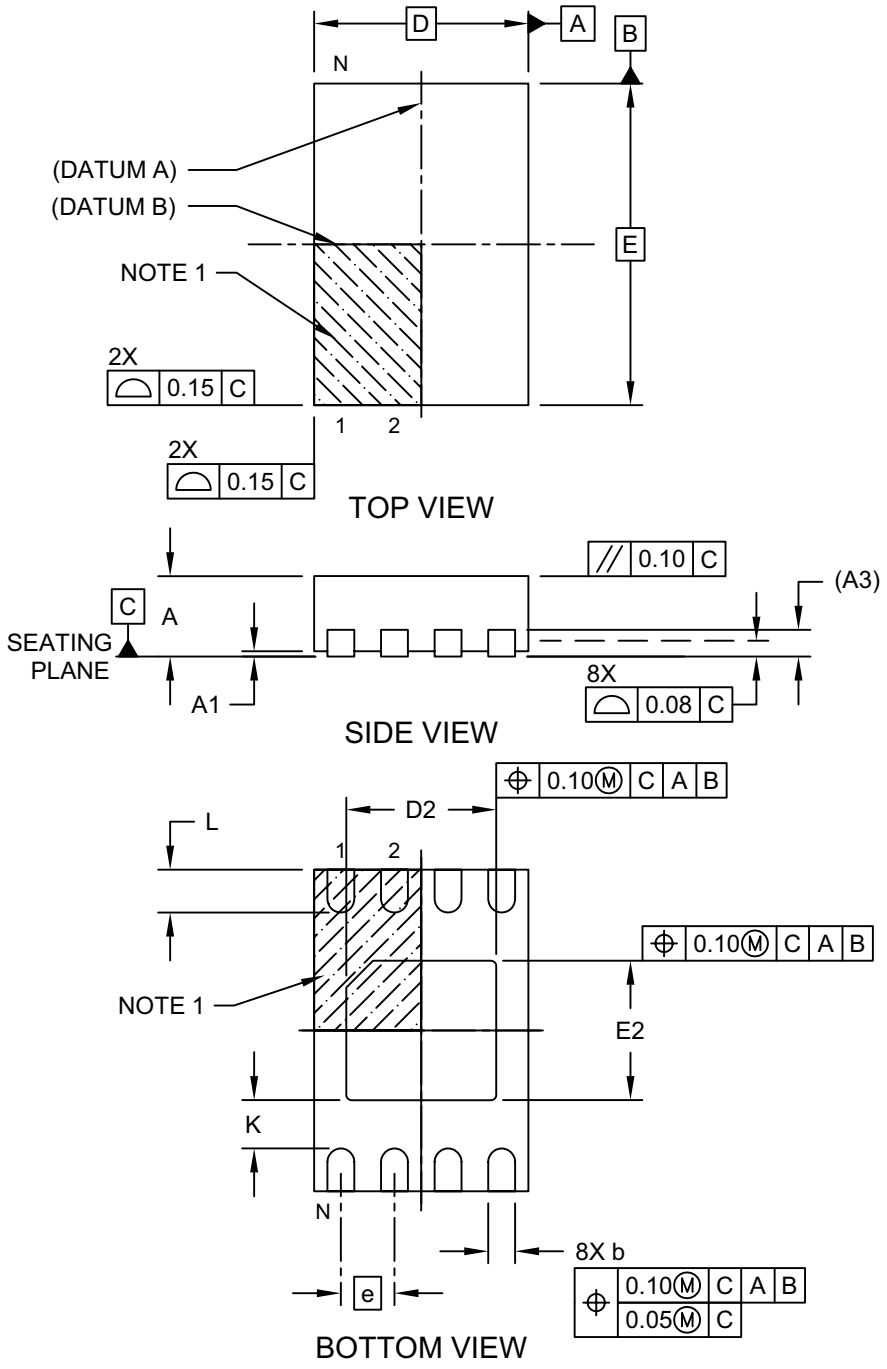
**8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]**
**With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)**

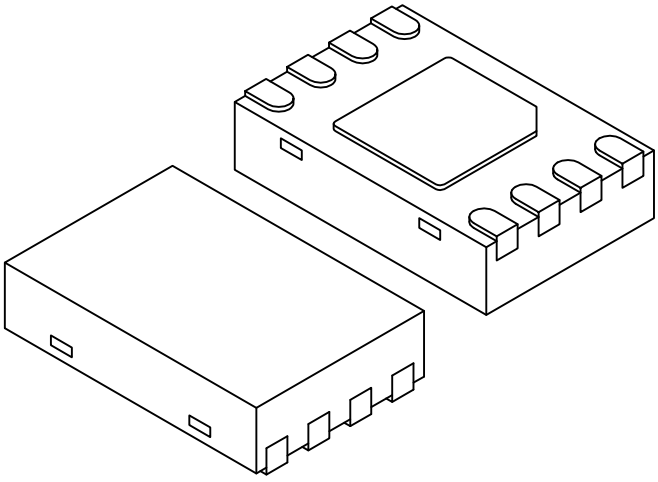
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.35 | 1.40 | 1.45 |
| Exposed Pad Width | E2 | 1.25 | 1.30 | 1.35 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2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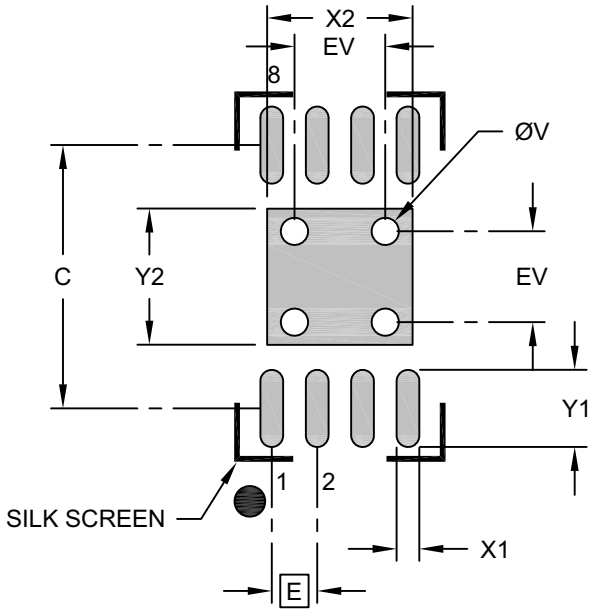
### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.60 |
| Optional Center Pad Length | Y2 | | | 1.50 |
| Contact Pad Spacing | C | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.25 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

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## APPENDIX A: REVISION HISTORY

### Revision L (07/2022)

Updated Package Drawings; Added Product Identification System for Automotive; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively.

### Revision K (06/2013)

Added E Temp to 93LC46C and 93C46C.

### Revision J (12/2011)

Added TDFN Package.

### Revision H (08/2010)

Added 8-Lead Rotated SOIC marking information; Revised Package Drawings; Revised Product ID System.

### Revision G (5/2008)

Revised Figures 2-1 through 2-4 and Figures 2-8 through 2-11; Revised Package Marking Information; Replaced Package Drawings; Revised Product ID section.

### Revision F (4/2005)

Added notes throughout.

### Revision E (3/2005)

Added DFN package.

### Revision D (12/2003)

Corrections to Section 1.0, Electrical Characteristics. Section 4.1, 6-Lead SOT-23 package to OT.


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**Technical support is available through the website at: http://microchip.com/support**

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## PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | X[1] | X | /XX |
|---|---|---|---|---|
| Device | Pinout | Tape and Reel | Temperature Range | Package |

| | | |
|---|---|---|
| **Device:** | 93AA46A: | 1-Kbit 1.8V Microwire Serial EEPROM |
| | 93AA46B: | 1-Kbit 1.8V Microwire Serial EEPROM |
| | 93AA46C: | 1-Kbit 1.8V Microwire Serial EEPROM w/ORG |
| | 93LC46A: | 1-Kbit 2.5V Microwire Serial EEPROM |
| | 93LC46B: | 1-Kbit 2.5V Microwire Serial EEPROM |
| | 93LC46C: | 1-Kbit 2.5V Microwire Serial EEPROM w/ORG |
| | 93C46A: | 1-Kbit 5.0V Microwire Serial EEPROM |
| | 93C46B: | 1-Kbit 5.0V Microwire Serial EEPROM |
| | 93C46C: | 1-Kbit 5.0V Microwire Serial EEPROM w/ORG |
| **Pinout:** | Blank = | Standard pinout |
| | X = | Rotated pinout (SOIC only) |
| **Tape and Reel:** | Blank = | Standard packaging |
| | T = | Tape and Reel[1] |
| **Temperature Range:** | I = | -40°C to +85°C (Industrial) |
| | E = | -40°C to +125°C (Extended) |
| **Package:** | MS = | Plastic Micro Small Outline - 8-lead (MSOP) |
| | OT = | Plastic Small Outline Transistor - 6-lead (SOT-23)(Tape & Reel only) |
| | P = | Plastic Dual In-Line - 300 mil Body, 8-lead (PDIP) |
| | SN = | Plastic Small Outline - Narrow 3.90 mm, 8-lead (SOIC) |
| | ST = | Plastic Thin Shrink Small Outline - 4.4 mm Body, 8-lead (TSSOP) |
| | MC = | Plastic Dual Flat, No Lead - 2x3x0.90 mm Body, 8-lead (DFN) |
| | MNY[2] = | Plastic Dual Flat, No Lead - 2x3x0.75 mm 8-lead (TDFN)(Tape & Reel only) |

**Examples:**

a) 93AA46C-I/P: 1-Kbit, 128x8 or 64x16 1.8V Serial EEPROM, Industrial Temp., PDIP package

b) 93AA46B-I/MS: 1-Kbit, 64x16 1.8V Serial EEPROM, Industrial Temp., MSOP package

c) 93AA46AT-I/OT: 1-Kbit, 128x8 1.8V Serial EEPROM, Industrial Temp., Tape and Reel, SOT-23 package

d) 93AA46CT-I/SN: 1-Kbit, 128x8 or 16x16 1.8V Serial EEPROM, Industrial Temp., Tape and Reel, SOIC package

a) 93LC46A-I/MS: 1-Kbit, 128x8 2.5V Serial EEPROM, Industrial Temp., MSOP package

b) 93LC46BT-I/OT: 1-Kbit, 64x16 2.5V Serial EEPROM, Industrial Temp., Tape and Reel, SOT-23 package

c) 93LC46B-I/ST: 1-Kbit, 64x16 2.5V Serial EEPROM, Industrial Temp., TSSOP package

d) 93LC46CT-E/MNY: 1-Kbit, 128x8 or 64x16 2.5V Serial EEPROM, Extended Temp., Tape and Reel, TDFN package

a) 93C46B-I/MS: 1-Kbit, 64x16 5.0V Serial EEPROM, Industrial Temp., MSOP package

b) 93C46C-I/MS: 1-Kbit, 128x8 or 64x16 5.0V Serial EEPROM, Industrial Temp., MSOP Package

c) 93C46CT-E/ST: 1-Kbit, 128x8 or 64x16, 5.0V Serial EEPROM, Extended Temp, TSSOP package

d) 93C46AXT-E/SN: 1-Kbit, 128x8 5.0V Serial EEPROM, Extended Temp., Tape and Reel, Rotated pinout, SOIC package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.


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## PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | X[1] | X | /XX | XXX[2,3] |
|---|---|---|---|---|---|
| Device | Pinout | Tape and Reel | Temperature Range | Package | Variant |

| | | |
|---|---|---|
| **Device:** | 93AA46A: | 1-Kbit 1.8V Microwire Serial EEPROM |
| | 93AA46B: | 1-Kbit 1.8V Microwire Serial EEPROM |
| | 93AA46C: | 1-Kbit 1.8V Microwire Serial EEPROM w/ORG |
| | 93LC46A: | 1-Kbit 2.5V Microwire Serial EEPROM |
| | 93LC46B: | 1-Kbit 2.5V Microwire Serial EEPROM |
| | 93LC46C: | 1-Kbit 2.5V Microwire Serial EEPROM w/ORG |
| | 93C46A: | 1-Kbit 5.0V Microwire Serial EEPROM |
| | 93C46B: | 1-Kbit 5.0V Microwire Serial EEPROM |
| | 93C46C: | 1-Kbit 5.0V Microwire Serial EEPROM w/ORG |
| **Pinout:** | Blank = | Standard pinout |
| **Tape and Reel:** | Blank = | Standard packaging |
| | T = | Tape and Reel[1] |
| **Temperature Range:** | I = | -40°C to +85°C (AEC-Q100 Grade 3) |
| | E = | -40°C to +125°C (AEC-Q100 Grade 1) |
| **Package:** | MS = | Plastic Micro Small Outline - 8-lead (MSOP) |
| | OT = | Plastic Small Outline Transistor - 6-lead (SOT-23)(Tape & Reel only) |
| | SN = | Plastic Small Outline - Narrow 3.90 mm, 8-lead (SOIC) |
| | ST = | Plastic Thin Shrink Small Outline - 4.4 mm Body, 8-lead (TSSOP) |
| **Variant[2,3]:** | 15KVAO = | Standard Automotive, 15K Process |
| | 15KVXX = | Customer-Specific Automotive, 15K Process |

**Examples:**

a) 93LC46AT-I/SN15KVAO: 1-Kbit, 128x8, 2.5V Serial EEPROM, Automotive Grade 3, Tape and Reel, SOIC package

b) 93LC46B-I/SN15KVAO: 1-Kbit, 64x16, 2.5V Serial EEPROM, Automotive Grade 3, SOIC package

c) 93LC46BT-I/OT15KVAO: 1-Kbit, 64x16, 2.5V Serial EEPROM, Automotive Grade 3, Tape and Reel, SOT-23 package

d) 93LC46BT-E/ST15KVAO: 1-Kbit, 64x16, 2.5V Serial EEPROM, Automotive Grade 1, Tape and Reel, TSSOP package

a) 93C46BT-E/SN15KVAO: 1-Kbit, 64x16, 2.5V Serial EEPROM, Automotive Grade 1, Tape and Reel, SOIC package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

**3:** For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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