E3M0900170J

1700V 900mΩ Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- 12V...15V / 0V V_{GS} compatible with most flyback controllers
- Ultra-low drain-gate capacitance
- Halogen free, RoHS compliant
- Automotive qualified (AEC-Q101) and PPAP capable

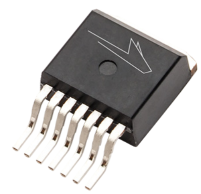
Benefits

- Smooth switching waveforms
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increases system switching frequency
- Increases system reliability

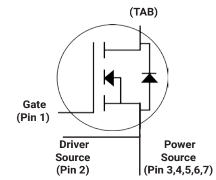
Typical Applications

- Auxillary power supplies
- Switch Mode Power Supplies
- High-Voltage capacitive loads

Package



TO-263-7



Orderable Part Number	Package	Marking
E3M0900170J-TR	TO-263-7L	E3M0900170J

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1700	V	$T_C = 25°C$	
Maximum Gate - Source Voltage (Transient)	$V_{GS(max)}$	-8		+19		Transient	
Operational Turn-On Gate-Source Voltage	$V_{GS\,op}$		+12...+15			Static	
Operational Turn-Off Gate-Source Voltage	$V_{GS\,op}$		-4...0				
DC Continuous Drain Current	I_D			4.4	A	V_{GS} =15 V, T_C = 25 °C, $T_J \le 175$ °C	Note 2
				3.3		V_{GS} =15 V, T_C = 100 °C, $T_J \le 175$°C	
Pulsed Drain Current	I_{DM}			15		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Power Dissipation	P_D			41	W	$T_C = 25$ °C, T_J = 175 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +175	°C		
Solder Temperature	T_L			260			

Note (1): Review application Note PRD-04814 for additional details
Note (2): Verified by design

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Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	3.1	4.2	V	V_{DS} = V_{GS}, I_D = 0.55 mA	Fig. 11
			2.6		V	V_{DS} = V_{GS}, I_D = 0.55 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 1700 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		900	1250	mΩ	V_{GS} = 15 V, I_D = 1.99 A	Fig. 4, 5, 6
			1938			V_{GS} = 15 V, I_D = 1.99 A, T_J = 175ºC	
g_{fs}	Transconductance		1		S	V_{DS}= 20 V, I_{DS}= 1.99 A	Fig. 7
			1			V_{DS}= 20 V, I_{DS}= 1.99 A, T_J = 175ºC	
C_{iss}	Input Capacitance		202		pF	V_{GS} = 0 V, V_{DS} = 0V to 1200 V F = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		8				
C_{rss}	Reverse Transfer Capacitance		1.4				
E_{oss}	C_{oss} Stored Energy		8		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		10		pF	V_{GS} = 0 V, V_{DS} = 0V to 1200V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		13		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		128		μJ	V_{DS}= 1200 V, V_{GS}= -4 V/15 V, I_D= 1.99 A, $R_{G(ext)}$ = 2.5 Ω, L= 1707 μH, T_J = 175ºC FWD = External SiC DIODE	Fig. 26, 28
E_{OFF}	Turn Off Switching Energy (External Diode)		13				
$t_{d(on)}$	Turn-On Delay Time		20		ns	V_{DD} = 1200 V, V_{GS} = -4 V/15 V I_D = 1.99 A, $R_{G(ext)}$ = 2.5 Ω, Tj=175⁰C, L=1707 μH Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		16				
$t_{d(off)}$	Turn-Off Delay Time		20				
t_f	Fall Time		42				
$R_{G(int)}$	Internal Gate Resistance		31		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		4		nC	V_{DS} = 1200 V, V_{GS} = -4 V/15 V I_D = 1.99 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		2				
Q_g	Total Gate Charge		8				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 1200V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 1200V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.7		V	V_{GS} = -4 V, I_{SD} = 1 A, T_J = 25 °C	Fig. 8, 9, 10
		4.2		V	V_{GS} = -4 V, I_{SD} = 1 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current	6		A	V_{GS} = -4 V, T_C = 25˚C	
I_{SM}	Diode pulse Current		15	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	22		ns	V_{GS} = -4 V, I_{SD} = 1.99 A, V_R = 1200 V dif/dt = 3710 A/µs, T_J = 25 °C	
Q_{rr}	Reverse Recovery Charge	50		nC		
I_{rrm}	Peak Reverse Recovery Current	5		A		
t_{rr}	Reverse Recover time	28		ns	V_{GS} = -4 V, I_{SD} = 1.99 A, V_R = 1200 V dif/dt = 1030 A/µs, T_J = 25 °C	
Q_{rr}	Reverse Recovery Charge	46		nC		
I_{rrm}	Peak Reverse Recovery Current	3		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	3.0	3.6	°C/W		Fig. 21

Typical Performance

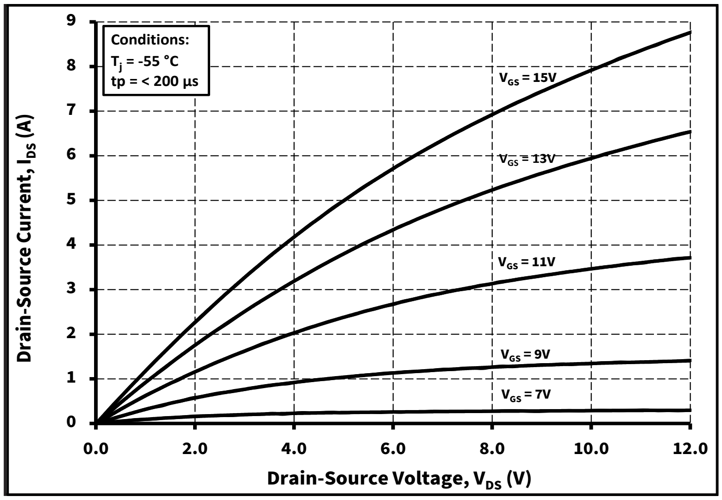


Figure 1. Output Characteristics T_J = -55 ºC

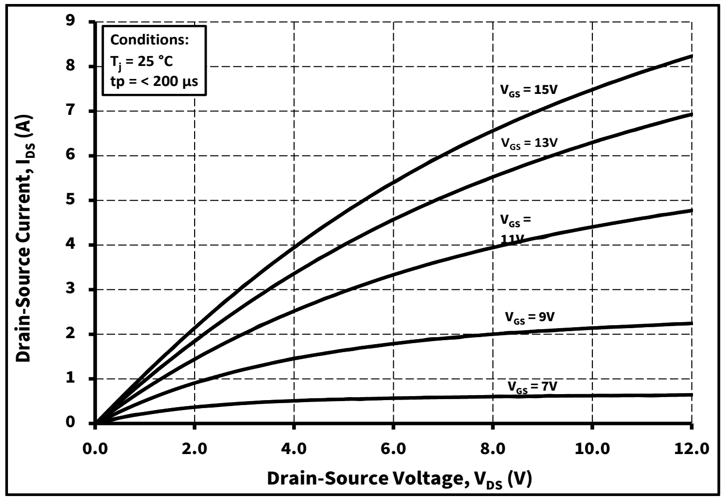


Figure 2. Output Characteristics T_J = 25 ºC

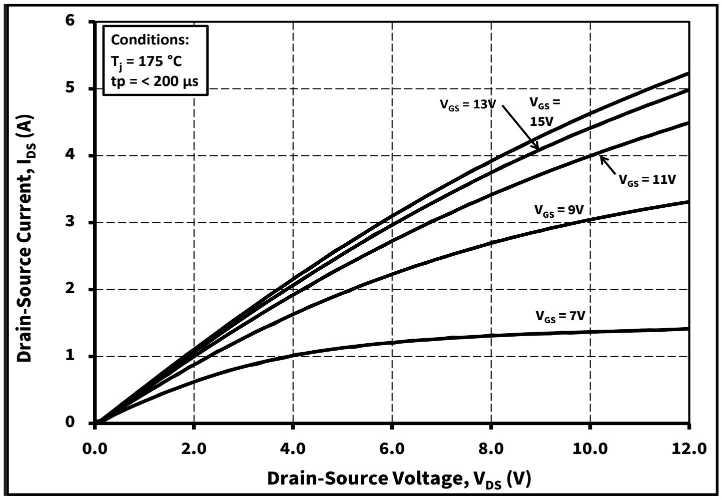


Figure 3. Output Characteristics T_J = 175 ºC

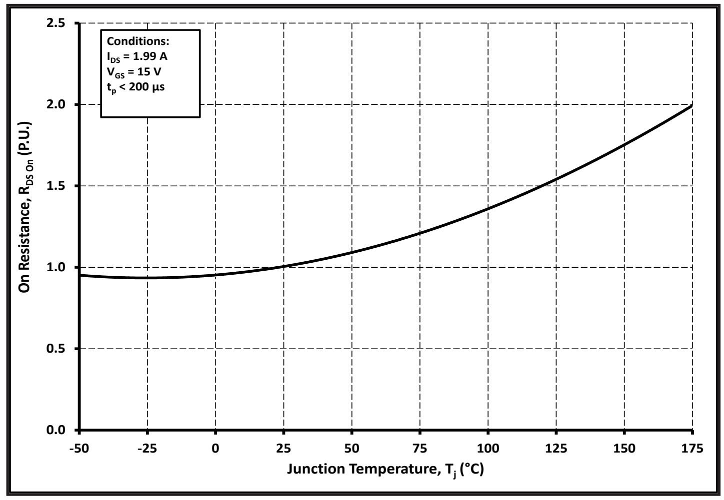


Figure 4. Normalized On-Resistance vs. Temperature

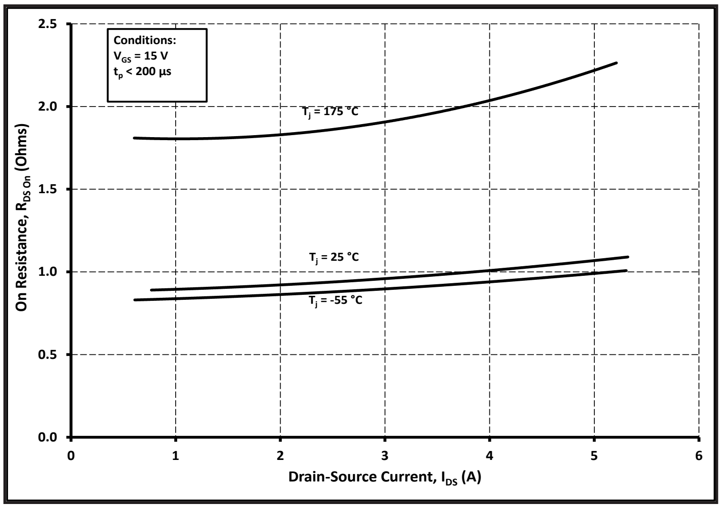


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

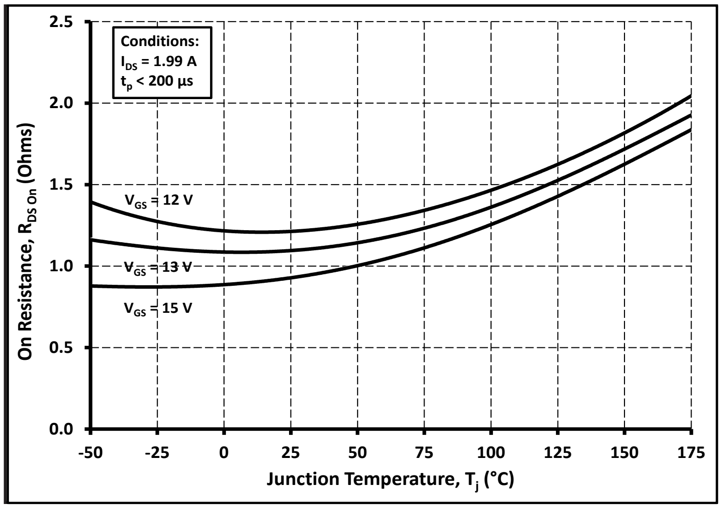


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

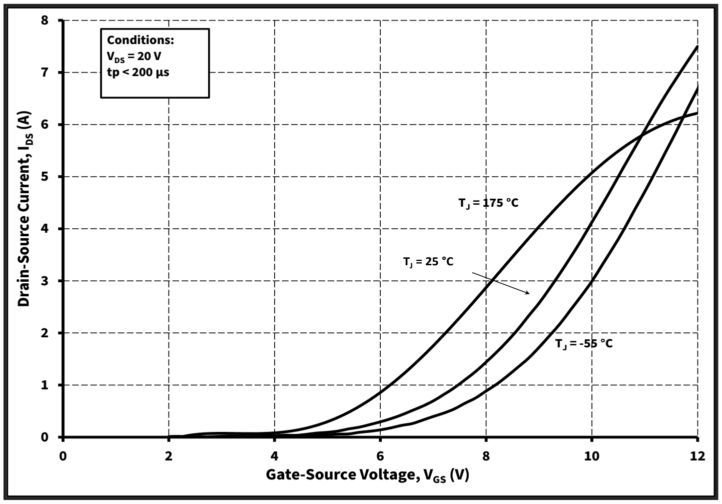


Figure 7. Transfer Characteristic for Various Junction Temperatures

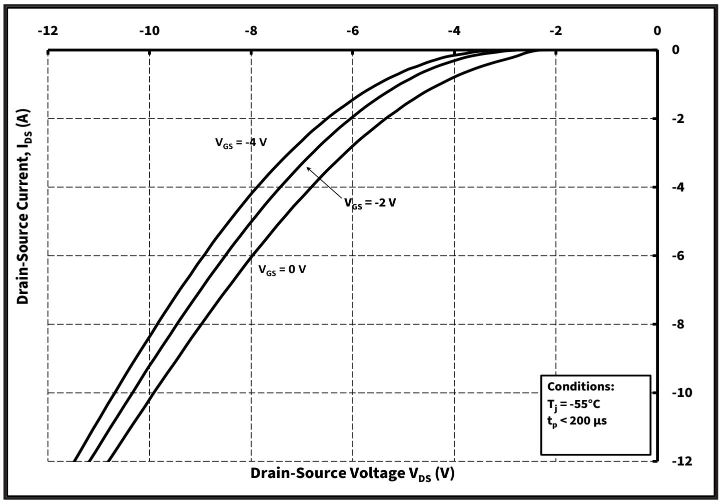


Figure 8. Body Diode Characteristic at -55 °C

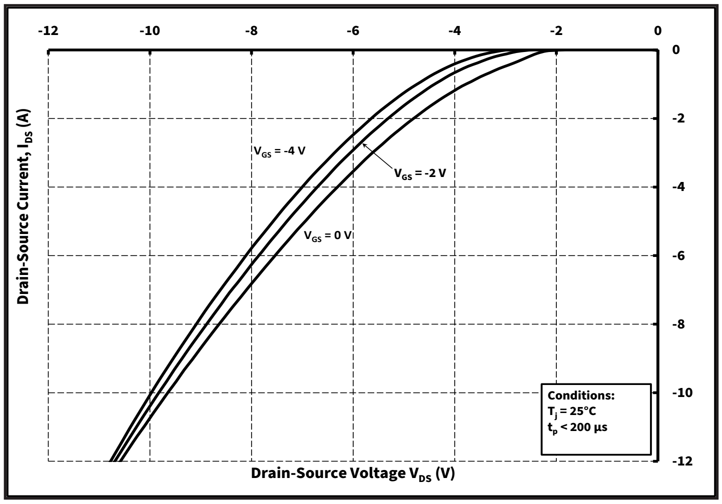


Figure 9. Body Diode Characteristic at 25 °C

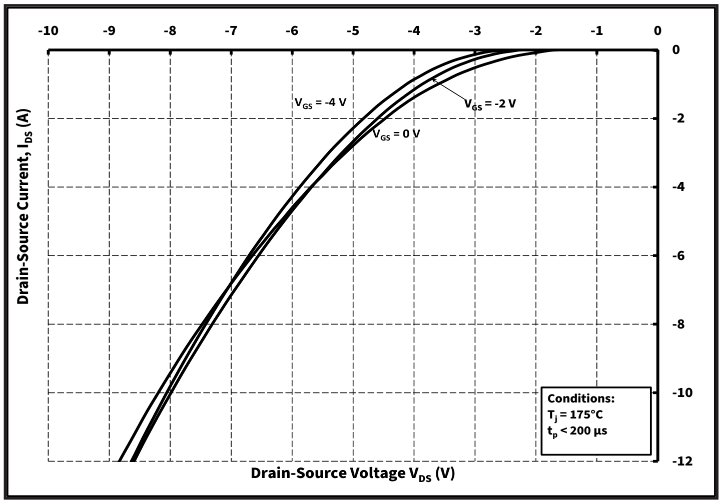


Figure 10. Body Diode Characteristic at 175 °C

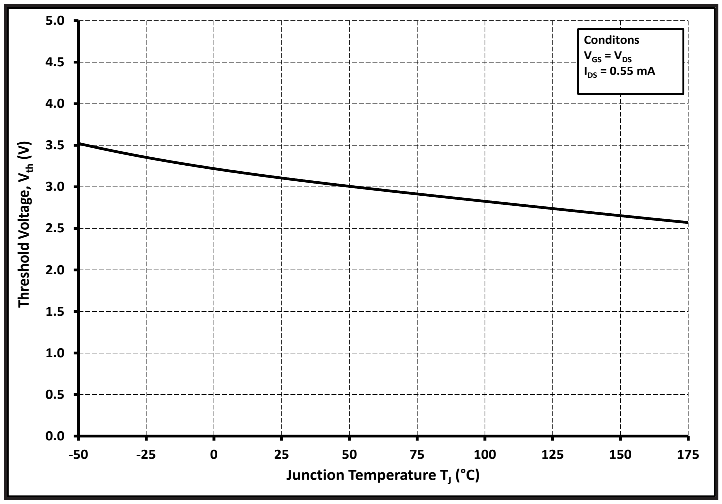


Figure 11. Threshold Voltage vs. Temperature

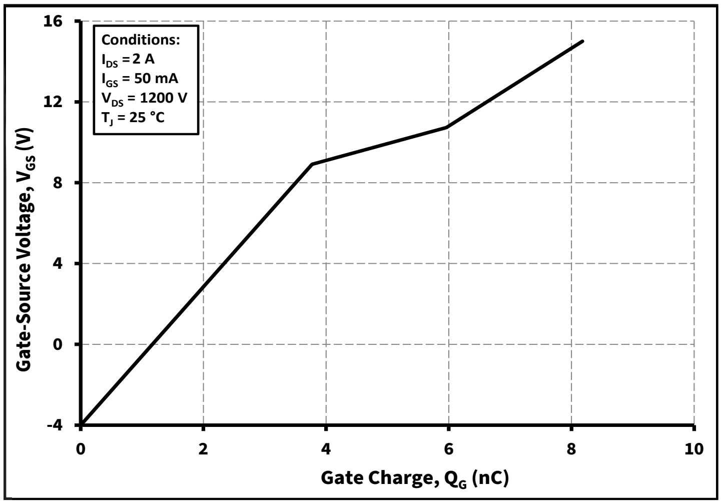


Figure 12. Gate Charge Characteristics

Typical Performance

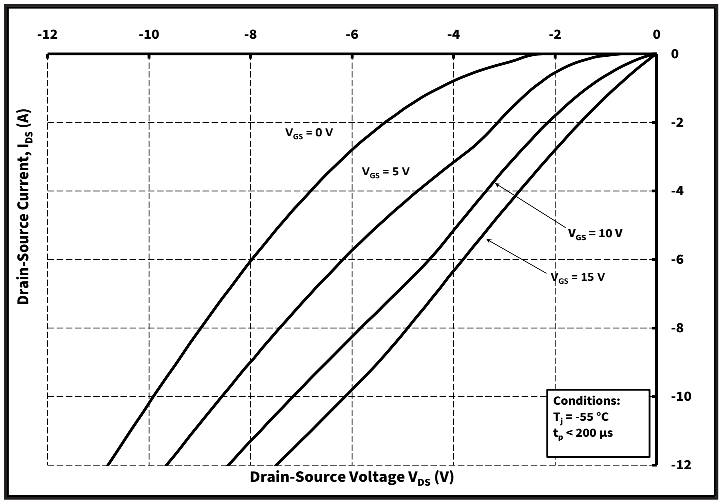


Figure 13. 3rd Quadrant Characteristic at -55 °C

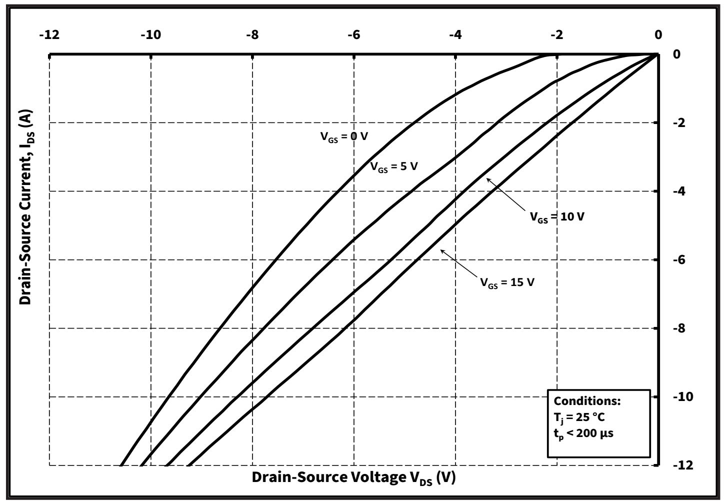


Figure 14. 3rd Quadrant Characteristic at 25 °C

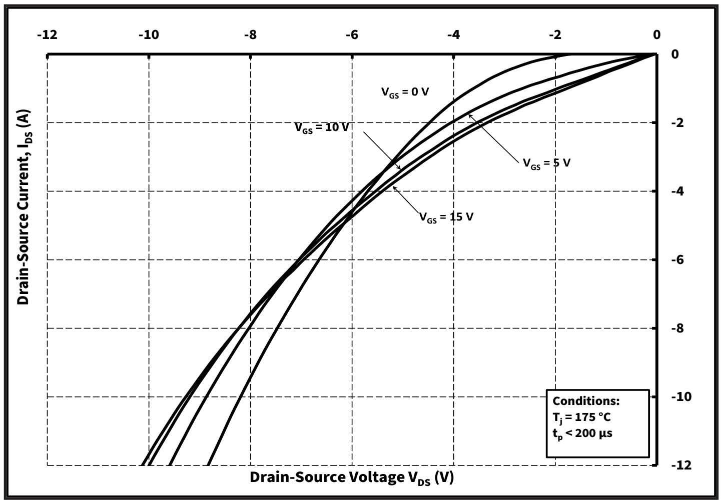


Figure 15. 3rd Quadrant Characteristic at 175 °C

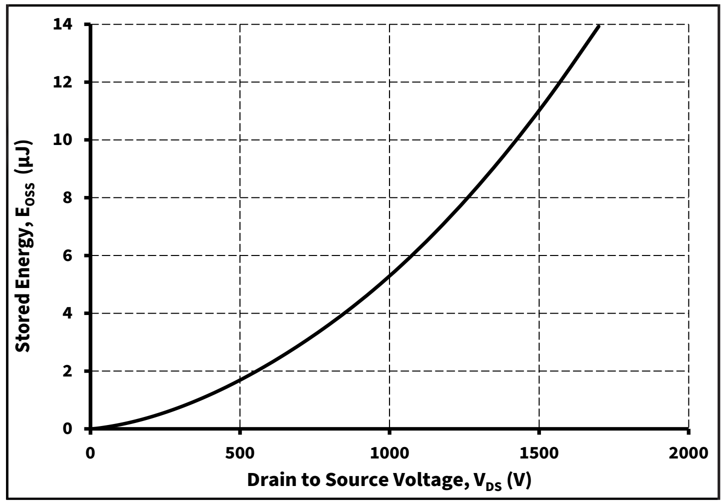


Figure 16. Output Capacitor Stored Energy

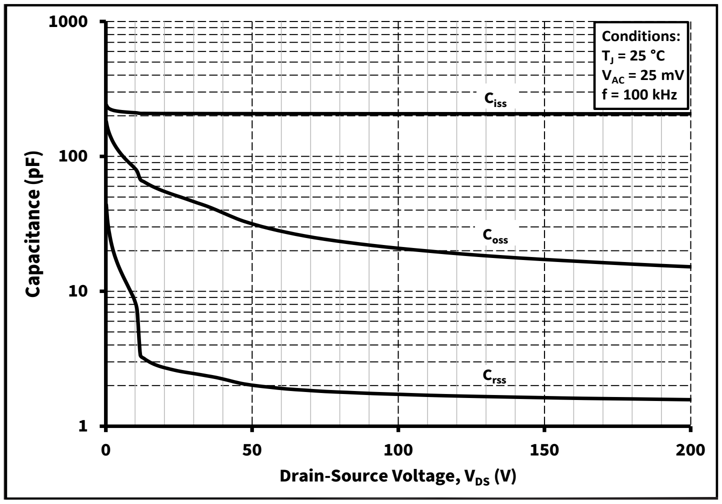


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

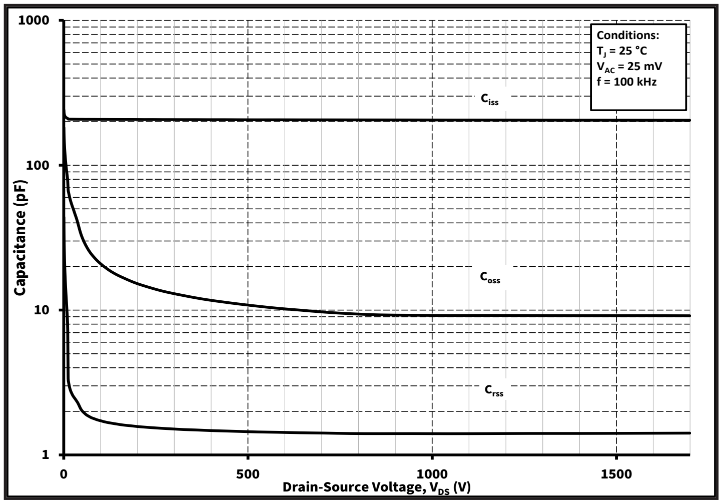


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1700V)

Typical Performance

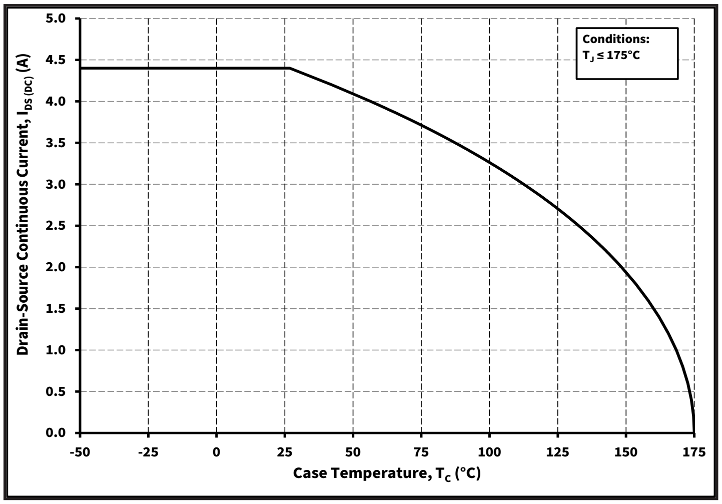


Figure 19. Continuous Drain Current Derating vs. Case Temperature

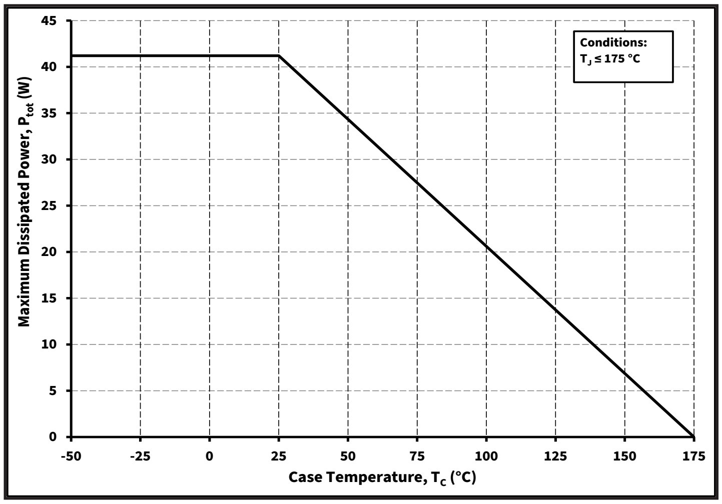


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

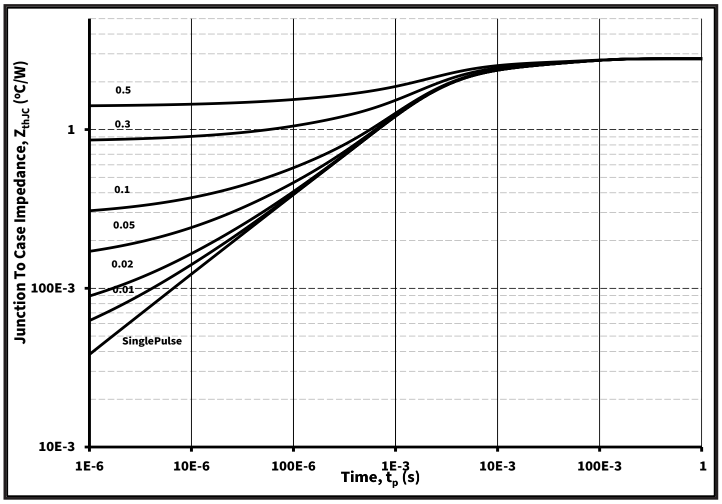


Figure 21. Transient Thermal Impedance (Junction - Case)

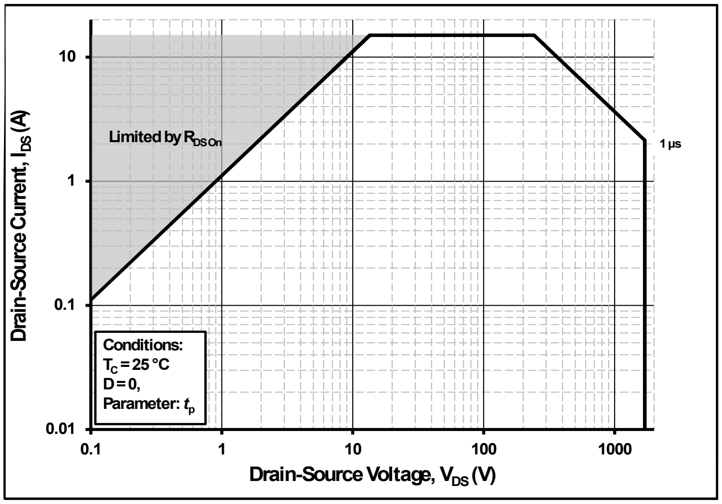


Figure 22. Safe Operating Area

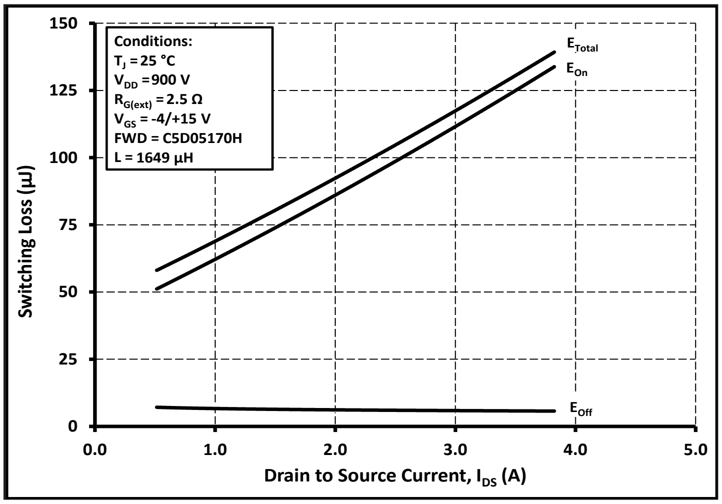


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 900V)

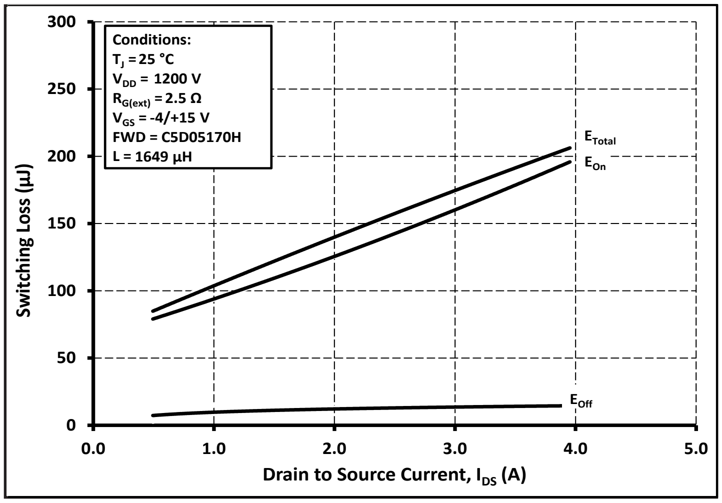


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 1200V)

Typical Performance

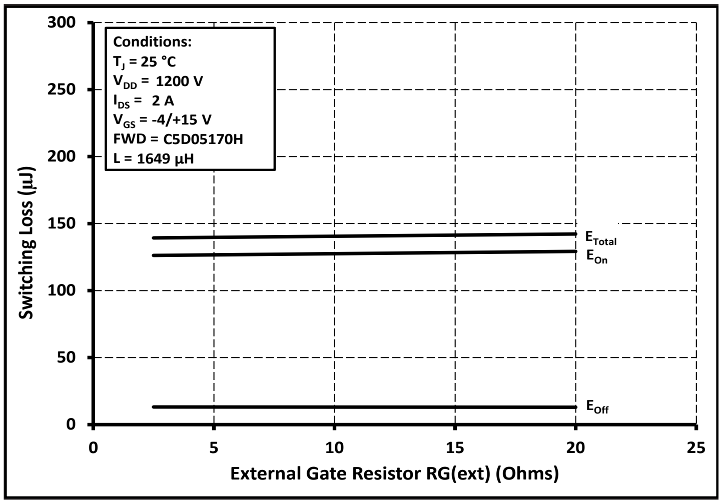


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

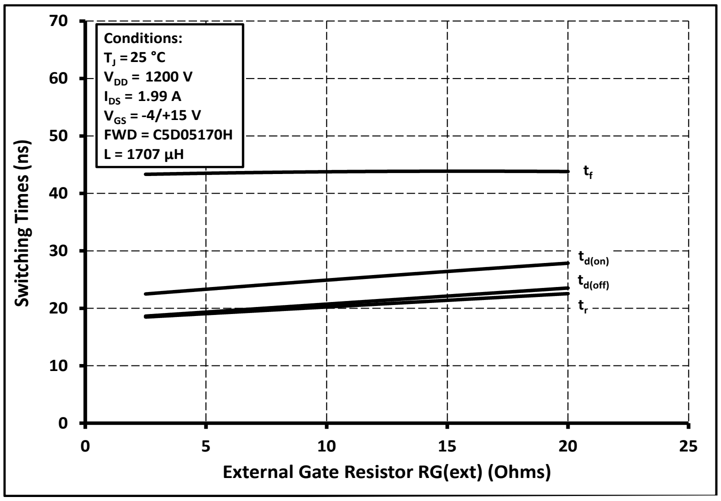


Figure 26. Switching Times vs. $R_{G(ext)}$

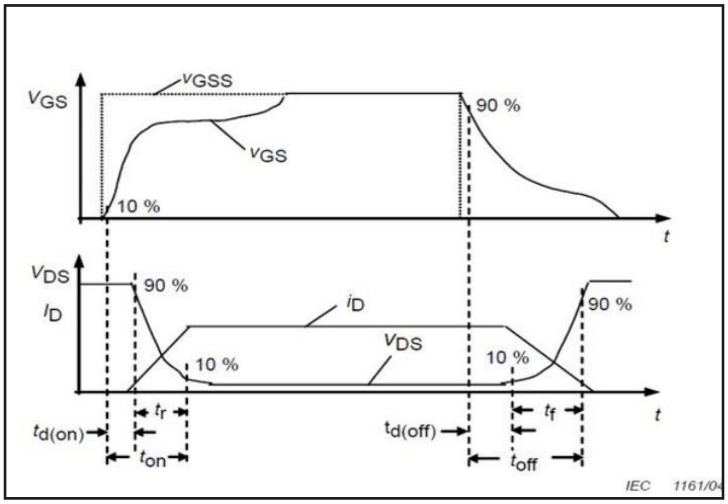


Figure 27. Switching Times Definition

Test Circuit Schematic

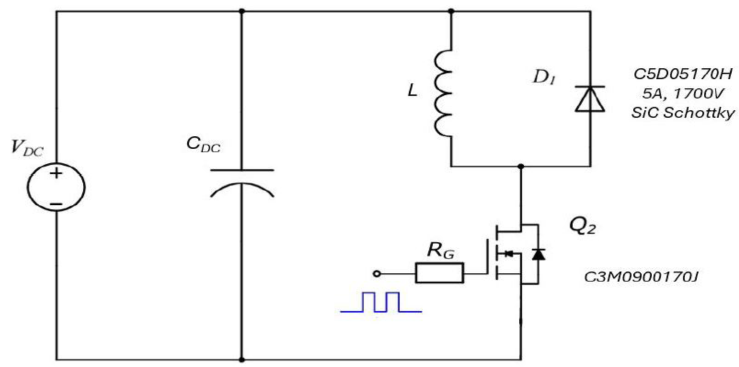
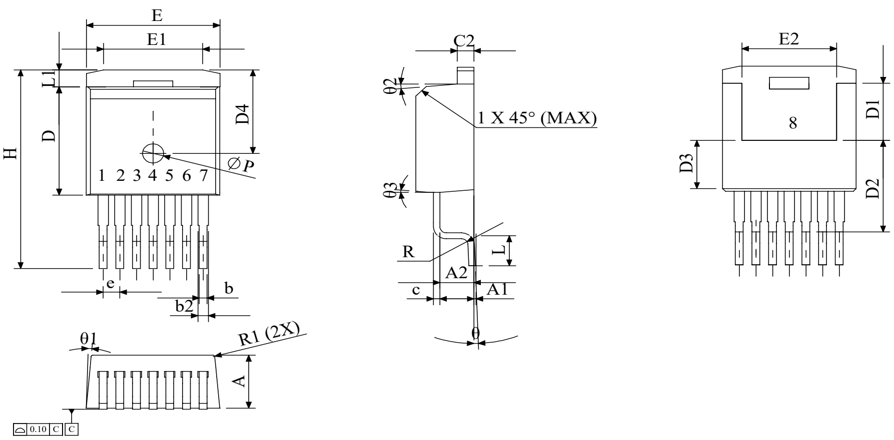


Figure 28. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.57
A1	0.00	0.25
b	0.50	0.70
b2	0.60	1.00
c	0.33	0.65
C2	1.17	1.40
D	9.025	9.125
D1	4.70	4.90
D2	7.170 REF	
D3	4.000 REF	
D4	7.000 REF	
A2	2.595 REF	
E	10.13	10.23
E1	6.50	8.60
E2	6.778	7.665
e	1.27 TYP	
H	15.043	17.313
L	2.324	2.700
L1	0.968	1.868
R	0.506 REF	
R1	0.500 REF	
θ	0°	8°
θ1	4.5°	5.5°
θ2	4°	6°
θ3	4°	6°

1	GATE
2	KELVIN
3	SOURCE
4	
5	
6	
7	
8	DRAIN

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

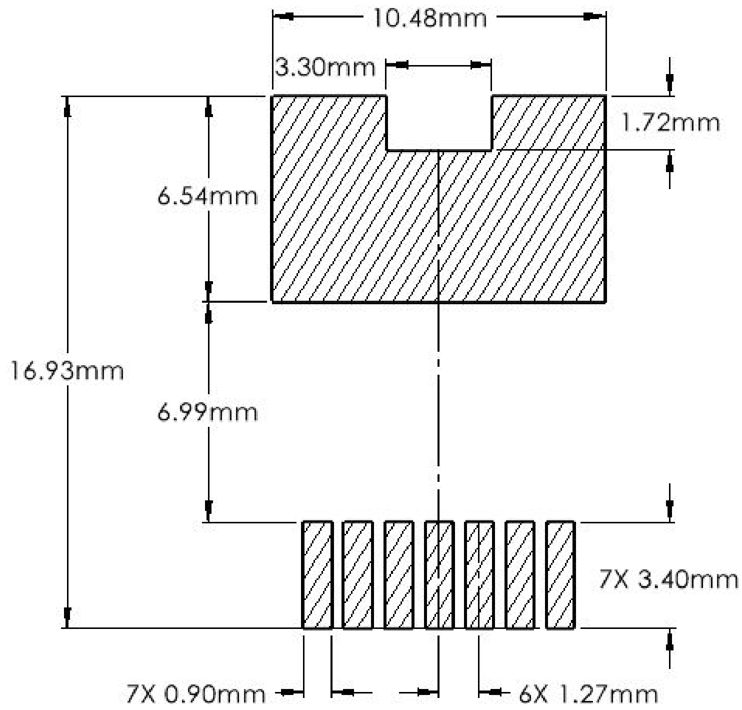
TITLE: PACKAGE OUTLINE DRAWING: TO 263-7L J

REVISION NO. 02 A4

Date: 08/12/25 PRD-05972 SCALE:1:1 SHEET 1 OF 1

Recommended Solder Pad Layout

All dimensions in mm



Revision history

Document Version	Date of release	Descriptiion of changes
1	March - 2025	Initial Release
2	September - 2025	Package drawing updated to correct dimension D1

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REACh Compliance

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